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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

Product Status	Obsolete
Туре	SC3850 Single Core
Interface	Ethernet, I ² C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8151sag1000b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
B9	M2A13	0	GVDD2
B10	VSS	Ground	N/A
B11	GVDD2	Power	N/A
B12	M2CS1	0	GVDD2
B13	VSS	Ground	N/A
B14	GVDD2	Power	N/A
B15	M2DQ35	I/O	GVDD2
B16	VSS	Ground	N/A
B17	GVDD2	Power	N/A
B18	M2DQ51	I/O	GVDD2
B19	VSS	Ground	N/A
B20	GVDD2	Power	N/A
B21	Reserved	NC	—
B22	Reserved	NC	—
B23	SR1_TXD0	0	SXPVDD1
B24	SR1_TXD0	0	SXPVDD1
B25	SXCVDD1	Power	N/A
B26	SXCVSS1	Ground	N/A
B27	SR1_RXD0	Ι	SXCVDD1
B28	SR1_RXD0	Ι	SXCVDD1
C1	M2DQ28	I/O	GVDD2
C2	M2DM3	0	GVDD2
C3	M2DQ26	I/O	GVDD2
C4	M2ECC4	I/O	GVDD2
C5	M2DM8	0	GVDD2
C6	M2ECC2	I/O	GVDD2
C7	M2CKE1	0	GVDD2
C8	M2CK0	0	GVDD2
C9	M2CK0	0	GVDD2
C10	M2BA1	0	GVDD2
C11	M2A1	0	GVDD2
C12	M2WE	0	GVDD2
C13	M2DQ37	I/O	GVDD2
C14	M2DM4	0	GVDD2
C15	M2DQ36	I/O	GVDD2
C16	M2DQ32	I/O	GVDD2
C17	M2DQ55	I/O	GVDD2
C18	M2DM6	0	GVDD2
C19	M2DQ53	I/O	GVDD2
C20	M2DQ52	I/O	GVDD2
C21	Reserved	NC	
C22	SR1_IMP_CAL_RX	I	SXCVDD1
C23	SXPVSS1	Ground	N/A
C24	SXPVDD1	Power	N/A
C25	SR1_REF_CLK	1	SXCVDD1
C26	SR1_REF_CLK	I	SXCVDD1



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
C27	Reserved	NC	_
C28	Reserved	NC	—
D1	GVDD2	Power	N/A
D2	VSS	Ground	N/A
D3	M2DQ29	I/O	GVDD2
D4	GVDD2	Power	N/A
D5	VSS	Ground	N/A
D6	M2ECC5	I/O	GVDD2
D7	GVDD2	Power	N/A
D8	VSS	Ground	N/A
D9	M2A8	0	GVDD2
D10	GVDD2	Power	N/A
D11	VSS	Ground	N/A
D12	M2A0	0	GVDD2
D13	GVDD2	Power	N/A
D14	VSS	Ground	N/A
D15	M2DQ39	I/O	GVDD2
D16	GVDD2	Power	N/A
D17	VSS	Ground	N/A
D18	M2DQ54	I/O	GVDD2
D19	GVDD2	Power	N/A
D20	VSS	Ground	N/A
D21	SXPVSS1	Ground	N/A
D22	SXPVDD1	Power	N/A
D23	SR1_TXD1	0	SXPVDD1
D24	SR1_TXD1	0	SXPVDD1
D25	SXCVSS1	Ground	N/A
D26	SXCVDD1	Power	N/A
D27	SR1_RXD1	I	SXCVDD1
D28	SR1_RXD1	I	SXCVDD1
E1	M2DQ31	I/O	GVDD2
E2	M2DQ30	I/O	GVDD2
E3	M2DQ27	I/O	GVDD2
E4	M2ECC7	I/O	GVDD2
E5	M2ECC6	I/O	GVDD2
E6	M2ECC3	I/O	GVDD2
E7	M2A9	0	GVDD2
E8	M2A6	0	GVDD2
E9	M2A3	0	GVDD2
E10	M2A10	0	GVDD2
E11	M2RAS	0	GVDD2
E12	M2A2	0	GVDD2
E13	M2DQ38	I/O	GVDD2
E14	M2DQS5	I/O	GVDD2
E15	M2DQS5	I/O	GVDD2
E16	M2DQ33	I/O	GVDD2



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
K15	VDD	Power	N/A
K16	VSS	Ground	N/A
K17	VSS	Ground	N/A
K18	VSS	Ground	N/A
K19	VDD	Power	N/A
K20	Reserved	NC	—
K21	Reserved	NC	—
K22	Reserved	NC	—
K23	SXPVDD2	Power	N/A
K24	SXPVSS2	Ground	N/A
K25	SXCVDD2	Power	N/A
K26	SXCVSS2	Ground	N/A
K27	SXCVDD2	Power	N/A
K28	SXCVSS2	Ground	N/A
L1	M2DQ9	I/O	GVDD2
L2	M2DQ12	I/O	GVDD2
L3	M2DQ13	I/O	GVDD2
L4	M2DQS0	I/O	GVDD2
L5	M2DQS0	I/O	GVDD2
L6	M2DM0	0	GVDD2
L7	M2DQ3	I/O	GVDD2
L8	M2DQ2	I/O	GVDD2
L9	M2DQ4	I/O	GVDD2
L10	VDD	Power	N/A
L11	VSS	Ground	N/A
L12	M3VDD	Power	N/A
L13	VSS	Ground	N/A
L14	VSS	Ground	N/A
L15	VSS	Ground	N/A
L16	VSS	Ground	N/A
L17	VSS	Ground	N/A
L18	VDD	Power	N/A
L19	VSS	Ground	N/A
L20	Reserved	NC	—
L21	Reserved	NC	—
L22	Reserved	NC	—
L23	SR2_TXD3/PE_TXD3/SG2_TX ⁴	0	SXPVDD2
L24	SR2_TXD3/PE_TXD3/SG2_TX ⁴	0	SXPVDD2
L25	SXCVSS2	Ground	N/A
L26	SXCVDD2	Power	N/A
L27	SR2_RXD3/PE_RXD3/SG2_RX ⁴	I	SXCVDD2
L28	SR2_RXD3/PE_RXD3/SG2_RX ⁴	I	SXCVDD2
M1	M2DQ8	I/O	GVDD2
M2	VSS	Ground	N/A
M3	GVDD2	Power	N/A
M4	M2DQ15	I/O	GVDD2

MSC8151 Single-Core Digital Signal Processor Data Sheet, Rev. 6



R13 VSS Ground NA R14 VDD Power NA R15 VSS Ground NA R16 MVDD Power NA R17 VSS Ground NA R18 VDD Power NA R19 VSS Ground NA R20 VSS Mon-user NA R21 SXPVD2 Ground NA R23 SXPVD2 Ground NA R23 SX2/XD1/PE_TXD1 ⁴ O SXPVD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVD2 R24 SR2_TXD1/PE_TXD1 ⁴ I SXCVD2 R26 SXCVD2 Power NA R26 SXCVD2 Power NA R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVD2 T1 VSS Ground NA T2 TCK I QVD T3 SRESET ^{6,7} I/O	Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
R14 VDD Power N/A R15 VSS Ground N/A R15 MVDD Power N/A R17 VSS Ground N/A R18 VDD Power N/A R19 VSS Ground N/A R19 VSS Ground N/A R20 VSS Ground N/A R21 SXPVS2 Ground N/A R22 SXPVDD2 Power N/A R23 SR2_TXDI/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXDI/PE_TXD1 ⁴ O SXPVDD2 R25 SXCVS2 Ground N/A R26 SKCVDD2 Power N/A R25 SR2_RXDI/PE_RXD1 ⁴ I SXCVD2 R26 SR2_RXDI/PE_RXD1 ⁴ I SXCVD2 R26 SR2_RXDI/PE_RXD1 ⁴ I QVD T1 VSS Ground N/A T2 TCK	R13	VSS	Ground	N/A
R15VSSGroundNAR16MVDDPowerNAR17VSSGroundNAR18VDDPowerNAR19VSSMon-userNAR20VSSMon-userNAR21SXPVS2GroundNAR22SXPVDD2GroundNAR23SXPVDD2GroundNAR24SR2_TXD1/FE_TXD14OSXPVDD2R24SR2_TXD1/FE_TXD14OSXPVDD2R24SR2_TXD1/FE_TXD14OSXPVDD2R25SXCVSS2GroundNAR26SXCVDD2GroundNAR27SR2_RXD1/FE_RXD14ISXCVDD2R28SR2_RXD1/FE_RXD14ISXCVDD2R28SR2_RXD1/FE_RXD14IOVDDT3SRESET*7I/OQVDDT4TD1IQVDDT5VSSGroundNAT6TD0OQVDDT7VSSGroundNAT10VSSGroundNAT11VDDPowerNAT11VDDPowerNAT114VSSGroundNAT15VSSGroundNAT16VSSGroundNAT17MSDPowerNAT18VSSGroundNAT14VSSGroundNAT15VDDPowerNAT16VSSGroundNA <td>R14</td> <td>VDD</td> <td>Power</td> <td>N/A</td>	R14	VDD	Power	N/A
R16 MVDD Power N/A R17 VSS Ground N/A R18 VDD Power N/A R19 VSS Ground N/A R19 VSS Non-user N/A R20 VSS Non-user N/A R21 SXPVSS2 Ground N/A R22 SXPVDD2 Power N/A R23 SR2_TXD1/PE_TXD14 O SXPVDD2 R24 SR2_TXD1/PE_TXD14 O SXPVDD2 R25 SXCVDD2 Ground N/A R26 SXCVDD2 Ground N/A R27 SR2_RXD1/PE_RXD14 I SXCVDD2 R28 SR2_RXD1/PE_RXD14 I QVDD T1 VSS Ground N/A T2 TCK I QVDD T4 TD I QVDD T7 VSS Ground N/A T18 VSS Ground	R15	VSS	Ground	N/A
R17 VSS Ground NA R18 VDD Power NA R19 VSS Ground NA R20 VSS Mon-user NA R21 SXPVSS2 Ground NA R21 SXPVDS2 Ground NA R22 SXPVDD2 Power NA R23 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R25 SXCVD2 Power NA R26 SXCVD2 Power NA R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVD2 T1 VSS Ground NA T2 TCK I QVDD T3 SRESETS ⁷ I/O QVDD T4 TDI I QVDD T7 VSS Ground NA T6 TDO O QVDD T7 VSS Ground NA </td <td>R16</td> <td>MVDD</td> <td>Power</td> <td>N/A</td>	R16	MVDD	Power	N/A
R18 VDD Power N/A R19 VSS Ground N/A R20 VSS Non-user N/A R21 SXPVS2 Ground N/A R22 SXPVDD2 Power N/A R23 SR2_TD0/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R25 SXCVSS2 Ground N/A R26 SXCVDD2 Power N/A R26 SXCVDD2 Power N/A R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 R28 SR2_RXD1/PE_RXD1 ⁴ I QVDD T1 VSS Ground N/A T2 TCK I QVDD T4 TD I QVDD T5 VSS Ground N/A T6 TDO Q QVDD T7 VSS Ground N/A T10 VSS Ground	R17	VSS	Ground	N/A
R19VSGroundNAR20VSSNon-userN/AR21SXPVSS2GroundN/AR22SXPVDD2PowerN/AR23SR_IXD1/PE_TXD14OSXPVDD2R24SRZ_TXD1/PE_TXD14OSXPVDD2R26SXCVSS2GroundN/AR26SXCVDD2PowerN/AR27SRZ_RXD1/PE_RXD14ISXCVD2R28SRZ_RXD1/PE_RXD14ISXCVD2R28SRZ_RXD1/PE_RXD14ISXCVD2R28SRZ_RXD1/PE_RXD14IQVDDT1VSSGroundN/AT2TCKIQVDDT3SRESET*7I/OQVDDT4TDIQVDDT5VSSGroundN/AT6TDOQVDDGroundN/AT7VSSGroundN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VSSGroundN/AT16VSSGroundN/AT17VSSGroundN/AT18VSSGroundN/AT19VDDPowerN/AT14VSSGroundN/AT15VSSGroundN/AT16VSSGroundN/AT17VSSGr	R18	VDD	Power	N/A
R20 VSS Non-user N/A R21 SXPVDS2 Ground N/A R23 SR2_TXD1/PE_TXD14 O SXPVDD2 R24 SR2_TXD1/PE_TXD14 O SXPVDD2 R25 SXCVDD2 Ground N/A R25 SXCVDD2 Ground N/A R26 SXCVDD2 Power N/A R27 SR2_RXD1/PE_RXD14 I SXCVD2 R28 SR2_RXD1/PE_RXD14 I SXCVD2 R1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{®,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO Q QVDD T7 VSS Ground N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground	R19	VSS	Ground	N/A
R21 SXPVSS2 Ground N/A R22 SXPVDD2 Power N/A R23 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R25 SXCVSS2 Ground N/A R26 SXCVDD2 Power N/A R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 R28 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{§,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T10 VSS Ground N/A T11 VDD Power N/A T11 VDD Power N/A T11 VSS Ground	R20	VSS	Non-user	N/A
R22 SXPVDD2 Power N/A R23 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R25 SXCVSS2 Ground N/A R26 SXCVDD2 Power N/A R26 SXCVD2 Power N/A R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD QVD T5 VSS Ground N/A T6 TDO O QVD QVD T7 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T14 VDD	R21	SXPVSS2	Ground	N/A
R23 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R24 SR2_TXD1/PE_TXD1 ⁴ O SXPVDD2 R25 SXOVSS2 Ground N/A R26 SXCVDD2 Power N/A R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 R28 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T14 VSS Ground N/A T14 VSS Ground <	R22	SXPVDD2	Power	N/A
R24 SR2_TXDT/PE_TXDT ⁴ O SXPVDD2 R25 SXCVSS2 Ground NA R26 SXCVDD2 Power N/A R27 SR2_RXDT/PE_RXDT ⁴ I SXCVDD2 R28 SR2_RXDT/PE_RXDT ⁴ I SXCVDD2 T1 VSS Ground NA T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground NA T6 TDO O QVDD T7 VSS Ground NA T8 VSS Ground NA T10 VSS Ground NA T11 VDD Power NA T11 VSS Ground NA T8 VSS Ground NA T10 VSS Ground NA T11 VDD Power NA <t< td=""><td>R23</td><td>SR2_TXD1/PE_TXD1⁴</td><td>0</td><td>SXPVDD2</td></t<>	R23	SR2_TXD1/PE_TXD1 ⁴	0	SXPVDD2
R25 SXCVSS2 Ground N/A R26 SXCVDD2 Power N/A R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 R28 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T10 VSS Ground N/A T11 VDD Power N/A T11 VSS Ground N/A T11 VSS Ground N/A T11 VSS Ground N/A T11 VSS Ground N/A T114 VSS Ground N/A <tr< td=""><td>R24</td><td>SR2_TXD1/PE_TXD1⁴</td><td>0</td><td>SXPVDD2</td></tr<>	R24	SR2_TXD1/PE_TXD1 ⁴	0	SXPVDD2
R26 SXCVDD2 Power N/A R27 \$R2_RXDT/PE_RXDT4 I SXCVDD2 R28 \$R2_RXDT/PE_RXD14 I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 \$RESET6.7 I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T11 VDD Power N/A T11 VSS Ground N/A T12 VSS Ground N/A T13 M3vDD Power N/A T14 VSS Ground N/A T13 M3vDD Power N/A T14 VSS Ground N/A	R25	SXCVSS2	Ground	N/A
R27 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 R28 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T14 VSS Ground N/A T	R26	SXCVDD2	Power	N/A
R28 SR2_RXD1/PE_RXD1 ⁴ I SXCVDD2 T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MDD Power N/A T18 VSS Ground N/A T20	R27	SR2_RXD1/PE_RXD1 ⁴	I	SXCVDD2
T1 VSS Ground N/A T2 TCK I QVDD T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T13 MSVDD Power N/A T14 VSS Ground N/A T13 MSVDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 M/DD Power N/A T18 VSS	R28	SR2_RXD1/PE_RXD1 ⁴	I	SXCVDD2
T2 TCK I QVDD T3 SRESET6.7 I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T19 VDD Power N/A T20 VSS <td>T1</td> <td>VSS</td> <td>Ground</td> <td>N/A</td>	T1	VSS	Ground	N/A
T3 SRESET ^{6,7} I/O QVDD T4 TDI I QVDD T5 VSS Ground N/A T6 TDO O QVDD T7 VSS Ground N/A T8 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T20 VSS Ground N/A T21 VSS Ground N/A T24 <td< td=""><td>T2</td><td>тск</td><td>I</td><td>QVDD</td></td<>	T2	тск	I	QVDD
T4TDIIQVDDT5VSSGroundN/AT6TDOOQVDDT7VSSGroundN/AT8VSSGroundN/AT9QVDDPowerN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT19VDDPowerN/AT11VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGVD1U2VSSGroundN/A	Т3	SRESET ^{6,7}	I/O	QVDD
T5VSSGroundN/AT6TDOOQVDDT7VSSGroundN/AT8VSSGroundN/AT9QVDDPowerN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVD2T27ReservedNC-U1M1DQ8I/OGVD1U2VSSGroundN/A	T4	TDI	I	QVDD
T6 TDO QVDD T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T19 VDD Power N/A T20 VSS Ground N/A T21 VSS Ground N/A T22 SR2_IMP_CAL_RX I SXCVDD2 T23 SXPVSS2 Ground N/A T25 SR2_	T5	VSS	Ground	N/A
T7 VSS Ground N/A T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T11 VDD Power N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T19 VD Power N/A T20 VSS Ground N/A T21 VSS Non-user N/A T22 SR2_IMP_CAL_RX I SXCVDD2 T23 SXPVSS2 Ground N/A T	Т6	TDO	0	QVDD
T8 VSS Ground N/A T9 QVDD Power N/A T10 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T11 VDD Power N/A T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T20 VSS Ground N/A T21 VSS Ground N/A T22 SR2_IMP_CAL_RX I SXCVDD2 T23 SXPVSS2 Ground N/A T24 SXPVDD2 Power N/A T25 SR2_REF_CLK I SXCVDD2	T7	VSS	Ground	N/A
T9QVDDPowerN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-U1M1DQ8I/OGroundN/AU2VSSGroundN/A	Т8	VSS	Ground	N/A
T10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPUD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-U1M1DQ8I/OGroundN/AU2VSSGroundN/A	Т9	QVDD	Power	N/A
T11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-U1M1DQ8I/OGVD11U2VSSGroundN/A	T10	VSS	Ground	N/A
T12 VSS Ground N/A T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T19 VDD Power N/A T20 VSS Ground N/A T21 VSS Ground N/A T21 VSS Ground N/A T21 VSS Non-user N/A T22 SR2_IMP_CAL_RX I SXCVDD2 T23 SXPVSS2 Ground N/A T24 SXPVDD2 Power N/A T25 SR2_REF_CLK I SXCVDD2 T26 SR2_REF_CLK I SXCVDD2 T27 Reserved NC - T28 Reserved NC -	T11	VDD	Power	N/A
T13 M3VDD Power N/A T14 VSS Ground N/A T15 VDD Power N/A T16 VSS Ground N/A T17 MVDD Power N/A T18 VSS Ground N/A T19 VDD Power N/A T20 VSS Ground N/A T21 VSS Ground N/A T22 SR2_IMP_CAL_RX I SXCVDD2 T23 SXPVSS2 Ground N/A T24 SXPVDD2 Power N/A T25 SR2_REF_CLK I SXCVDD2 T26 SR2_REF_CLK I SXCVDD2 T27 Reserved NC - T28 Reserved NC - U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T12	VSS	Ground	N/A
T14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-U1M1DQ8I/OGroundN/AU2VSSGroundN/A	T13	M3VDD	Power	N/A
T15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-U1M1DQ8I/OGVDD1U2VSSGroundN/A	T14	VSS	Ground	N/A
T16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGroundN/A	T15	VDD	Power	N/A
T17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGroundN/A	T16	VSS	Ground	N/A
T18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T18ReservedNC-U1M1DQ8I/OGroundN/A	T17	MVDD	Power	N/A
T19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNCT28ReservedNCU1M1DQ8I/OGroundU2VSSGroundN/A	T18	VSS	Ground	N/A
T20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNCU1M1DQ8I/OGVDD1U2VSSGroundN/A	T19	VDD	Power	N/A
T21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGVDD1U2VSSGroundN/A	T20	VSS	Ground	N/A
T22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGVDD1U2VSSGroundN/A	T21	VSS	Non-user	N/A
T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGVDD1U2VSSGroundN/A	T22	SR2_IMP_CAL_RX	I	SXCVDD2
T24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-T28ReservedNC-U1M1DQ8I/OGVDD1U2VSSGroundN/A	T23	SXPVSS2	Ground	N/A
T25 SR2_REF_CLK I SXCVDD2 T26 SR2_REF_CLK I SXCVDD2 T27 Reserved NC - T28 Reserved NC - U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T24	SXPVDD2	Power	N/A
T26 SR2_REF_CLK I SXCVDD2 T27 Reserved NC — T28 Reserved NC — U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T25	SR2_REF_CLK	I	SXCVDD2
T27 Reserved NC T28 Reserved NC U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T26	SR2_REF_CLK	I	SXCVDD2
T28 Reserved NC U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T27	Reserved	NC	—
U1 M1DQ8 I/O GVDD1 U2 VSS Ground N/A	T28	Reserved	NC	—
U2 VSS Ground N/A	U1	M1DQ8	I/O	GVDD1
	U2	VSS	Ground	N/A



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
U3	GVDD1	Power	N/A
U4	M1DQ15	I/O	GVDD1
U5	M1DQ1	I/O	GVDD1
U6	VSS	Ground	N/A
U7	GVDD1	Power	N/A
U8	M1DQ7	I/O	GVDD1
U9	M1DQ6	I/O	GVDD1
U10	VDD	Power	N/A
U11	VSS	Ground	N/A
U12	M3VDD	Power	N/A
U13	VSS	Ground	N/A
U14	VDD	Power	N/A
U15	VSS	Ground	N/A
U16	VDD	Power	N/A
U17	VSS	Ground	N/A
U18	VDD	Power	N/A
U19	VSS	Ground	N/A
U20	VSS	Ground	N/A
U21	VSS	Ground	N/A
U22	VSS	Non-user	N/A
U23	SR2_TXD0/PE_TXD0 ⁴	0	SXPVDD2
U24	SR2_TXD0/PE_TXD0 ⁴	0	SXPVDD2
U25	SXCVDD2	Power	N/A
U26	SXCVSS2	Ground	N/A
U27	SR2_RXD0/PE_RXD0 ⁴	I	SXCVDD2
U28	SR2_RXD0/PE_RXD0 ⁴	I	SXCVDD2
V1	M1DQ9	I/O	GVDD1
V2	M1DQ12	I/O	GVDD1
V3	M1DQ13	I/O	GVDD1
V4	M1DQS0	I/O	GVDD1
V5	M1DQS0	I/O	GVDD1
V6	M1DM0	0	GVDD1
V7	M1DQ3	I/O	GVDD1
V8	M1DQ2	I/O	GVDD1
V9	M1DQ4	I/O	GVDD1
V10	VSS	Ground	N/A
V11	VDD	Power	N/A
V12	VSS	Ground	N/A
V13	VDD	Power	N/A
V14	VSS	Ground	N/A
V15	VDD	Power	N/A
V16	VSS	Ground	N/A
V17	VDD	Power	N/A
V18	VSS	Ground	N/A
V19	VDD	Power	N/A
V20	NVDD	Power	N/A



AB1 MIDGS2 I/O GVDD1 AB2 MIDQS2 I/O GVDD1 AB3 MIDQ19 I/O GVDD1 AB4 MIDM2 0 GVDD1 AB5 MIDQ21 I/O GVDD1 AB5 MIDQ22 I/O GVDD1 AB7 MICKE0 0 GVDD1 AB8 MIA11 0 GVDD1 AB8 MIA1 0 GVDD1 AB9 MIA7 0 GVDD1 AB10 MICK2 0 GVDD1 AB11 MIAPR_QUT 0 GVDD1 AB13 MIAPR_IN 1 GVDD1 AB13 MIAPR_IN 1 GVDD1 AB14 MIDQ43 I/O GVDD1 AB15 MIDQ40 I/O GVDD1 AB17 MIDQ40 I/O GVDD1 AB18 MIDQ59 I/O GVDD1 AB20 MIDQ60 I/O N/D	Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AB2 MIDOS2 I/O GVDD1 AB3 MIDO19 I/O GVDD1 AB4 MIDM2 0 GVDD1 AB6 MIDO21 I/O GVDD1 AB6 MIDO21 I/O GVDD1 AB6 MIDO21 I/O GVDD1 AB7 MICKE0 0 GVDD1 AB8 MIA11 0 GVDD1 AB9 MIA7 0 GVDD1 AB1 MIAPAR_OUT 0 GVDD1 AB12 MIOD19 0 GVDD1 AB13 MIAPAR_OUT 0 GVDD1 AB14 MIDO43 I/O GVDD1 AB13 MIAPAR_IN 1 GVD1 AB14 MIDO43 I/O GVD1 AB15 MIDM5 0 GVD1 AB16 MIDA40 I/O GVD1 AB18 MIDC40 I/O GVD1 AB19 MIDM60 I/O N/A	AB1	M1DQS2	I/O	GVDD1
AB3 M1D019 UO GVDD1 AB4 M1D021 UO GVDD1 AB6 M1D021 UO GVDD1 AB6 M1D022 UO GVDD1 AB7 M1CKE0 O GVDD1 AB8 M1A1 O GVDD1 AB9 M1A7 O GVDD1 AB9 M1A7 O GVDD1 AB10 M1CK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1D011 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1D043 UO GVDD1 AB15 M1D04 UO GVDD1 AB16 M1D240 UO GVDD1 AB18 M1D260 UO GVDD1 AB12 VSS Ground NA AB22 GPIO271MR4RCW_SRC5 ^{5.8} IO NVDD AB23 GPIO271MR4RCW_SRC5 ^{5.8} IO <td< td=""><td>AB2</td><td>M1DQS2</td><td>I/O</td><td>GVDD1</td></td<>	AB2	M1DQS2	I/O	GVDD1
AB4 M1M2 O GVDD1 AB5 M1DQ21 I/O GVDD1 AB6 M1DQ22 I/O GVDD1 AB7 M1CKE0 O GVDD1 AB8 M1A1 O GVDD1 AB8 M1A7 O GVDD1 AB8 M1A7 O GVDD1 AB10 M1CK2 O GVDD1 AB11 M1APAR_DUT O GVDD1 AB13 M1APAR_IN I GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1D043 I/O GVD1 AB16 M1D044 I/O GVD1 AB16 M1D040 I/O GVD1 AB19 M1DM7 O GVD1 AB22 GPI031/12_SDA ^{5,8} I/O NVD AB23 GPI031/12_SDA ^{5,8} I/O NVD AB24 GPI031/12_SDA ^{5,8} I/O NVDD AB25 GPI003/172_SDA ^{5,8} I/	AB3	M1DQ19	I/O	GVDD1
AB5 M10Q21 I/O GVDD1 AB6 M1DQ22 I/O GVDD1 AB7 M1CKE0 0 GVDD1 AB8 M1A1 0 GVDD1 AB9 M1A7 0 GVDD1 AB9 M1A7 0 GVDD1 AB10 M1CK2 0 GVDD1 AB11 M1APAR_OUT 0 GVDD1 AB12 M10D11 0 GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1D43 I/O GVDD1 AB15 M1D45 0 GVDD1 AB16 M1D040 I/O GVDD1 AB17 M1D240 I/O GVDD1 AB18 M1D260 I/O GVDD1 AB20 M1D460 I/O GVD1 AB21 VSS Ground NA AB22 GPI027/TMR4/RCW_SRC2^5.8 I/O NVDD AB23 GPI026/RG5/RC5.8 I/O <	AB4	M1DM2	0	GVDD1
AB6 M1022 I/O GVD11 AB7 M1CKE0 O GVD01 AB8 M1A1 O GVD01 AB8 M1A7 O GVD01 AB9 M1A7 O GVD01 AB10 MTCKE O GVD01 AB11 M1APAR_OUT O GVD01 AB12 M10DT1 O GVD01 AB13 M1APAR_DIN I GVD01 AB14 M10A3 I/O GVD01 AB16 M1DQ40 I/O GVD01 AB17 M1DQ40 I/O GVD01 AB18 M1DQ55 I/O GVD01 AB19 M1DQ60 I/O GVD01 AB20 M1DQ60 I/O GVD01 AB23 GPI031/2C, SDA ^{5,8} I/O NVDD AB24 GPI031/2C, SDA ^{5,8} I/O NVDD AB25 GPI031/2C, SDA ^{5,8} I/O NVDD AB26 GPI01/MR1/RCW_SRC2 ^{5,8} </td <td>AB5</td> <td>M1DQ21</td> <td>I/O</td> <td>GVDD1</td>	AB5	M1DQ21	I/O	GVDD1
AB7 MCKE0 O GVDD1 AB8 M1A11 O GVDD1 AB9 M1A7 O GVDD1 AB10 MTCK2 O GVDD1 AB10 MTCK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 MTAPAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB16 M1DQ44 I/O GVDD1 AB16 M1DQ44 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ69 I/O GVDD1 AB21 VSS I/O NVDD AB22 GPI03/I2C_SDA ^{5,8} I/O NVDD AB23 GPI02/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB24 GPI02/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI00/IRG0/RC5 ^{6,6,}	AB6	M1DQ22	I/O	GVDD1
AB8 M1A1 O GVDD1 AB9 M1A7 O GVDD1 AB10 M1GK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB16 M1DQ43 I/O GVDD1 AB16 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB21 VSS Ground N/A AB22 GPIO31/2C_SDA ^{8,3} I/O N/DD AB23 GPIO27/MR4/RCW_SRC6 ^{5,8} I/O N/DD AB24 GPIO27/MR4/RCW_SRC6 ^{5,8} I/O N/DD AB25 GPIO21/MR1/RCW_SRC5 ^{5,8} I/O N/DD AB26 GPIO03/RG3/RC5 ^{5,8} I/O N/DD AC1 VSS Ground N/A AC2 <td>AB7</td> <td>M1CKE0</td> <td>0</td> <td>GVDD1</td>	AB7	M1CKE0	0	GVDD1
AB9 M1A7 O GVDD1 AB10 MTCRZ O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DQ44 I/O GVDD1 AB17 M1DQ59 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB20 M1DQ59 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI027/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPI00/IRQ16/RC16,8 I/O NVDD AB26 GPI00/IRQ16/RC16,8 I/O NVDD AB27 GPI05/IRQ5/RC5,8 I/O NVDD	AB8	M1A11	0	GVDD1
AB10 MTCK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 MTAPAR_IN I GVDD1 AB14 M1DC43 IO GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DC43 IO GVDD1 AB16 M1DC44 IO GVDD1 AB17 M1DC40 IO GVDD1 AB18 M1DC49 O GVDD1 AB18 M1DC40 IO GVDD1 AB20 M1DC60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/2C_SDA ^{5,8} I/O NVDD AB23 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI00/IRG0/RC0 ^{6,8} I/O NVDD AB28 GPI00/IRG0/RC0 ^{6,8} I/O NVD AC1 </td <td>AB9</td> <td>M1A7</td> <td>0</td> <td>GVDD1</td>	AB9	M1A7	0	GVDD1
AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DQ43 I/O GVDD1 AB16 M1DQ44 I/O GVDD1 AB16 M1DQ40 I/O GVDD1 AB18 M1DQ40 I/O GVDD1 AB19 M1DQ40 I/O GVDD1 AB20 M1DQ60 I/O GVD1 AB21 VSS Ground N/A AB22 GPIO2/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB23 GPIO2/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB24 GPIO2/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB25 GPIO2/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB26 GPIO10/RGG/RC5 ^{6,8} I/O NVDD AB27 GPIO5/RGG/RC5 ^{5,8} I/O NVD AC1 VSS Ground N/A <td>AB10</td> <td>M1CK2</td> <td>0</td> <td>GVDD1</td>	AB10	M1CK2	0	GVDD1
AB12 M10DT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1D043 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1D044 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ40 I/O GVDD1 AB18 M1DQ40 I/O GVDD1 AB18 M1DQ40 O GVD1 AB18 M1DQ59 I/O GVD1 AB20 M1DQ60 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI02/TIMR/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI02/TIMR/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPI02/TIMR/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI00/IRQ0/RC10 ^{5,8} I/O NVDD AB27 GPI00/IRQ0/RC10 ^{5,8} I/O NVDD	AB11	M1APAR_OUT	0	GVDD1
AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DMS O GVDD1 AB15 M1DQ44 I/O GVDD1 AB16 M1DQ44 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPIO3/I2C_SDA ^{5,8} I/O NVDD AB23 GPIO2/TIME4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPIO2/TIME4/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPIO2/TIME4/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPIO1/IRG10/RC10 ^{5,8} I/O NVDD AB27 GPIO3/IRG2/RC5 ^{5,8} I/O NVDD AB28 GPIO1/IRG10/RC10 ^{5,8} I/O NVDD AB29 GPIO1/IRG3/RC10 ^{5,8} I/O	AB12	M1ODT1	0	GVDD1
AB14 M1DQ43 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DQ44 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DA7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPIO31/I2C_SDA ^{5,8} I/O NVDD AB23 GPIO27/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPIO25/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPIO24/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPIO10/IRQ10/RC16 ^{5,3} I/O NVDD AB27 GPIO5/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPIO1/IRQ10/RC16 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A	AB13	M1APAR_IN	I	GVDD1
AB15 M1DM5 O GVD1 AB16 M1D044 I/O GVD1 AB17 M1D040 I/O GVD1 AB17 M1D059 I/O GVD1 AB18 M1D059 I/O GVD1 AB19 M1DM7 O GVD1 AB20 M1D060 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI00/IRQ10/RC10 ^{6,8} I/O NVDD AB27 GPI03/IRQ5/RC5 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC2 GVD1 Power N/A AC3 M1D016 I/O GVD1	AB14	M1DQ43	I/O	GVDD1
AB16 M1DQ44 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB18 M1DQ60 I/O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI026/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI02/TRQ7/RC10 ^{5,8} I/O NVDD AB26 GPI01/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI06/IRQ5/RC5 ^{6,8} I/O NVDD AB28 GPI00/IRQ1/RQ6/RC5 ^{6,8} I/O NVDD AB28 GPI00/IRQ1/RQ6/RC5 ^{6,8} I/O NVDD AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground	AB15	M1DM5	0	GVDD1
AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground NA AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC0 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ10/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A </td <td>AB16</td> <td>M1DQ44</td> <td>I/O</td> <td>GVDD1</td>	AB16	M1DQ44	I/O	GVDD1
AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/12C_SDA ^{5.8} I/O NVDD AB23 GPI027/TIMR4/RCW_SRC0 ^{5.8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5.8} I/O NVDD AB25 GPI021/IRQ10/RC10 ^{5.8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5.8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5.8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC6 M1DQ17 I/O GVD1 AC4 VSS Ground N/A	AB17	M1DQ40	I/O	GVDD1
AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI027/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRG6/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC10 VSS Ground N/A <td>AB18</td> <td>M1DQ59</td> <td>I/O</td> <td>GVDD1</td>	AB18	M1DQ59	I/O	GVDD1
AB20 M1DQ80 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5.8} I/O NVDD AB23 GPI025/TIMR2/KCW_SRC0 ^{5.8} I/O NVDD AB24 GPI025/TIMR2/RCW_SRC1 ^{5.8} I/O NVDD AB25 GPI024/TIMR1/RCW_SRC2 ^{5.8} I/O NVDD AB26 GPI001/RQT0/RC10 ^{5.8} I/O NVDD AB27 GPI05//RQ5/RC5 ^{5.8} I/O NVDD AB28 GPI00//RQ0/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC6 GVD1 Power N/A AC6 GVD1 Power N/A	AB19	M1DM7	0	GVDD1
AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5.8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5.8} I/O NVDD AB24 GPI028/TMR2/RCW_SRC1 ^{5.8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5.8} I/O NVDD AB26 GPI010/IRC10/RC10 ^{5.8} I/O NVDD AB27 GPI05/IRC5/RC5 ^{5.8} I/O NVDD AB28 GPI00/IRC0/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 MIDQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 MIDQ17 I/O GVD1 AC5 GVDD1 Power N/A AC6 MIDQ17 I/O GVD1 AC6 MIDQ17 I/O GVD1 AC6 MIDQ1 Power N/A	AB20	M1DQ60	I/O	GVDD1
AB22 GPI031/J2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{6,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A <	AB21	VSS	Ground	N/A
AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010//RQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05//RQ3//RC5 ^{5,8} I/O NVDD AB28 GPI00//RQ3//RC5 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1D016 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1D016 I/O GVD1 AC6 M1D017 I/O GVD1 AC6 M1D017 I/O GVD1 AC6 M1D017 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC9 M1BA2 O GVD1 <t< td=""><td>AB22</td><td>GPIO31/I2C_SDA^{5,8}</td><td>I/O</td><td>NVDD</td></t<>	AB22	GPIO31/I2C_SDA ^{5,8}	I/O	NVDD
AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC10 VSS Ground N/A AC11	AB23	GPIO27/TMR4/RCW_SRC0 ^{5,8}	I/O	NVDD
AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC9 M1BA2 O GVD1 AC10 VSS Ground N/A AC11 GVD1 Power N/A AC8 GVD1 Power N/A AC9 M1BA2 O GVD1 AC10 VSS Ground N/A AC11 GVD1 <td< td=""><td>AB24</td><td>GPIO25/TMR2/RCW_SRC1^{5,8}</td><td>I/O</td><td>NVDD</td></td<>	AB24	GPIO25/TMR2/RCW_SRC1 ^{5,8}	I/O	NVDD
AB26GPI010/IRQ10/RC10 ^{5.8} I/ONVDDAB27GPI05/IRQ5/RC5 ^{5.8} I/ONVDDAB28GPI00/IRQ0/RC0 ^{5.8} I/ONVDDAC1VSSGroundN/AAC2GVDD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC11GVDD1PowerN/AAC3M1A2OGVDD1AC4VSSGroundN/AAC5GVD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVD1PowerN/AAC9M1BA2OGVD1AC11GVDD1PowerN/AAC11GVD1PowerN/AAC12M1A4OGVD1AC13VSSGroundN/AAC14GVD1PowerN/AAC15M1DQ42I/OGVD1AC16VSSGroundN/AAC17GVD1PowerN/AAC18M1DQ58I/OGVD1	AB25	GPIO24/TMR1/RCW_SRC2 ^{5,8}	I/O	NVDD
AB27GPIO5/IRQ5/RC5 ^{5.8} I/ONVDDAB28GPIO0/IRQ0/RC0 ^{5.8} I/ONVDDAC1VSSGroundN/AAC2GVD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVD1PowerN/AAC9M1BA2OGVD11AC11GVD1PowerN/AAC12M1A4OGVD11AC13VSSGroundN/AAC14GVD1PowerN/AAC15M1DQ42I/OGVD11AC16VSSGroundN/AAC17GVD1PowerN/AAC18M1DQ58I/OGVD14	AB26	GPIO10/IRQ10/RC10 ^{5,8}	I/O	NVDD
AB28 GPIOUÍRQO/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 GVD1 O GVD1 AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 O GVD1 AC7 VSS Ground N/A AC8 GVD1 O GVD1 AC10 VSS Ground N/A AC11 GVD1 O GVD1 AC12 M1A4 O GVD1 AC14 GVD1 O GVD1 AC15 M1DQ42 I/O GVD1 AC16 VSS Ground N/A AC17 GVD1 GVD1 Power N/A	AB27	GPI05/IRQ5/RC5 ^{5,8}	I/O	NVDD
AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 M1DQ17 Power N/A AC6 M1DQ17 I/O GVDD1 AC7 VSS Ground N/A AC8 GVDD1 Power N/A AC9 M1BA2 O GVDD1 AC10 VSS Ground N/A AC11 GVDD1 Power N/A AC12 M1A4 O GVDD1 AC13 VSS Ground N/A AC14 GVDD1 Power N/A AC15 M1DQ42 I/O GVDD1 AC16 VSS Ground N/A AC17 GVDD1 MA GVD1 MA	AB28	GPIO0/IRQ0/RC0 ^{5,8}	I/O	NVDD
AC2GVDD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC1	VSS	Ground	N/A
AC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC2	GVDD1	Power	N/A
AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17//OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC3	M1DQ16	I/O	GVDD1
AC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC4	VSS	Ground	N/A
AC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC5	GVDD1	Power	N/A
AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC6	M1DQ17	I/O	GVDD1
AC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC7	VSS	Ground	N/A
AC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC8	GVDD1	Power	N/A
AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC9	M1BA2	0	GVDD1
AC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC10	VSS	Ground	N/A
AC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC11	GVDD1	Power	N/A
AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC12	M1A4	0	GVDD1
AC14 GVDD1 Power N/A AC15 M1DQ42 I/O GVDD1 AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC13	VSS	Ground	N/A
AC15 M1DQ42 I/O GVDD1 AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC14	GVDD1	Power	N/A
AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC15	M1DQ42	I/O	GVDD1
AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC16	VSS	Ground	N/A
AC18 M1DQ58 I/O GVDD1	AC17	GVDD1	Power	N/A
	AC18	M1DQ58	I/O	GVDD1



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL ^{5,8}	I/O	NVDD
AC24	GPIO26/TMR3 ^{5,8}	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0 ^{5,8}	I/O	NVDD
AC28	GPIO22 ^{5,8}	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	0	GVDD1
AD8	M1A6	0	GVDD1
AD9	M1A3	0	GVDD1
AD10	M1A10	0	GVDD1
AD11	M1RAS	0	GVDD1
AD12	M1A2	0	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	M1DQS5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	M1DQS7	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	0	NVDD
AD23	GPIO15/DDN0/IRQ15/RC15 ^{5,8}	I/O	NVDD
AD24	GPIO13/IRQ13/RC13 ^{5,8}	I/O	NVDD
AD25	GE_MDC	0	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3 ³	I/O	NVDD
AD28	TDM2RCK/GE1_TD0 ³	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AE9	M1A8	0	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	0	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD ^{5,8}	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK ³	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL ³	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK ³	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK ³	I/O	NVDD
AE27	TDM2RSN/GE1_TD2 ³	I/O	NVDD
AE28	TDM2RDT/GE1_TD1 ³	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	0	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	0	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	0	GVDD1
AF8	M1CK0	0	GVDD1
AF9	M1CK0	0	GVDD1
AF10	M1BA1	0	GVDD1
AF11	M1A1	0	GVDD1
AF12	M1WE	0	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	0	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	0	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD ^{5,8}	I/O	NVDD
AF22	TDM0RSN/GE2_TD2 ³	I/O	NVDD
AF23	TDM0TDT/GE2_TD3 ³	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL ³	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD



Using this waveform, the definitions are listed in Table 10. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signalling environment.

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals $SR[1-2]_TX$, $\overline{SR[1-2]_TX}$, $SR[1-2]_RX$ and $\overline{SR[1-2]_RX}$ each have a peak-to-peak swing of A – B volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, V _{OD} (or Differential Output Swing):	The differential output voltage (or swing) of the transmitter, V _{OD} , is defined as the difference of the two complimentary output voltages: $V_{SR[1-2]_TX} - V_{\overline{SR[1-2]_TX}}$. The V _{OD} value can be either positive or negative.
Differential Input Voltage, V _{ID} (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SR[1-2]_RX} - V_{\overline{SR[1-2]_RX}}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V _{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = A - B $ volts.
Differential Peak-to-Peak, V _{DIFFp-p}	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times (A - B) $ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times V_{OD} $.
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal ($\overline{SR[1-2]}_{TX}$, for example) from the non-inverting signal ($\overline{SR[1-2]}_{TX}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 16 as an example for differential waveform.
Common Mode Voltage, V _{cm}	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SR[1-2]_TX} + V_{SR[1-2]_TX}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

Table 10. Differential Signal Definitions

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.



2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.







Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 11. PCI Ex	oress (2.5 Gbps) Differential Transmitter	(Tx) Out	put DC Specifications
	(p:000 (=:0 00p0		(1), 000	

Parameter	Symbol	Min	Typical	Мах	Units	Notes	
Differential peak-to-peak output voltage	V _{TX-DIFFp-p}	800	1000	1200	mV	1	
De-emphasized differential output voltage (ratio)	V _{TX-DE-RATIO}	3.0	3.5	4.0	dB	2	
DC differential Tx impedance	Z _{TX-DIFF-DC}	80	100	120	Ω	3	
Transmitter DC impedance	Z _{TX-DC}	40	50	60	Ω	4	
Notes: 1 Very and 2 X Wey - Very - Measured at the package pips with a test load of 50.0 to GND on each pip							

V_{TX-DIFFp-p} = 2 × |V_{TX-D} - V_{TX-D}| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 Ratio of the V_{TX-DIFFp-p} of the second and following bits after a transition divided by the V_{TX-DIFFp-p} of the first bit after a

transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.

3. Tx DC differential mode low impedance

4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Notes
Differential input peak-to-peak voltage	V _{RX-DIFFp-p}	120	1000	1200	mV	1
DC differential Input Impedance	Z _{RX-DIFF-DC}	80	100	120	Ω	2
DC input impedance	Z _{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	Z _{RX-HIGH-IMP-DC}	50	—	—	ΚΩ	4
Electrical idle detect threshold	V _{RX-IDLE-DET-DIFFp-p}	65	—	175	mV	5

Notes: 1. V_{RX-DIFFp-p} = 2 × |V_{RX-D+} - V_{RX-D-}| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Output voltage	V _O	-0.40	—	2.30	V	1
Long run differential output voltage	V _{DIFFPP}	800	—	1600	mVp-p	—
Short run differential output voltageVV500—1000mVp-p						—
Note: Voltage relative to COMMON of either signal comprising a differential pair.						



Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.



Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time	t _{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	^t DDKHAS	0.917 1.10		ns ns	3
ADDR/CMD output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	^t DDKHAX	0.767 1.02		ns ns	3
MCSn output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	^t DDKHCS	0.917 1.10		ns ns	3
MCSn output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	tddkhcx	0.767 1.02		ns ns	3
MCK to MDQS Skew • 800 MHz data rate • 667 MHz data rate	t _{DDKHMH}	-0.4 -0.6	0.375 0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 800 MHz 667 MHz 	^t DDKHDS, ^t DDKLDS	300 375		ps ps	5
MDQ/MECC/MDM output hold with respect to MDQS 800 MHz 667 MHz 	t _{DDKHDX,} t _{DDKLDX}	300 375	_	ps ps	5
MDQS preamble	t _{DDKHMP}	$-0.9 \times t_{MCK}$	_	ns	_
MDQS postamble	t _{DDKHME}	$-0.4 imes t_{MCK}$	$-0.6 imes t_{MCK}$	ns	—

Table 21. DDR SDRAM Output AC Timing Specifications

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Table 22 provides the DDR2 differential specifications for the differential signals MDQS/MDQS and MCK/MCK.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V _{IXAC}	0.5 imes GVDD - 0.175	0.5 × GVDD + 0.175	V
Output AC differential cross-point voltage	V _{OXAC}	0.5 imes GVDD - 0.125	0.5 × GVDD + 0.125	V

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/MDQS and MCK/MCK.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
Input AC differential cross-point voltage	V _{IXAC}	0.5 imes GVDD - 0.150	0.5 × GVDD + 0.150	V
Output AC differential cross-point voltage	V _{OXAC}	0.5 imes GVDD - 0.115	0.5 × GVDD + 0.115	V

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK frequency range	^t CLK_REF	—	100/125	_	MHz	1
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK clock frequency tolerance	^t CLK_TOL	-350	—	350	ppm	—
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK reference clock duty cycle (measured at 1.6 V)	^t CLK_DUTY	40	50	60	%	_
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK max deterministic peak-peak jitter at 10 ⁻⁶ BER	^t clk_dj	_	—	42	ps	—
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK total reference clock jitter at 10 ⁻⁶ BER (peak-to-peak jitter at ref_clk input)	^t clk_tj	_	_	86	ps	2
SR[1–2]_REF_CLK/SR[1–2]_REF_CLK rising/falling edge rate	^t clkrr/ ^t clkfr	1	—	4	V/ns	3
Differential input high voltage	V _{IH}	200	—	—	mV	4
Differential input low voltage	V _{IL}	_	_	-200	mV	4
Rising edge rate (SR[1–2]_REF_CLK) to falling edge rate (SR[1–2]_REF_CLK) matching	Rise-Fall Matching	_	_	20	%	5, 6

Table 24. SR[1–2]_REF_CLK and SR[1–2]_REF_CLK Input Clock Requirements



2.6.7 Asynchronous Signal Timing

Table 35 lists the asynchronous signal timing specifications.

Table 37. Signal Timing

Characteristics		Symbol	Туре	Min		
Input		t _{IN}	Asynchronous	One CLKIN cycle		
Output		t _{OUT}	Asynchronous	Application dependent		
Note:	Input value relevant for EE0, IRQ[15–0], and NMI only.					

The following interfaces use the specified asynchronous signals:

• *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8151 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- Boot function. Signal STOP_BS.
- I^2C interface. Signals I2C_SCL and I2C_SDA.
- Interrupt inputs. Signals IRQ[15–0] and NMI.
- Interrupt outputs. Signals INT_OUT and NMI_OUT (minimum pulse width is 32 ns).

2.6.8 JTAG Signals

Table 38 lists the JTAG timing specifications shown in Figure 29 through Figure 32.

Table 38. JTAG Timing

Characteristics		All frequencies		Unit	
Characteristics	Symbol	Min	Max	Unit	
TCK cycle time	t _{тскх}	36.0	—	ns	
TCK clock high phase measured at $V_{M} = V_{DDIO}/2$	t _{тскн}	15.0	—	ns	
Boundary scan input data setup time	t _{BSVKH}	0.0	—	ns	
Boundary scan input data hold time	t _{BSXKH}	15.0	—	ns	
TCK fall to output data valid	t _{TCKHOV}	—	20.0	ns	
TCK fall to output high impedance	t _{TCKHOZ}	—	24.0	ns	
TMS, TDI data setup time	t _{TDIVKH}	0.0	—	ns	
TMS, TDI data hold time	t _{TDIXKH}	5.0	—	ns	
TCK fall to TDO data valid	t _{TDOHOV}	—	10.0	ns	
TCK fall to TDO high impedance	t _{TDOHOZ}	—	12.0	ns	
TRST assert time	t _{TRST}	100.0	—	ns	
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.					

Figure 29 shows the test clock input timing diagram



Figure 29. Test Clock Input Timing



3.1.2 Power-On Ramp Time

This section describes the AC electrical specification for the power-on ramp rate requirements for all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the power-on ramp time is required to avoid falsely triggering the ESD circuitry. Table 39 defines the power supply ramp time specification.

Table 39. Power Supply Ramp Rate

Parameter Min Ma				Max	Unit
Required ramp rate.		—	36000	V/s	
Notes:	1.	Ramp time is specified as a linear ramp from 10% to 90% of nominal voltage of the specific non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is th might falsely trigger the ESD circuitry.	voltage sup e most critic	oply. If the ra	amp is this range
	2. Required over the full recommended operating temperature range (see Table 3).				
	3. All supplies must be at their stable values within 50 ms.				
	4.	The GVDD pins can be held low on the application board at powerup. If GVDD is not held low on the board-level impedance-to-ground. If the impedance is hid	ow, then G∨ h (that is, in	DD will rise (DD will rise finite).	to a

3.1.3 Power Supply Guidelines

Use the following guidelines for power-up sequencing:

• Couple M3VDD with the VDD power rail using an extremely low impedance path.

theoretically, GVDD can rise up close to the VDD levels.

- Couple inputs PLL1_AVDD, PLL2_AVDD and PLL3_AVDD with the VDD power rail using an RC filter (see Figure 37).
- There is no dependency in power-on/power-off sequence between the GVDD1, GVDD2, NVDD, and QVDD power rails.
- Couple inputs M1VREF and M2VREF with the GVDD1 and GVDD2 power rails, respectively. They should rise at the same time as or after their respective power rail.
- There is no dependency between RapidIO supplies: SXCVDD1, SXCVDD2, SXPVDD1 and SXPVDD2 and other MSC8151 supplies in the power-on/power-off sequence
- Couple inputs SR1_PLL_AVDD and SR2_PLL_AVDD with SXCVDD1 and SXCVDD2 power rails, respectively, using an RC filter (see Figure 38).

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8151 device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- $R = 5 \ \Omega \pm 5\%$
- $C1 = 10 \,\mu\text{F} \pm 10\%$, 0603, X5R, with ESL $\leq 0.5 \,\text{nH}$, low ESL Surface Mount Capacitor.
- $C2 = 1.0 \ \mu\text{F} \pm 10\%$, 0402, X5R, with ESL $\leq 0.5 \ n\text{H}$, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.



Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.



Figure 38. SerDes PLL Supplies



ware Design Considerations

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

Rterm = Rim - Rbuf

where Rim = trace characteristic impedance

Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.



Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example



ware Design Considerations

DDR Memory Related Pins 3.5.1

This section discusses the various scenarios that can be used with either of the MSC8151 DDR ports.

The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin Note: names refer to Table 1.

3.5.1.1 **DDR Interface Is Not Used**

Signal Name	Pin Connection			
MDQ[0-63]	NC			
MDQS[7-0]	NC			
MDQS[7-0]	NC			
MA[15–0]	NC			
MCK[0-2]	NC			
MCK[0-2]	NC			
MCS[1-0]	NC			
MDM[7-0]	NC			
MBA[2-0]	NC			
MCAS	NC			
MCKE[1-0]	NC			
MODT[1-0]	NC			
MMDIC[1-0]	NC			
MRAS	NC			
MWE	NC			
MECC[7-0]	NC			
MDM8	NC			
MDQS8	NC			
MDQS8	NC			
MAPAR_OUT	NC			
MAPAR_IN	NC			
MVREF ³	NC			
GVDD1/GVDD2 ³	NC			
 For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the 				

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Clocks and General Configuration Registers chapters in the MSC8151 Reference Manual for details.

For MSC8151 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8151, connecting these 3. pins to GND increases device power consumption.

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ware Design Considerations

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Signal Name		Signal Name	Pin connection
MAPAR_OUT		-	NC
MAPAR_IN			NC
Notes:	 For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2. For MSC8151 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8151, connecting these pins to GND increases device power consumption. 		

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

TADIE 44. CONNECTIVITY OF DENAI RADIATO INTENACE REFATED FINS WHEN THE RADIATO INTENACE IS NOT USE	Table 44. Connectivity	v of Serial RapidIO Interface	Related Pins When the Ra	pidIO Interface Is Not Used
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Signal Name	Pin Connection	
SR_IMP_CAL_RX	NC	
SR_IMP_CAL_TX	NC	
SR[1-2]_REF_CLK	SXCVSS	
SR[1-2]_REF_CLK	SXCVSS	
SR[1-2]_RXD[3-0]	SXCVSS	
SR[1-2]_RXD[3-0]	SXCVSS	
SR[1-2]_TXD[3-0]	NC	
SR[1-2]_TXD[3-0]	NC	
SR[1-2]_PLL_AVDD	In use	
SR[1–2]_PLL_AGND	In use	
SXPVSS	In use	
SXCVSS	In use	
SXPVDD	In use	
SXCVDD	In use	
Note: All lanes in the HSSI SerDes should be powered down. Refer to the MSC8151 Reference Manual for details.		

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
SR[1-2]_REF_CLK	In use
SR[1-2]_REF_CLK	In use

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NOTES:

ALL DIMENSIONS IN MILLIMETERS. 1.

- A1

CORNER

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 2.

BOTTOM VIEW

- MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
- DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Φ

Ø 0.1 M A

3.94 3.21

- /5 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
- 6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
- 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y. 7.

Figure 40. MSC8151 Mechanical Information, 783-ball FC-PBGA Package

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SIDE VIEW