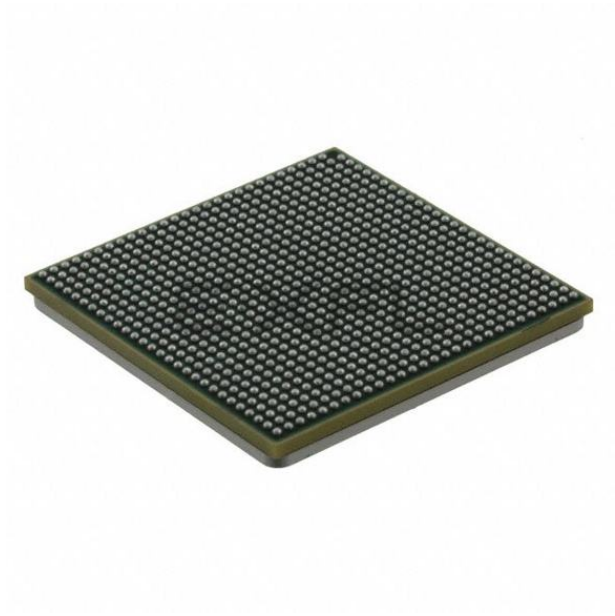

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Single Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8151tvt1000b

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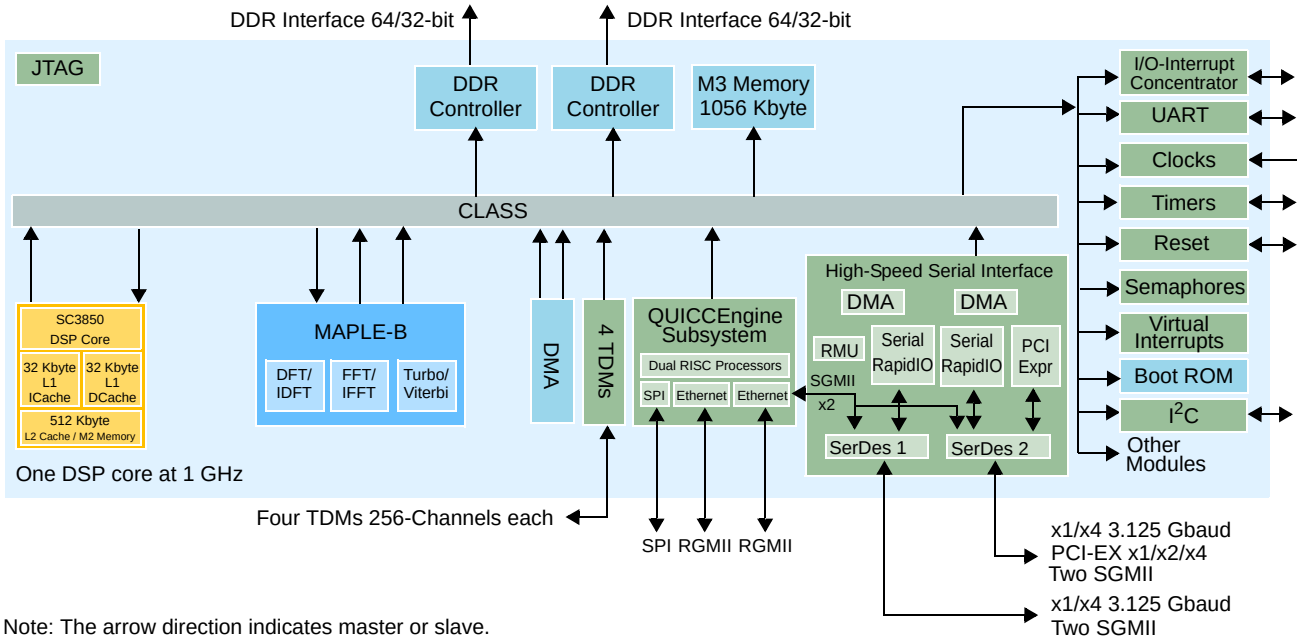


Figure 1. MSC8151 Block Diagram

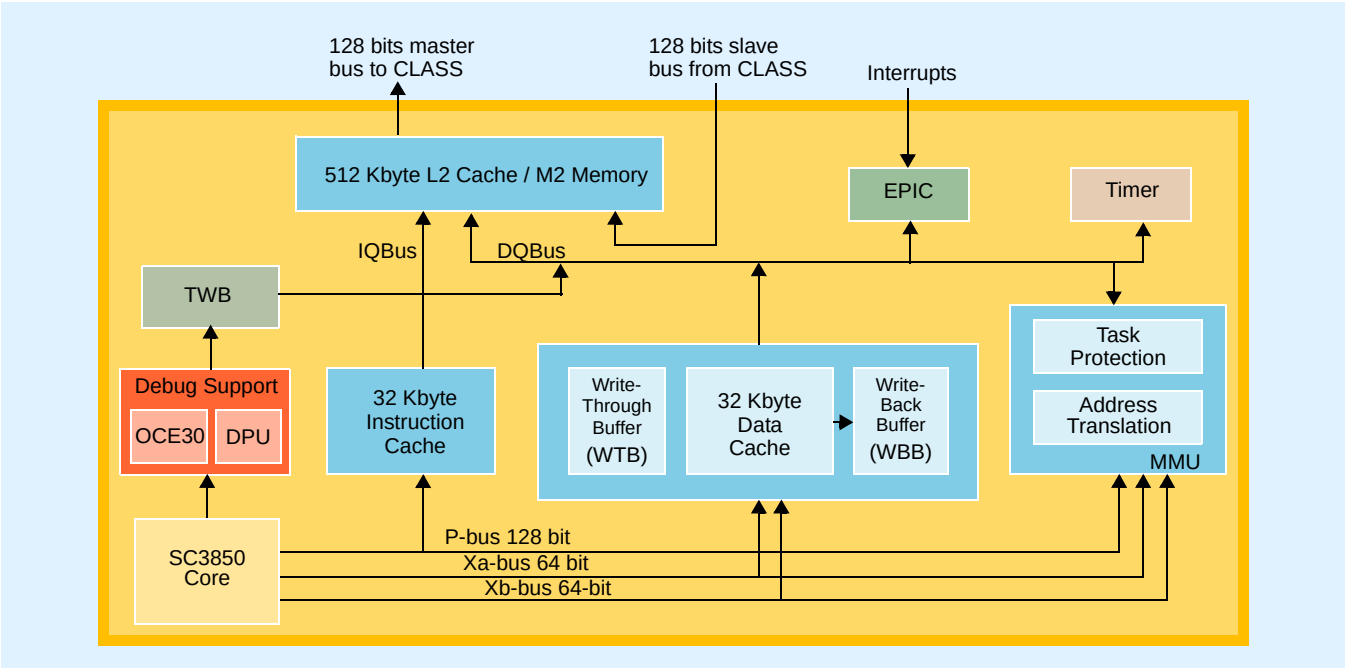


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

1 Pin Assignment

This section includes diagrams of the MSC8151 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

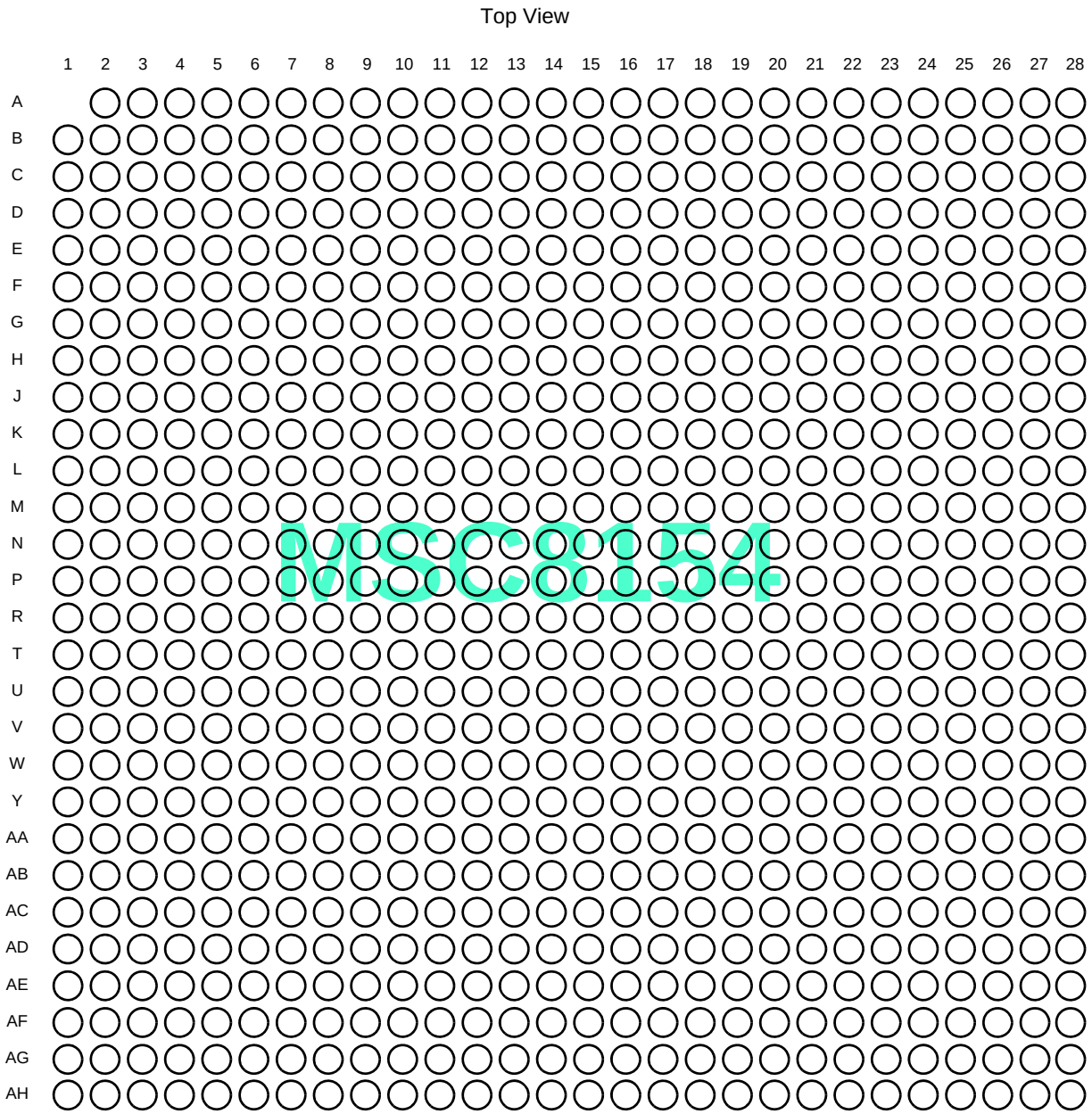


Figure 3. MSC8151 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	$\overline{\text{M2DQS7}}$	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND[9]	Ground	SXCVSS1
E26	SR1_PLL_AVDD[9]	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX[4]	O	SXPVDD1
F24	$\overline{\text{SR1\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	$\overline{\text{SR1\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD1
F28	SR1_RXD2/SG1_RX[4]	I	SXCVDD1
G1	$\overline{\text{M2DQS2}}$	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
G7	M2CKE0	O	GVDD2
G8	M2A11	O	GVDD2
G9	M2A7	O	GVDD2
G10	$\overline{\text{M2CK2}}$	O	GVDD2
G11	M2APAR_OUT	O	GVDD2
G12	M2ODT1	O	GVDD2
G13	$\overline{\text{M2APAR\_IN}}$	I	GVDD2
G14	M2DQ43	I/O	GVDD2
G15	M2DM5	O	GVDD2
G16	M2DQ44	I/O	GVDD2
G17	M2DQ40	I/O	GVDD2
G18	M2DQ59	I/O	GVDD2
G19	M2DM7	O	GVDD2
G20	M2DQ60	I/O	GVDD2
G21	Reserved	NC	—
G22	Reserved	NC	—
G23	SXPVSS1	Ground	N/A
G24	SXPVDD1	Power	N/A
G25	SR1_IMP_CAL_TX	I	SXCVDD1
G26	SXCVSS1	Ground	N/A
G27	Reserved	NC	—
G28	Reserved	NC	—
H1	GVDD2	Power	N/A
H2	VSS	Ground	N/A
H3	M2DQ18	I/O	GVDD2
H4	GVDD2	Power	N/A
H5	VSS	Ground	N/A
H6	M2DQ20	I/O	GVDD2
H7	GVDD2	Power	N/A
H8	VSS	Ground	N/A
H9	M2A15	O	GVDD2
H10	M2CK2	O	GVDD2
H11	M2MDIC0	I/O	GVDD2
H12	M2VREF	I	GVDD2
H13	M2MDIC1	I/O	GVDD2
H14	M2DQ46	I/O	GVDD2
H15	M2DQ47	I/O	GVDD2
H16	M2DQ45	I/O	GVDD2
H17	M2DQ41	I/O	GVDD2
H18	M2DQ62	I/O	GVDD2
H19	M2DQ63	I/O	GVDD2
H20	M2DQ61	I/O	GVDD2
H21	Reserved	NC	—
H22	Reserved	NC	—
H23	SR1_TXD3/SG2_TX[4]	O	SXPVDD1
H24	$\overline{\text{SR1\_TXD3}}$/$\overline{\text{SG2\_TX}}$[4]	O	SXPVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
R13	VSS	Ground	N/A
R14	VDD	Power	N/A
R15	VSS	Ground	N/A
R16	MVDD	Power	N/A
R17	VSS	Ground	N/A
R18	VDD	Power	N/A
R19	VSS	Ground	N/A
R20	VSS	Non-user	N/A
R21	SXPVSS2	Ground	N/A
R22	SXPVDD2	Power	N/A
R23	SR2_TXD1/PE_TXD1[4]	O	SXPVDD2
R24	$\overline{\text{SR2\_TXD1}}$/$\overline{\text{PE\_TXD1}}$[4]	O	SXPVDD2
R25	SXCVSS2	Ground	N/A
R26	SXCVDD2	Power	N/A
R27	$\overline{\text{SR2\_RXD1}}$/$\overline{\text{PE\_RXD1}}$[4]	I	SXCVDD2
R28	SR2_RXD1/PE_RXD1[4]	I	SXCVDD2
T1	VSS	Ground	N/A
T2	TCK	I	QVDD
T3	$\overline{\text{SRESET}}$[6,7]	I/O	QVDD
T4	TDI	I	QVDD
T5	VSS	Ground	N/A
T6	TDO	O	QVDD
T7	VSS	Ground	N/A
T8	VSS	Ground	N/A
T9	QVDD	Power	N/A
T10	VSS	Ground	N/A
T11	VDD	Power	N/A
T12	VSS	Ground	N/A
T13	M3VDD	Power	N/A
T14	VSS	Ground	N/A
T15	VDD	Power	N/A
T16	VSS	Ground	N/A
T17	MVDD	Power	N/A
T18	VSS	Ground	N/A
T19	VDD	Power	N/A
T20	VSS	Ground	N/A
T21	VSS	Non-user	N/A
T22	SR2_IMP_CAL_RX	I	SXCVDD2
T23	SXPVSS2	Ground	N/A
T24	SXPVDD2	Power	N/A
T25	SR2_REF_CLK	I	SXCVDD2
T26	$\overline{\text{SR2\_REF\_CLK}}$	I	SXCVDD2
T27	Reserved	NC	—
T28	Reserved	NC	—
U1	M1DQ8	I/O	GVDD1
U2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AE9	M1A8	O	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	O	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD[5,8]	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK[3]	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL[3]	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK[3]	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK[3]	I/O	NVDD
AE27	TDM2RSN/GE1_TD2[3]	I/O	NVDD
AE28	TDM2RDT/GE1_TD1[3]	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	O	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	O	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	O	GVDD1
AF8	M1CK0	O	GVDD1
AF9	$\overline{\text{M1CK0}}$	O	GVDD1
AF10	M1BA1	O	GVDD1
AF11	M1A1	O	GVDD1
AF12	$\overline{\text{M1WE}}$	O	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	O	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	O	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD[5,8]	I/O	NVDD
AF22	TDM0RSN/GE2_TD2[3]	I/O	NVDD
AF23	TDM0TDT/GE2_TD3[3]	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL[3]	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AH17	$\overline{\text{M1DQS6}}$	I/O	GVDD1
AH18	M1DQS6	I/O	GVDD1
AH19	M1DQ48	I/O	GVDD1
AH20	M1DQ49	I/O	GVDD1
AH21	VSS	Ground	N/A
AH22	TDM0RCK/GE2_RD2[3]	I/O	NVDD
AH23	TDM0RDT/GE2_RD3[3]	I/O	NVDD
AH24	TDM0TSN/GE2_RD0[3]	I/O	NVDD
AH25	TDM1RCK/GE2_RD1[3]	I/O	NVDD
AH26	TDM3TDT/GE1_RD3[3]	I/O	NVDD
AH27	TDM3TCK/GE1_RD2[3]	I	NVDD
AH28	VSS	Ground	N/A

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).
2. Signal function during power-on reset is determined by the RCW source type.
3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.
4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.
5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the *GPIO* chapter in the *MSC8151 Reference Manual*.
6. Open-drain signal.
7. Internal 20 KΩ pull-up resistor.
8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the *GPIO* chapter of the *MSC8151 Reference Manual* for configuration details.
9. Connect to power supply via external filter. See **Section 3.2**, *PLL Power Supply Design Considerations* for details.
10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.

2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.5 V.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	0.49 × V_{DDDDR}	0.51 × V_{DDDDR}	V	2,3,4
Input high voltage	V_{IH}	MV_{REF} + 0.100	V_{DDDDR}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to 0.5 × V_{DDDDR}, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 250 μA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, 0 V ≤ V_{OUT} ≤ V_{DDDDR}.

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V for DDR2 memory or V_{DDDDR} = 1.5 V for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Max	Unit
I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF
Delta I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF

Note: Guaranteed by FAB process and micro-construction.

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF}.

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn} • DDR2 SDRAM • DDR3 SDRAM	I_{MVREFn}	—	 300 250	 µA µA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8151 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, "HSSI AC Timing Specifications."

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{\text{SR[1–2]\_TX}}$) or a receiver input (SR[1–2]_RX and $\overline{\text{SR[1–2]\_RX}}$). Each signal swings between A volts and B volts where A > B.

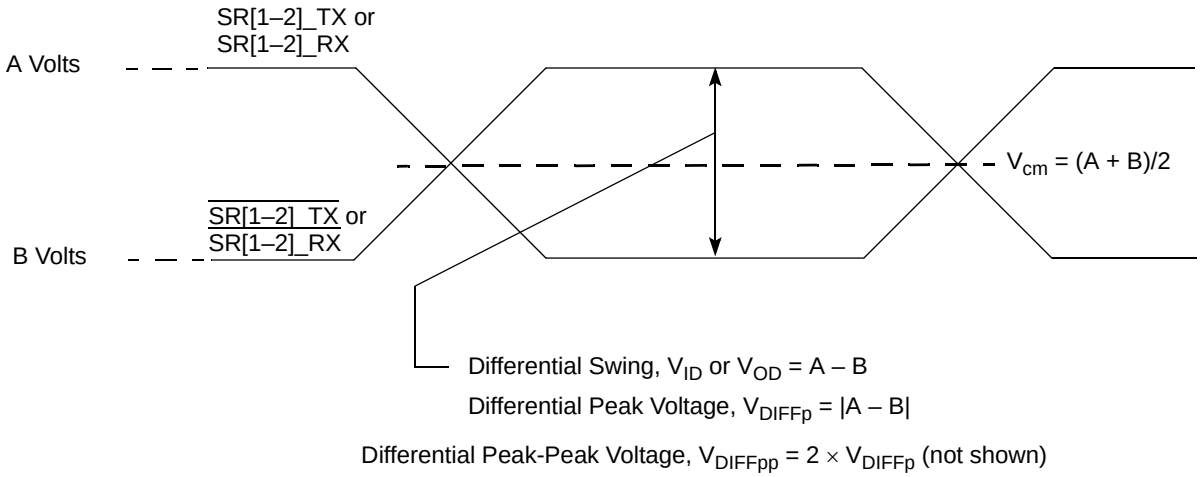


Figure 4. Differential Voltage Definitions for Transmitter or Receiver

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	1
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	2
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	3
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	4

Notes:
1. $V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
3. Tx DC differential mode low impedance
4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	5

Notes:
1. $V_{RX-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	—
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	—

Note: Voltage relative to COMMON of either signal comprising a differential pair.

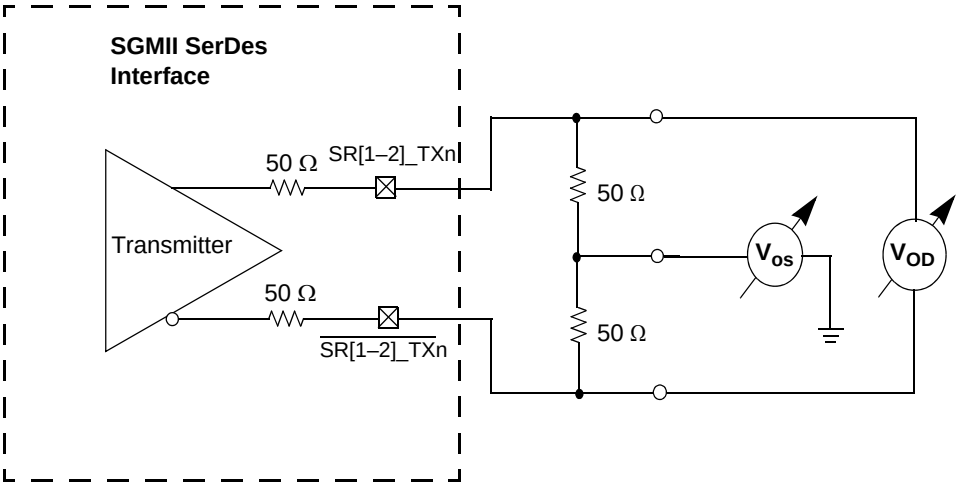


Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16. SGMII DC Receiver Electrical Characteristics[5]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—		N/A		—	1
Input differential voltage	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		175	—			
Loss of signal threshold	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	VLOS	30	—	100	mV	3, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	W	—

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.
4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.
5. The supply voltage is 1.0 V.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8151 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8151.
6. At recommended operating conditions with V_{DDDDR} (1.5 V or 1,8 V) ± 5%.

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

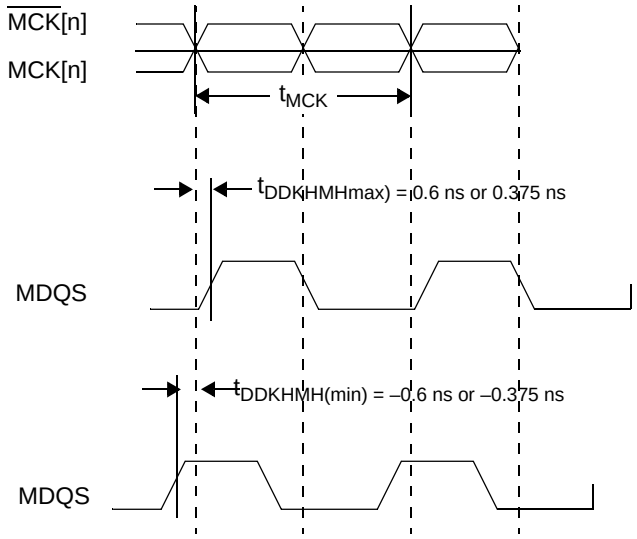


Figure 12. MCK to MDQS Timing

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) or at the receiver inputs (SR[1–2]_RX[n] and $\overline{\text{SR[1–2]\_RX}}$[n]) as depicted in Figure 19, respectively.

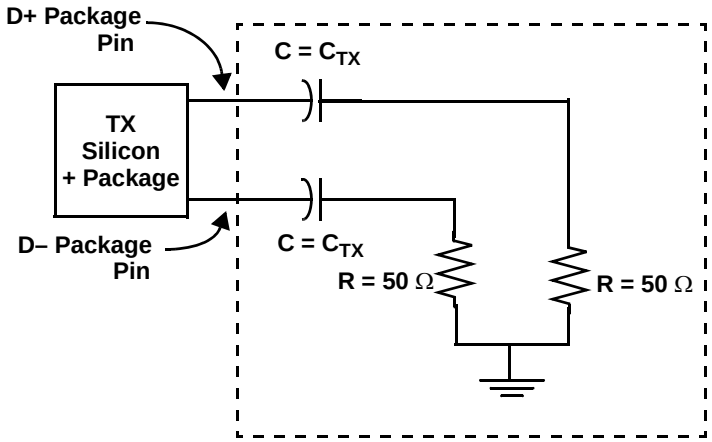


Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1

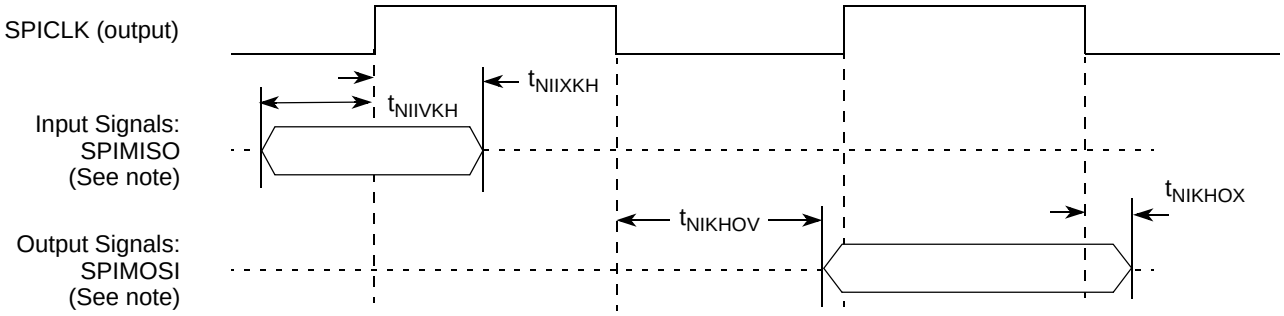
Notes: 1. See Figure 18 for single frequency sinusoidal jitter limits
2. Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes: 1. Measured at receiver.
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
3. Each UI is 800 ps ± 100 ppm.



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

Figure 30 shows the boundary scan (JTAG) timing diagram.

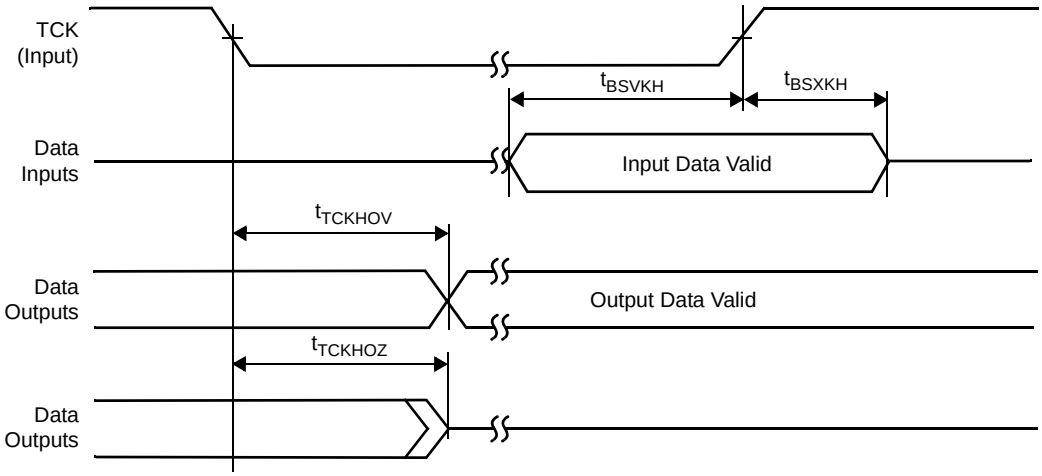


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

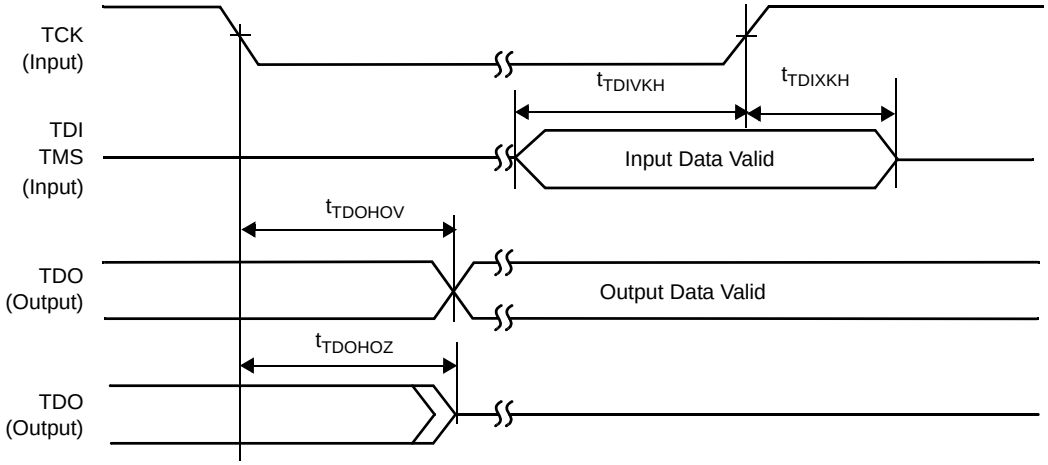


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 32. $\overline{\text{TRST}}$ Timing

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC

Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8151 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8151, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1–2]\_REF\_CLK}}$	SXCVSS
SR[1–2]_REF_CLK	SXCVSS
SR[1–2]_RXD[3–0]	SXCVSS
$\overline{\text{SR[1–2]\_RXD[3–0]}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD[3–0]}}$	NC
SR[1–2]_TXD[3–0]	NC
SR[1–2]_PLL_AVDD	In use
SR[1–2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use

Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8151 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1–2]\_REF\_CLK}}$	In use
SR[1–2]_REF_CLK	In use

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***TCLK	GND
TDMT***n***DAT	GND
TDM***n***TSYN	GND
V_{DDIO}	2.5 V

Notes: 1. ***n*** = {0, 1, 2,3}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See *TDM* chapter in the ***MSC8151 Reference Manual*** for details.

3.5.5 Miscellaneous Pins

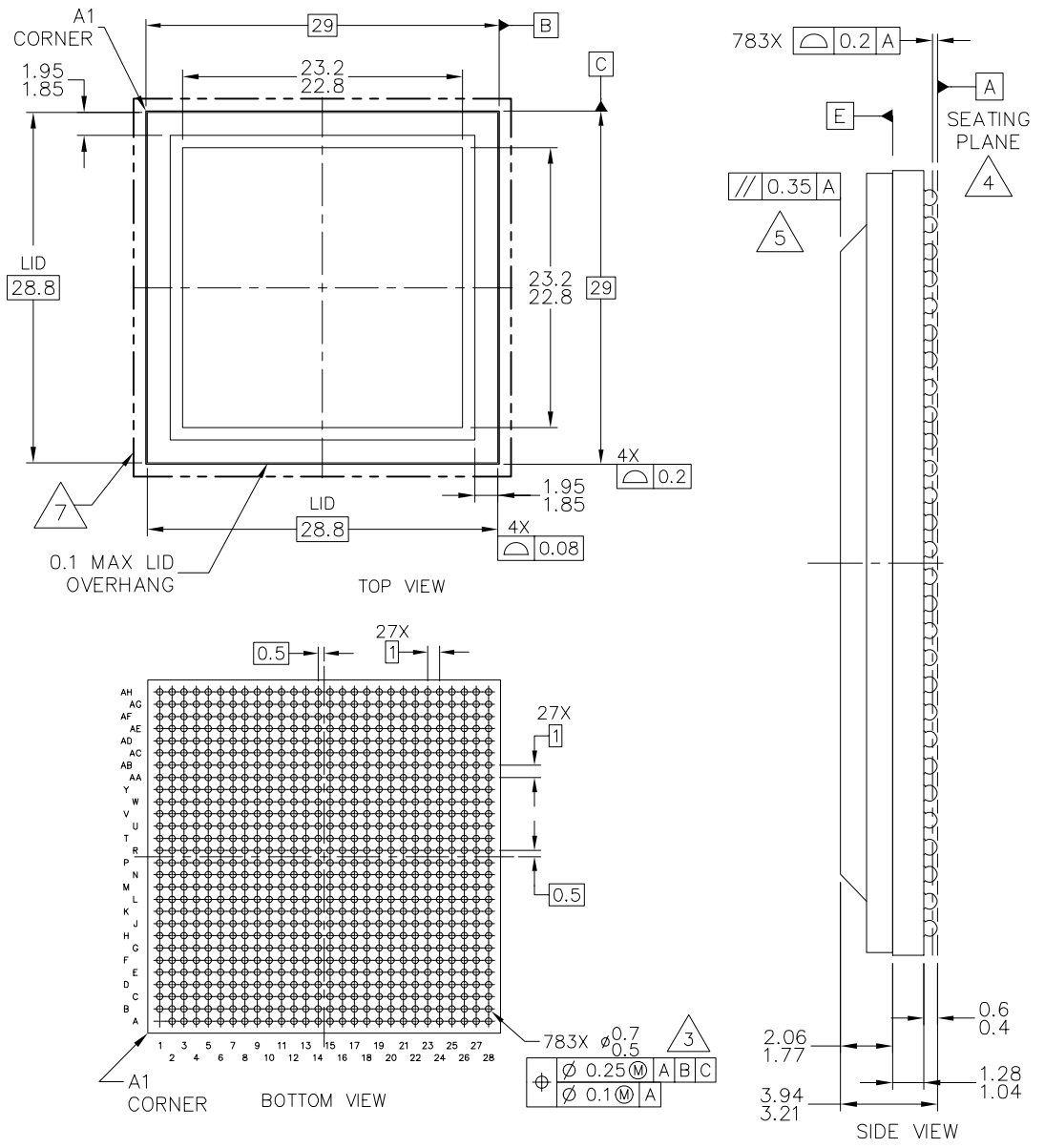
Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[15–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 3.1** for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
V_{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8151 Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 40. MSC8151 Mechanical Information, 783-ball FC-PBGA Package