### NXP USA Inc. - MSC8151TVT1000B Datasheet





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#### Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

#### Details

Product Status	Obsolete
Туре	SC3850 Single Core
Interface	Ethernet, I <sup>2</sup> C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
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Figure 1. MSC8151 Block Diagram



Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

# 1 Pin Assignment

This section includes diagrams of the MSC8151 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

## 1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

#### Top View



Figure 3. MSC8151 FC-PBGA Package, Top View



E17         M2D056         UO         GVDD2           E18         M2D057         UO         GVDD2           E19         M2D057         UO         GVDD2           E20         Reserved         NC            E21         Reserved         NC            E23         SRPVD01         Power         NA           E24         Reserved         NC            E23         SRPVD01         Power         NA           E24         SR1.PLL_AOD <sup>9</sup> Ground         NA           E25         SR1.PLL_ADD <sup>9</sup> Power         NA           E27         SXCVDD1         Power         NA           E28         SXCVDD1         Power         NA           F1         VSS         Ground         NA           F2         GVD02         Power         NA           F3         M2D16         UO         GVD2           F4         VSS         Ground         NA           F5         GVD2         Power         NA           F8         GVD2         Power         NA           F8         GVD2         Power         NA	Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name
E16         M2DOS7         I/O         GVDD2           E19         M2DOS7         I/O         GVDD2           E20         Reserved         NC            E21         Reserved         NC            E22         Reserved         NC            E23         SXPVDD1         Power         N/A           E24         SXPVSS1         Ground         SXCVS1           E24         SXPVDD1         Power         N/A           E25         SR1_PLL_AND9         Power         N/A           E26         SR1_PLL_AND9         Power         N/A           E27         S/CVS1         Ground         N/A           E28         S/CVDD1         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2DO16         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2DO17         I/O         GVDD2           F7         VSS         Ground         N/A	E17	M2DQ56	I/O	GVDD2
E19         M2DOS7         I/O         GVDD2           E20         Reserved         NC            E21         Reserved         NC            E22         Reserved         NC            E23         SXPVDD1         Power         NA           E24         SXPVSS1         Ground         NXA           E25         SR1, PLL, AND <sup>9</sup> Ground         SXCVSS1           E28         SK1, PLL, AND <sup>9</sup> Power         NA           E28         SXCVDD1         Power         NA           F1         VSS         Ground         NA           F2         GVDD2         Power         NA           F3         M2D016         U/O         GVDD2           F4         VSS         Ground         NA           F5         GVD2         Power         NA           F6         M2D017         U/O         GVDD2           F7         VSS         Ground         NA           F8         GVD2         Power         NA           F10         VSS         Ground         NA           F14         GVD2         Power         NA	E18	M2DQ57	I/O	GVDD2
E20         Reserved         NC            E21         Reserved         NC            E23         SXPVDD1         NA            E23         SXPVDD1         Power         N/A           E24         SXPVDS1         Ground         N/A           E25         SR1_PLL_ANDP <sup>9</sup> Ground         SXCVSS1           E26         SR1_PLL_ANDP <sup>9</sup> Ground         N/A           E27         SXCVSS1         Ground         N/A           E28         SXCVD01         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2DQ16         I/O         GVDD2           F4         VSS         Ground         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         M2DQ17         I/O         GVD2           F10         VSS         Ground         N/A           F11         GVD2         Power         N/A           F11         GVD2         Power         N/A	E19	M2DQS7	I/O	GVDD2
E21         Reserved         NC            E22         Reserved         NC            E23         SXPVDD1         Power         N/A           E24         SXPVSS1         Ground         SXCVSS1           E26         SR1_PLL_ANDP <sup>9</sup> Ground         SXCVSS1           E26         SR1_PL_ANDP <sup>9</sup> Ground         N/A           E28         SXCVDD1         Power         N/A           E27         SXCVSS1         Ground         N/A           E28         SXCVDD1         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2O16         I/O         GVD2           F4         VSS         Ground         N/A           F5         GVD2         Power         N/A           F6         M2O17         I/O         GVD2           F7         VSS         Ground         N/A           F8         GVD2         Power         N/A           F10         VSS         Ground         N/A           F11         GVD2         Power         N/A<	E20	Reserved	NC	_
E22         Resved         NC         —           E23         SXPVDD1         Power         N/A           E24         SXPVD1         Ground         N/A           E25         SR1_PLL_AGND <sup>9</sup> Ground         SXCVSS1           E26         SR1_PLL_AGND <sup>9</sup> Power         SXCVSD1           E27         SXCVSS1         Ground         N/A           E28         SXCVDD1         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2D016         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         Ground         N/A           F11         GVDD2         Power	E21	Reserved	NC	_
E23         SXPVDD1         Power         N/A           E24         SXPVDS1         Ground         SXCVS51           E26         SR1_PLL_ANDD <sup>9</sup> Power         SXCVD11           E27         SXCVS51         Ground         N/A           E28         SXCVD01         Power         N/A           E28         SXCVD01         Power         N/A           E28         SXCVD01         Power         N/A           F2         GVD02         Power         N/A           F3         M2D016         Ground         N/A           F5         GVD02         Power         N/A           F6         M2D017         VO         GVD02         Power         N/A           F6         M2D017         VS         Ground         N/A         Power         N/A           F7         VSS         Ground         N/A         Power         N/A           F10         VSS         Ground         N/A         Power         N/A           F11         GVD02         Power         N/A         Power         N/A           F11         GVD02         Power         N/A         Power         N/A <td< td=""><td>E22</td><td>Reserved</td><td>NC</td><td>_</td></td<>	E22	Reserved	NC	_
E24         SXPVSS1         Ground         N/A           E25         SR1_PLL_AGND <sup>9</sup> Ground         SXCVSS1           E26         SR1_PLL_AGND <sup>9</sup> Power         SXCVSD1           E27         SXCVDS1         Ground         N/A           E28         SXCVDD1         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         MzD016         U/O         GVDD2           F4         VSS         Ground         N/A           F6         GVD02         Power         N/A           F6         MzD017         U/O         GVD02           F7         VSS         Ground         N/A           F8         GVD02         Power         N/A           F9         MzBA2         O         GVD02           F10         VSS         Ground         N/A           F11         GVD02         Power         N/A           F13         VSS         Ground         N/A           F14         GVD02         Power         N/A           F16         VSS         Ground         N/A	E23	SXPVDD1	Power	N/A
E25         SR1_PLL_AGND <sup>9</sup> Ground         SXCVS31           E26         SR1_PLL_AVDD <sup>9</sup> Power         SXCVD01           E27         SXCVSS1         Ground         N/A           E28         SXCVD01         Power         N/A           F1         VSS         Ground         N/A           F2         GVD02         Power         N/A           F3         M2D016         U/O         GVD02           F4         VSS         Ground         N/A           F6         M2D017         U/O         GVD02           F7         VSS         Ground         N/A           F8         GVD02         Power         N/A           F8         GVD02         Power         N/A           F9         M2BA2         O         GVD02           F10         VSS         Ground         N/A           F11         GVD02         Power         N/A           F13         M2A4         O         GVD02           F14         GVD02         Power         N/A           F15         M2D043         I/O         GVD02           F16         VSS         Ground         N/A	E24	SXPVSS1	Ground	N/A
E26         SR1_PLL_AVDD <sup>9</sup> Power         SXCVDD1           E27         SXCVS51         Ground         N/A           E28         SXCVD1         Power         N/A           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2D016         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVD2         Power         N/A           F6         M2D017         I/O         GVD2           F7         VSS         Ground         N/A           F8         GVD2         Power         N/A           F8         GVD2         Power         N/A           F10         VSS         Ground         N/A           F11         GVD2         Power         N/A           F12         M2A4         O         GVD2           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F15         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A	E25	SR1_PLL_AGND <sup>9</sup>	Ground	SXCVSS1
E27         SXCVSS1         Ground         N/A           E28         SXCVDD1         Power         NA           F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2D016         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2D017         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F8         GVD2         Power         N/A           F9         M2BA2         O         GVD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVD2           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F14         GVD2         Power         N/A           F14         M2DQ57         Ground         N/A           F17 <td>E26</td> <td>SR1_PLL_AVDD<sup>9</sup></td> <td>Power</td> <td>SXCVDD1</td>	E26	SR1_PLL_AVDD <sup>9</sup>	Power	SXCVDD1
E28         SXCVDD1         Power         N/A           F1         VSS         Ground         NA           F2         GVDD2         Power         N/A           F3         M2Dq16         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         NA           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         NA           F8         GVDD2         Power         N/A           F8         GVDD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F11         GVD2         Power         N/A           F11         GVD2         Power         N/A           F12         M2A4         O         GVD2           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F18         M2DQ57         I/O         GVD2           F14	E27	SXCVSS1	Ground	N/A
F1         VSS         Ground         N/A           F2         GVDD2         Power         N/A           F3         M2DQ16         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F8         GVD2         Power         N/A           F9         M2BA2         O         GVD2           F10         VSS         Ground         N/A           F11         GVD2         Power         N/A           F12         M2A4         O         GVD2           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F15         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A           F17         GVD2         Power         N/A           F14         GVD2         Power         N/A           F16	E28	SXCVDD1	Power	N/A
F2         GVDD2         Power         N/A           F3         M2DQ16         I/O         GVDD2           F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F8         GVDD2         O         GVD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F11         GVD2         Power         N/A           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F15         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A           F17         GVD02         Power         N/A           F17         GVD02         Power         N/A           F17         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A           F17 <td>F1</td> <td>VSS</td> <td>Ground</td> <td>N/A</td>	F1	VSS	Ground	N/A
F3         M2DQ16         I/O         GVDD2           F4         VSS         Ground         NA           F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F14         GVDD2         Power         N/A           F14         GVDD2         Power         N/A           F14         GVD2         Power         N/A           F14         GVD2         Power         N/A           F14         GVD2         Power         N/A           F15         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A           F17         GVD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F20	F2	GVDD2	Power	N/A
F4         VSS         Ground         N/A           F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Ground         N/A           F8         GVDD2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         O         GVDD2           F11         GVDD2         O         GVDD2           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2D42         I/O         GVD2           F16         VSS         Ground         N/A           F17         GVD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F19         M2DQSG1TX <sup>4</sup> O         SXPVD1           F21         SXPVDD1         Power         N/A           F2	F3	M2DQ16	I/O	GVDD2
F5         GVDD2         Power         N/A           F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVS1         Ground         N/A <t< td=""><td>F4</td><td>VSS</td><td>Ground</td><td>N/A</td></t<>	F4	VSS	Ground	N/A
F6         M2DQ17         I/O         GVDD2           F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F19         M2DQ57         I/O         GVD2           F20         GVD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1      <	F5	GVDD2	Power	N/A
F7         VSS         Ground         N/A           F8         GVDD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         Ground         N/A           F12         M2A4         O         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2D42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F17         M2DQ42         I/O         GVD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F20         GVD2         Power         N/A           F21         SXPVS1         Ground         N/A           F22         SXPVS1         O         SX	F6	M2DQ17	I/O	GVDD2
F8         GVD2         Power         N/A           F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVD2         Power         N/A           F11         GVD2         O         GVDD2           F11         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVD2         Power         N/A           F18         M2DQ58         I/O         GVD2           F19         M2DQS7         I/O         GVD2           F20         GVDD2         Power         N/A           F21         SXPVD1         Power         N/A           F22         SXPVS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F24         SR1_TXD2/SG1_RX <sup>4</sup> I         SXCVD1           F25         SXCVD1         Power         N/A	F7	VSS	Ground	N/A
F9         M2BA2         O         GVDD2           F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> I         SXCVD1           F25         SXCVD1         Power         N/A           F26         SXCVD51_TX <sup>4</sup> I         SX	F8	GVDD2	Power	N/A
F10         VSS         Ground         N/A           F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ42         I/O         GVDD2           F18         M2DQ58         I/O         GVD2           F19         M2DQS7         I/O         GVD2           F20         GVD2         Power         N/A           F21         SXPVDD1         Power         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F25         SXCVD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F28         SR1_RXD2/SG1_RX <sup>4</sup> I	F9	M2BA2	0	GVDD2
F11         GVDD2         Power         N/A           F12         M2A4         O         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Ground         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVD1         Power         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F25         SXCVD1         Power         N/A           F26         SXCVD1         Power         N/A           F26         SXCVD1         Ground         N/A           F26         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQS2         I/O	F10	VSS	Ground	N/A
F12         M2A4         0         GVDD2           F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVD51_TX <sup>4</sup> O         SXPVDD1           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SRVDS1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVD1         Power         N/A           F26         SXCVD1         Power         N/A           F25         SXCVD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQ32         I/O <td>F11</td> <td>GVDD2</td> <td>Power</td> <td>N/A</td>	F11	GVDD2	Power	N/A
F13         VSS         Ground         N/A           F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Ground         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F25         SXCVD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/S	F12	M2A4	0	GVDD2
F14         GVDD2         Power         N/A           F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVD1         Power         N/A           F23         SR1_TXD/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVD1         Power         N/A           F26         SXCVD1         Power         N/A           F26         SXCVD1         Power         N/A           F26         SXCVD1         Power         N/A           F27         SR1_RXD/SG1_RX <sup>4</sup> I         SXCVD1           F28         SR1_RXD/SG1_RX <sup>4</sup> I         SXCVD1           F28         SR1_RXD/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQS2	F13	VSS	Ground	N/A
F15         M2DQ42         I/O         GVDD2           F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SRT_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQS2         I/O         GVD2           G2         M2DQS2         I/O         GVD2           G3         M2D	F14	GVDD2	Power	N/A
F16         VSS         Ground         N/A           F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22	F15	M2DQ42	I/O	GVDD2
F17         GVDD2         Power         N/A           F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVD1           F25         SXCVD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DQ2         I/O         GVDD2           G5         M2DQ2         I/O         GVDD2           G6         M2DQ2         I/O         GVDD2	F16	VSS	Ground	N/A
F18         M2DQ58         I/O         GVDD2           F19         M2DQS7         I/O         GVDD2           F20         GVDD2         Power         N/A           F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F26         SXCVDD1         Power         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F17	GVDD2	Power	N/A
F19M2DQS7I/OGVDD2F20GVDD2PowerN/AF21SXPVDD1PowerN/AF22SXPVSS1GroundN/AF23SR1_TXD2/SG1_TX4OSXPVDD1F24SR1_TXD2/SG1_TX4OSXPVDD1F25SXCVD1PowerN/AF26SXCVSS1GroundN/AF27SR1_RXD2/SG1_RX4ISXCVD1F28SR1_RXD2/SG1_RX4ISXCVD1G1M2DQS2I/OGVD2G3M2DQ19I/OGVD2G4M2DM2OGVD2G6M2DQ22I/OGVD2	F18	M2DQ58	I/O	GVDD2
F20GVDD2PowerN/AF21SXPVDD1PowerN/AF22SXPVSS1GroundN/AF23SR1_TXD2/SG1_TX4OSXPVDD1F24SR1_TXD2/SG1_TX4OSXPVDD1F25SXCVDD1PowerN/AF26SXCVSS1GroundN/AF27SR1_RXD2/SG1_RX4ISXCVDD1F28SR1_RXD2/SG1_RX4ISXCVDD1G1M2DQS2I/OGVDD2G3M2DQ19I/OGVDD2G4M2DQ2I/OGVDD2G6M2DQ22I/OGVDD2	F19	M2DQS7	I/O	GVDD2
F21         SXPVDD1         Power         N/A           F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F20	GVDD2	Power	N/A
F22         SXPVSS1         Ground         N/A           F23         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVD2           G6         M2DQ22         I/O         GVD2	F21	SXPVDD1	Power	N/A
F23SR1_TXD2/SG1_TX4OSXPVDD1F24SR1_TXD2/SG1_TX4OSXPVDD1F25SXCVDD1PowerN/AF26SXCVSS1GroundN/AF27SR1_RXD2/SG1_RX4ISXCVDD1F28SR1_RXD2/SG1_RX4ISXCVDD1G1M2DQS2I/OGVDD2G2M2DQS2I/OGVDD2G3M2DQ19I/OGVDD2G4M2DM2OGVDD2G5M2DQ21I/OGVDD2G6M2DQ22I/OGVDD2	F22	SXPVSS1	Ground	N/A
F24         SR1_TXD2/SG1_TX <sup>4</sup> O         SXPVDD1           F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DQ21         I/O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F23	SR1_TXD2/SG1_TX <sup>4</sup>	0	SXPVDD1
F25         SXCVDD1         Power         N/A           F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DQ21         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F24	SR1_TXD2/SG1_TX <sup>4</sup>	0	SXPVDD1
F26         SXCVSS1         Ground         N/A           F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DQ2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F25	SXCVDD1	Power	N/A
F27         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DQ21         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F26	SXCVSS1	Ground	N/A
F28         SR1_RXD2/SG1_RX <sup>4</sup> I         SXCVDD1           G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F27	SR1_RXD2/SG1_RX <sup>4</sup>	I	SXCVDD1
G1         M2DQS2         I/O         GVDD2           G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	F28	SR1_RXD2/SG1_RX <sup>4</sup>	I	SXCVDD1
G2         M2DQS2         I/O         GVDD2           G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	G1	M2DQS2	I/O	GVDD2
G3         M2DQ19         I/O         GVDD2           G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	G2	M2DQS2	I/O	GVDD2
G4         M2DM2         O         GVDD2           G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	G3	M2DQ19	I/O	GVDD2
G5         M2DQ21         I/O         GVDD2           G6         M2DQ22         I/O         GVDD2	G4	M2DM2	0	GVDD2
G6 M2DQ22 I/O GVDD2	G5	M2DQ21	I/O	GVDD2
	G6	M2DQ22	I/O	GVDD2



Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name
G7	M2CKE0	0	GVDD2
G8	M2A11	0	GVDD2
G9	M2A7	0	GVDD2
G10	M2CK2	0	GVDD2
G11	M2APAR_OUT	0	GVDD2
G12	M2ODT1	0	GVDD2
G13	M2APAR_IN	I	GVDD2
G14	M2DQ43	I/O	GVDD2
G15	M2DM5	0	GVDD2
G16	M2DQ44	I/O	GVDD2
G17	M2DQ40	I/O	GVDD2
G18	M2DQ59	I/O	GVDD2
G19	M2DM7	0	GVDD2
G20	M2DQ60	I/O	GVDD2
G21	Reserved	NC	—
G22	Reserved	NC	—
G23	SXPVSS1	Ground	N/A
G24	SXPVDD1	Power	N/A
G25	SR1_IMP_CAL_TX	I	SXCVDD1
G26	SXCVSS1	Ground	N/A
G27	Reserved	NC	_
G28	Reserved	NC	_
H1	GVDD2	Power	N/A
H2	VSS	Ground	N/A
H3	M2DQ18	I/O	GVDD2
H4	GVDD2	Power	N/A
H5	VSS	Ground	N/A
H6	M2DQ20	I/O	GVDD2
H7	GVDD2	Power	N/A
H8	VSS	Ground	N/A
H9	M2A15	0	GVDD2
H10	M2CK2	0	GVDD2
H11	M2MDIC0	I/O	GVDD2
H12	M2VREF	I	GVDD2
H13	M2MDIC1	I/O	GVDD2
H14	M2DQ46	I/O	GVDD2
H15	M2DQ47	I/O	GVDD2
H16	M2DQ45	I/O	GVDD2
H17	M2DQ41	I/O	GVDD2
H18	M2DQ62	I/O	GVDD2
H19	M2DQ63	I/O	GVDD2
H20	M2DQ61	I/O	GVDD2
H21	Reserved	NC	_
H22	Reserved	NC	_
H23	SR1_TXD3/SG2_TX <sup>4</sup>	0	SXPVDD1
H24	SR1_TXD3/SG2_TX <sup>4</sup>	0	SXPVDD1



R13         VSS         Ground         N/A           R14         VDD         Power         N/A           R15         VSS         Ground         N/A           R16         MVDD         Power         N/A           R16         MVDD         Power         N/A           R17         VSS         Ground         N/A           R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R20         VSS         Ground         N/A           R21         SXPVDS2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/FE_TXD14         O         SXPVDD2           R24         SR2_TXD1/FE_TXD14         O         SXPVDD2           R25         SXCVSS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/FE_RXD14         1         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> V/O	Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name
R14         VDD         Power         N/A           R15         VSS         Ground         N/A           R16         MVDD         Power         N/A           R17         VSS         Ground         N/A           R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R19         VSS         Ground         N/A           R20         VSS         Ground         N/A           R21         SXPVSS2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R24         SR2_XD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVDD2         Power         N/A           R26         SXCVDD2         Power         N/A           R26         SR2_RD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TD         I         QVD	R13	VSS	Ground	N/A
R15         VSS         Ground         N/A           R16         MVDD         Power         N/A           R17         VSS         Ground         N/A           R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R20         VSS         Non-user         N/A           R21         SXPVS2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD14         O         SXPVDD2           R24         SR2_TXD1/PE_TXD14         O         SXPVDD2           R25         SXCVSD2         Ground         N/A           R26         SX2CVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD14         I         SXCVDD2           R28         SR2_RXD1/PE_RXD14         I         QVDD           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         Q         QDD	R14	VDD	Power	N/A
R16         MVDD         Power         N/A           R17         VSS         Ground         N/A           R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R20         VSS         Non-user         N/A           R21         SXPVS52         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>8,7</sup> I/O         QVDD           T4         TD         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O	R15	VSS	Ground	N/A
R17         VSS         Ground         N/A           R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R20         VSS         Non-user         N/A           R21         SXPVDS2         Ground         N/A           R21         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVD2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>N,7</sup> I/O         QVD           T6         TOO         O         QVDD           T6         VSS         Ground         N/A           T18         VSS         Ground         N/A           T14         VDD         Power <td>R16</td> <td>MVDD</td> <td>Power</td> <td>N/A</td>	R16	MVDD	Power	N/A
R18         VDD         Power         N/A           R19         VSS         Ground         N/A           R20         VSS         Non-user         N/A           R21         SXPVSS2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVD2           R25         SXCVSS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>0,7</sup> I/O         QVDD           T4         TDI         I         QVDD         TA           T5         VSS         Ground         N/A           T6         TOO         O         QVDD           T7         VSS         Ground         N/A           T6         TOO         Q         QVD         Power         N/A           T10	R17	VSS	Ground	N/A
R19         VSS         Ground         N/A           R20         VSS         Non-user         N/A           R21         SXPVDD2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVD2           R25         SXCVSS2         Ground         N/A           R26         SXCVD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVD2           T1         VSS         Ground         N/A           T2         TCK         I         QVD           T4         TDI         I         QVD           T6         VSS         Ground         N/A           T7         VSS         Ground         N/A           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T11         VDD         Power         <	R18	VDD	Power	N/A
R20         VS         Nn-user         N/A           R21         SXPVSS2         Ground         NA           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVSS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_TXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T114         VSS         Ground	R19	VSS	Ground	N/A
R21         SXPVSS2         Ground         N/A           R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVSS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_TXD1 <sup>4</sup> I         SXCVDD2           R27         SR2_RXD1/PE_TXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_TXD1 <sup>4</sup> I         QVDD           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SREST <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VSS         Ground         N/A           T12         VSS         Ground	R20	VSS	Non-user	N/A
R22         SXPVDD2         Power         N/A           R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SRPVDD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SRPVDD2           R26         SXCVDD2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T13         M3VDD <td>R21</td> <td>SXPVSS2</td> <td>Ground</td> <td>N/A</td>	R21	SXPVSS2	Ground	N/A
R23         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVSS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T14         VDD         Power         N/A           T14         VSS         Ground <td< td=""><td>R22</td><td>SXPVDD2</td><td>Power</td><td>N/A</td></td<>	R22	SXPVDD2	Power	N/A
R24         SR2_TXD1/PE_TXD1 <sup>4</sup> O         SXPVDD2           R25         SXCVSS2         Ground         NA           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         NA           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A <td>R23</td> <td>SR2_TXD1/PE_TXD1<sup>4</sup></td> <td>0</td> <td>SXPVDD2</td>	R23	SR2_TXD1/PE_TXD1 <sup>4</sup>	0	SXPVDD2
R25         SXCVS2         Ground         N/A           R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T11         VDD         Power         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A	R24	SR2_TXD1/PE_TXD1 <sup>4</sup>	0	SXPVDD2
R26         SXCVDD2         Power         N/A           R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T8         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T13         M3VDD         Power         N/A           T11         VSS         Ground         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A	R25	SXCVSS2	Ground	N/A
R27         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T4         TDI         I         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16	R26	SXCVDD2	Power	N/A
R28         SR2_RXD1/PE_RXD1 <sup>4</sup> I         SXCVDD2           T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18	R27	SR2_RXD1/PE_RXD1 <sup>4</sup>	I	SXCVDD2
T1         VSS         Ground         N/A           T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T18         VSS         Ground         N/A           T18         VSS </td <td>R28</td> <td>SR2_RXD1/PE_RXD1<sup>4</sup></td> <td>I</td> <td>SXCVDD2</td>	R28	SR2_RXD1/PE_RXD1 <sup>4</sup>	I	SXCVDD2
T2         TCK         I         QVDD           T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18         VSS	T1	VSS	Ground	N/A
T3         SRESET <sup>6,7</sup> I/O         QVDD           T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18         VSS         Ground         N/A           T20         VSS         Ground         N/A           T21         <	T2	ТСК		QVDD
T4         TDI         I         QVDD           T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18         VSS         Ground         N/A           T19         VDD         Power         N/A           T20         VSS         Ground         N/A           T21         VSS         Ground         N/A           T21         VSS         Ground         N/A           T21         VSS<	Т3	SRESET <sup>6,7</sup>	I/O	QVDD
T5         VSS         Ground         N/A           T6         TDO         O         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T16         VSS         Ground         N/A           T18         VSS         Ground         N/A           T20         VSS         Ground         N/A           T21         VSS         Ground         N/A           T22         SR2_IMP_CAL_RX         I         SXCVD2           T23	T4	TDI		QVDD
T6         TDO         QVDD           T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T11         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18         VSS         Ground         N/A           T20         VSS         Ground         N/A           T21         VSS <td< td=""><td>T5</td><td>VSS</td><td>Ground</td><td>N/A</td></td<>	T5	VSS	Ground	N/A
T7         VSS         Ground         N/A           T8         VSS         Ground         N/A           T9         QVDD         Power         N/A           T10         VSS         Ground         N/A           T11         VDD         Power         N/A           T11         VDD         Power         N/A           T11         VDD         Power         N/A           T12         VSS         Ground         N/A           T13         M3VDD         Power         N/A           T14         VSS         Ground         N/A           T15         VDD         Power         N/A           T16         VSS         Ground         N/A           T17         MVDD         Power         N/A           T18         VSS         Ground         N/A           T20         VSS         Ground         N/A           T21         VSS         Non-user         N/A           T22         SR2_IMP_CAL_RX         I         SXCVDD2           T23         SXPVSS2         Ground         N/A           T24         SXPUD2         Power         N/A           <	Т6	TDO	0	QVDD
T8VSSGroundN/AT9QVDDPowerN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVD2T26SR2_REF_CLKISXCVD2T27ReservedNC	T7	VSS	Ground	N/A
T9QVDDPowerN/AT10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	Т8	VSS	Ground	N/A
T10VSSGroundN/AT11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-	Т9	QVDD	Power	N/A
T11VDDPowerN/AT12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC—	T10	VSS	Ground	N/A
T12VSSGroundN/AT13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	T11	VDD	Power	N/A
T13M3VDDPowerN/AT14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	T12	VSS	Ground	N/A
T14VSSGroundN/AT15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	T13	M3VDD	Power	N/A
T15VDDPowerN/AT16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC—	T14	VSS	Ground	N/A
T16VSSGroundN/AT17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSGroundN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC-	T15	VDD	Power	N/A
T17MVDDPowerN/AT18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	T16	VSS	Ground	N/A
T18VSSGroundN/AT19VDDPowerN/AT20VSSGroundN/AT21VSSNon-userN/AT22SR2_IMP_CAL_RXISXCVDD2T23SXPVSS2GroundN/AT24SXPVDD2PowerN/AT25SR2_REF_CLKISXCVDD2T26SR2_REF_CLKISXCVDD2T27ReservedNC	T17	MVDD	Power	N/A
T19         VDD         Power         N/A           T20         VSS         Ground         N/A           T21         VSS         Non-user         N/A           T22         SR2_IMP_CAL_RX         I         SXCVDD2           T23         SXPVSS2         Ground         N/A           T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T18	VSS	Ground	N/A
T20         VSS         Ground         N/A           T21         VSS         Non-user         N/A           T22         SR2_IMP_CAL_RX         I         SXCVDD2           T23         SXPVSS2         Ground         N/A           T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T19	VDD	Power	N/A
T21         VSS         Non-user         N/A           T22         SR2_IMP_CAL_RX         I         SXCVDD2           T23         SXPVSS2         Ground         N/A           T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T20	VSS	Ground	N/A
T22         SR2_IMP_CAL_RX         I         SXCVDD2           T23         SXPVSS2         Ground         N/A           T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T21	VSS	Non-user	N/A
T23         SXPVSS2         Ground         N/A           T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T22	SR2_IMP_CAL_RX		SXCVDD2
T24         SXPVDD2         Power         N/A           T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T23	SXPVSS2	Ground	N/A
T25         SR2_REF_CLK         I         SXCVDD2           T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T24	SXPVDD2	Power	N/A
T26         SR2_REF_CLK         I         SXCVDD2           T27         Reserved         NC         —	T25	SR2_REF_CLK	I	SXCVDD2
T27 Reserved NC —	T26	SR2_REF_CLK	I	SXCVDD2
	T27	Reserved	NC	_
T28 Reserved NC —	T28	Reserved	NC	_
U1 M1DQ8 I/O GVDD1	U1	M1DQ8	I/O	GVDD1
U2 VSS Ground N/A	U2	VSS	Ground	N/A



Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name
AB1	M1DQS2	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	0	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	0	GVDD1
AB8	M1A11	0	GVDD1
AB9	M1A7	0	GVDD1
AB10	M1CK2	0	GVDD1
AB11	M1APAR_OUT	0	GVDD1
AB12	M1ODT1	0	GVDD1
AB13	M1APAR_IN	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	0	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	0	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA <sup>5,8</sup>	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0 <sup>5,8</sup>	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1 <sup>5,8</sup>	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2 <sup>5,8</sup>	I/O	NVDD
AB26	GPI010/IRQ10/RC10 <sup>5,8</sup>	I/O	NVDD
AB27	GPIO5/IRQ5/RC5 <sup>5,8</sup>	I/O	NVDD
AB28	GPIO0/IRQ0/RC0 <sup>5,8</sup>	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	0	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	0	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1



Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name
AE9	M1A8	0	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	0	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD <sup>5,8</sup>	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK <sup>3</sup>	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL <sup>3</sup>	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK <sup>3</sup>	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK <sup>3</sup>	I/O	NVDD
AE27	TDM2RSN/GE1_TD2 <sup>3</sup>	I/O	NVDD
AE28	TDM2RDT/GE1_TD1 <sup>3</sup>	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	0	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	0	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	0	GVDD1
AF8	M1CK0	0	GVDD1
AF9	М1СКО	0	GVDD1
AF10	M1BA1	0	GVDD1
AF11	M1A1	0	GVDD1
AF12	M1WE	0	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	0	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	0	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD <sup>5,8</sup>	I/O	NVDD
AF22	TDM0RSN/GE2_TD2 <sup>3</sup>	I/O	NVDD
AF23	TDM0TDT/GE2_TD3 <sup>3</sup>	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL <sup>3</sup>	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD



Ball Number	Signal Name <sup>1,2</sup>	Pin Type <sup>10</sup>	Power Rail Name	
AH17	M1DQS6	I/O	GVDD1	
AH18	I/O	GVDD1		
AH19	M1DQ48	I/O	GVDD1	
AH20	M1DQ49	I/O	GVDD1	
AH21	VSS	Ground	N/A	
AH22	TDM0RCK/GE2_RD2 <sup>3</sup>	I/O	NVDD	
AH23	TDM0RDT/GE2_RD3 <sup>3</sup>	I/O	NVDD	
AH24	TDM0TSN/GE2_RD0 <sup>3</sup>	I/O	NVDD	
AH25	TDM1RCK/GE2_RD1 <sup>3</sup>	I/O	NVDD	
AH26	TDM3TDT/GE1_RD3 <sup>3</sup>	I/O	NVDD	
AH27	TDM3TCK/GE1_RD2 <sup>3</sup>	I	NVDD	
AH28	VSS	Ground	N/A	
<ol> <li>Notes: 1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).</li> <li>2. Signal function during power-on reset is determined by the RCW source type.</li> <li>3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.</li> <li>4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.</li> <li>5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the <i>GPIO</i> chapter in the <i>MSC8151 Reference Manual</i>.</li> <li>6. Open-drain signal.</li> <li>7. Internal 20 KΩ pull-up resistor.</li> <li>8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. South and the MSC8151 Reference of the MSC8151 Reference of the MSC8151 Reference of the MSC8151 Reference dation and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. South a CPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. South a CPIO chapter of the MSC8151 Reference of the MSC8151 Reference Manual.</li> </ol>				

Connect to power supply via external filter. See Section 3.2, PLL Power Supply Design Considerations for details.

Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.



### 2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with  $V_{DDDDR} = 1.5 \text{ V}$ .

#### Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O reference voltage	MV <sub>REF</sub>	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2,3,4
Input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.100	V <sub>DDDDR</sub>	V	5
Input low voltage	V <sub>IL</sub>	GND	MV <sub>REF</sub> – 0.100	V	5
I/O leakage current	I <sub>OZ</sub>	-50	50	μA	6

Notes: 1. V<sub>DDDDR</sub> is expected to be within 50 mV of the DRAM V<sub>DD</sub> at all times. The DRAM and memory controller can use the same or different sources.

2.  $MV_{REF}$  is expected to be equal to  $0.5 \times V_{DDDDR}$ , and to track  $V_{DDDDR}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed ±1% of the DC value.

 V<sub>TT</sub> is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV<sub>REF</sub> with a minimum value of MV<sub>REF</sub> – 0.4 and a maximum value of MV<sub>REF</sub> + 0.04 V. V<sub>TT</sub> should track variations in the DC-level of MV<sub>REF</sub>.

- 4. The voltage regulator for MV<sub>REF</sub> must be <u>able</u> to supply up to 250  $\mu$ A.
- 5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
- **6.** Output leakage is measured with all outputs are disabled,  $0 V \le V_{OUT} \le V_{DDDDR}$ .

### 2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

**Note:** At recommended operating conditions (see Table 3) with V<sub>DDDDR</sub> = 1.8 V for DDR2 memory or V<sub>DDDDR</sub> = 1.5 V for DDR3 memory.

#### Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Мах	Unit
I/O capacitance: DQ, DQS, DQS	C <sub>IO</sub>	6	8	pF
Delta I/O capacitance: DQ, DQS, DQS	C <sub>DIO</sub>	—	0.5	pF
Note: Guaranteed by FAB process and micro-constructio	n.			



rical Characteristics

### 2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV<sub>REF</sub>.

Note: Values when used at recommended operating conditions (see Table 3).

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV <sub>REFn</sub> • DDR2 SDRAM • DDR3 SDRAM	I <sub>MVREFn</sub>		300 250	μΑ μΑ

#### Table 9. Current Draw Characteristics for MV<sub>REF</sub>

## 2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8151 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, "HSSI AC Timing Specifications."

### 2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]\_TX and  $\overline{SR[1–2]}_TX$ ) or a receiver input (SR[1–2]\_RX and  $\overline{SR[1–2]}_RX$ ). Each signal swings between A volts and B volts where A > B.



Figure 4. Differential Voltage Definitions for Transmitter or Receiver



**Note:** Specifications are valid at the recommended operating conditions listed in Table 3.

|--|

Parameter	Symbol	Min	Typical	Мах	Units	Notes		
Differential peak-to-peak output voltage	V <sub>TX-DIFFp-p</sub>	800	1000	1200	mV	1		
De-emphasized differential output voltage (ratio)	V <sub>TX-DE-RATIO</sub>	3.0	3.5	4.0	dB	2		
DC differential Tx impedance	Z <sub>TX-DIFF-DC</sub>	80	100	120	Ω	3		
Transmitter DC impedance	Z <sub>TX-DC</sub>	40	50	60	Ω	4		
Notes: 1 Very and - 2 × Very - Very - Measured at the package pips with a test load of 50 O to GND on each pip								

V<sub>TX-DIFFp-p</sub> = 2 × |V<sub>TX-D+</sub> - V<sub>TX-D-</sub>| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 Ratio of the V<sub>TX-DIFFp-p</sub> of the second and following bits after a transition divided by the V<sub>TX-DIFFp-p</sub> of the first bit after a

2. Ratio of the  $v_{TX-DIFFP-P}$  of the second and following bits after a transition divided by the  $v_{TX}$ . transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.

**3.** Tx DC differential mode low impedance

4. Required Tx D+ as well as D– DC Impedance during all states

### Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Notes
Differential input peak-to-peak voltage	V <sub>RX-DIFFp-p</sub>	120	1000	1200	mV	1
DC differential Input Impedance	Z <sub>RX-DIFF-DC</sub>	80	100	120	Ω	2
DC input impedance	Z <sub>RX-DC</sub>	40	50	60	Ω	3
Powered down DC input impedance	Z <sub>RX-HIGH-IMP-DC</sub>	50	—	—	KΩ	4
Electrical idle detect threshold	V <sub>RX-IDLE-DET-DIFFp-p</sub>	65	—	175	mV	5

V<sub>RX-DIFFp-p</sub> = 2 × |V<sub>RX-D+</sub> - V<sub>RX-D-</sub>| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

5.  $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$ . Measured at the package pins of the receiver

### 2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

#### Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes	
Output voltage	Vo	-0.40	—	2.30	V	1	
Long run differential output voltage	V <sub>DIFFPP</sub>	800	—	1600	mVp-p	—	
Short run differential output voltage V <sub>DIFFPP</sub> 500 — 1000 mVp-p —							
Note: Voltage relative to COMMON of either signal comprising a differential pair.							





### Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16.	SGMII DC	Receiver	Electrical	Characteristics <sup>5</sup>
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Parameter		Symbol	Min	Тур	Max	Unit	Notes
DC Input voltage range		—		N/A		—	1
Input differential	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	V <sub>RX_DIFFp-p</sub>	100	—	1200	mV	2, 4
voltage	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		175	—			
Loss of signal         SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1         VLOS		30	—	100	mV	3, 4	
threshold	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		65	—	175		
Receiver diffe	erential input impedance	Z <sub>RX_DIFF</sub>	80	—	120	W	—
Notos: 1	Input must be externally AC coupled	•	•	•	•	•	•

**tes:** 1. Input must be externally AC-coupled.

2.  $V_{RX\_DIFFp-p}$  is also referred to as peak-to-peak input differential voltage.

3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the PCI Express Specification document. for details.

4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.

5. The supply voltage is 1.0 V.



#### Table 21. DDR SDRAM Output AC Timing Specifications (continued)

		Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes			
Notes:	1.	The symbols used for timing specifications follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for								
		inputs and t <sub>(first two letters of functional block)</sub> (refere	ence)(state)(signal)(s	tate) for outputs. Output	ut hold time can be rea	ad as DDR 1	timing			
		(DD) from the fising of failing edge of the real type was symbolizes DDR timing (DD) for the	time those mem	ory clock reference (K	) ages from the high (F	JA). FOI exa H) state unti	il outouts			
		(A) are setup (S) or output valid time. Also, $t_{D}$	אס ואסע symbolize	es DDR timing (DD) for	r the time $t_{MCK}$ memory	v clock refe	rence (K)			
		goes low (L) until data outputs (D) are invalid (X) or data output hold time.								
	2.	All MCK/MCK referenced measurements are	e made from the	crossi <u>ng of</u> t <u>he tw</u> o sig	gnals.					
	3.	ADDR/CMD includes all DDR SDRAM output	it signals except	MCK/MCK, MCS, and	I MDQ/MECC/MDM/M	DQS.				
	4.	Note that t <sub>DDKHMH</sub> follows the symbol conver	ntions described	in note 1. For example	e, t <sub>DDKHMH</sub> describes t	he DDR tim	ning (DD)			
		from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t <sub>DDKHMH</sub> can be modified through control of								
		CLK CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same								
		adjustment value. See the MSC8151 Reference Manual for a description and understanding of the timing modifications								
		enabled by use of these bits.			0	•				
	5.	Determined by maximum possible skew betw	ween a data strol	be (MDQS) and any c	orresponding bit of dat	a (MDQ), E	CC			
	_	(MECC), or data mask (MDM). The data stro	be should be ce	ntered inside of the da	ata eye at the pins of the	ne MSC815	1.			
	6.	At recommended operating conditions with V	/ <sub>DDDDR</sub> (1.5 V or	1,8 V) ± 5%.						

**Note:** For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by <sup>1</sup>/<sub>2</sub> applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t<sub>DDKHMH</sub>).



Figure 12. MCK to MDQS Timing



### 2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs ( $SR[1-2]_TX[n]$  and  $\overline{SR[1-2]_TX[n]}$ ) or at the receiver inputs ( $SR[1-2]_RX[n]$  and  $\overline{SR[1-2]_RX[n]}$ ) as depicted in Figure 19, respectively.



Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF\_CLK jitter.

Parameter	Symbol	Min	Тур	Max	Unit	Notes		
Deterministic Jitter	JD	—	—	0.17	UI p-p	—		
Total Jitter	JT	—	—	0.35	UI p-p	2		
Unit Interval	UI	799.92	800	800.08	ps	1		
Notes: 1. See Figure 18 for single frequency sinusoidal jitter limits								

**2.** Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF\_CLK jitter.

**Table 30. SGMII Receive AC Timing Specifications** 

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10 <sup>-12</sup>	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3
Notes: 1 Measured at receiver						

s: 1. Measured at receive

Refer to RapidIO<sup>TM</sup> 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
 Each UI is 800 ps ± 100 ppm.





Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)



Figure 30 shows the boundary scan (JTAG) timing diagram.



Figure 30. Boundary Scan (JTAG) Timing





Figure 31. Test Access Port Timing

Figure 32 shows the  $\overline{\text{TRST}}$  timing diagram.



Figure 32. TRST Timing



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### 3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Signal Name			Pin connection
MAPAR_OUT		-	NC
MAPAR_IN			NC
Notes:	1. 2.	For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2. For MSC8151 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8151, connecting these pins to GND increases device power consumption.	

## 3.5.2 HSSI-Related Pins

### 3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Signal Name	Pin Connection	
SR_IMP_CAL_RX	NC	
SR_IMP_CAL_TX	NC	
SR[1-2]_REF_CLK	SXCVSS	
SR[1-2]_REF_CLK	SXCVSS	
SR[1-2]_RXD[3-0]	SXCVSS	
SR[1-2]_RXD[3-0]	SXCVSS	
SR[1-2]_TXD[3-0]	NC	
SR[1-2]_TXD[3-0]	NC	
SR[1-2]_PLL_AVDD	In use	
SR[1–2]_PLL_AGND	In use	
SXPVSS	In use	
SXCVSS	In use	
SXPVDD	In use	
SXCVDD	In use	
Note: All lanes in the HSSI SerDes should be powered down. Refer to the MSC8151 Reference Manual for details.		

### 3.5.2.2 HSSI Specific Lane Is Not Used

### Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
SR[1-2]_REF_CLK	In use
SR[1-2]_REF_CLK	In use



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#### Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

	Signal Name	Pin Connection
TDM <b>n</b> TCLK		GND
TDMT <b>n</b> DAT		GND
TDM <b>n</b> TSYN		GND
V <sub>DDIO</sub>		2.5 V
Notes:         1.         n = {0, 1, 2,         2.         In case of s         MSC8151 F	<i>n</i> = {0, 1, 2,3} In case of subset of TDM interface usage please make sure to disable unused TDM modules. See <i>TDM</i> chapter in the <i>MSC8151 Reference Manual</i> for details.	

## 3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
INT_OUT	NC
IRQ[15-0]	See the GPIO connectivity guidelines in this table.
NMI	V <sub>DDIO</sub>
NMI_OUT	NC
RC[21–0]	GND
STOP_BS	GND
тск	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
TRST	See Section 3.1 for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1-0]	See the GPIO connectivity guidelines in this table.
DRQ[1-0]	See the GPIO connectivity guidelines in this table.
RCW_LSEL_0	GND
RCW_LSEL_1	GND
RCW_LSEL_2	GND
RCW_LSEL_3	GND
V <sub>DDIO</sub>	2.5 ∨

**Note:** For details on configuration, see the *MSC8151 Reference Manual*. For additional information, refer to the *MSC815x* and *MSC825x DSP Family Design Checklist*.

age Information



# Package Information



### NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- A MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
- A DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- A PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
- 6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
- 7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

### Figure 40. MSC8151 Mechanical Information, 783-ball FC-PBGA Package