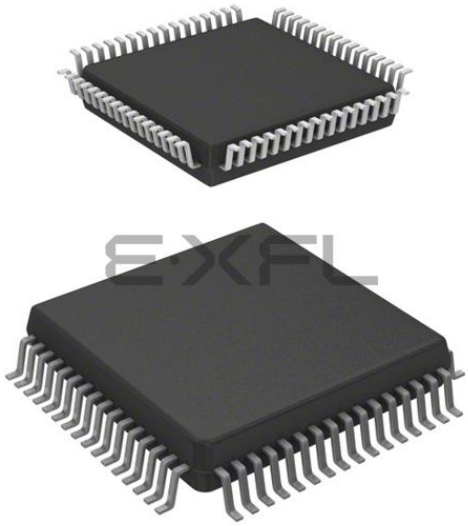

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
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Peripherals	POR, PWM
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908ab32cfu

Section 20. Computer Operating Properly (COP)

Section 21. Low-Voltage Inhibit (LVI)

Figure	Title	Page

List of Tables

1.6.14 Port D I/O Pins (PTD7–PTD0)

PTD7–PTD0 are general-purpose bidirectional I/O port pins. PTD6 and PTD4 are special function port pins that are shared with the timer interface modules (TIMA and TIMB). See **Section 11. Timer Interface Module A (TIMA)** and **Section 12. Timer Interface Module B (TIMB)**.

1.6.15 Port E I/O Pins (PTE7/SPSCK–PTE0/TxD)

PTE7–PTE0 are special function, bidirectional port pins. PTE7–PTE4 are shared with the serial peripheral interface mode (SPI), PTE3–PTE2 are shared with timer A (TIMA), and PTE1–PTE0 are shared with the serial communications interface (SCI). See **Section 15. Serial Communications Interface Module (SCI)**, **Section 16. Serial Peripheral Interface Module (SPI)**, **Section 11. Timer Interface Module A (TIMA)**, and **Section 17. Input/Output (I/O) Ports**.

1.6.16 Port F I/O Pins (PTF7–PTF0/TACH2)

PTF7–PTF6 are general-purpose bidirectional I/O port pins. PTF5–PTF0 are special function, bidirectional port pins. PTF5–PTF2 are shared with timer B (TIMB), and PTF1–PTF0 are shared with timer A (TIMA). See **Section 11. Timer Interface Module A (TIMA)**, **Section 12. Timer Interface Module B (TIMB)**, and **Section 17. Input/Output (I/O) Ports**.

1.6.17 Port G I/O Pins (PTG2/KBD2–PTG0/KBD0)

PTG2–PTG0 are general-purpose bidirectional I/O pins with keyboard wakeup function. See **Section 19. Keyboard Interrupt Module (KBI)** and **Section 17. Input/Output (I/O) Ports**.

1.6.18 Port H I/O Pins (PTH1/KBD4–PTH0/KBD3)

PTH1–PTH0 are general-purpose bidirectional I/O pins with Keyboard wakeup function. See **Section 19. Keyboard Interrupt Module (KBI)** and **Section 17. Input/Output (I/O) Ports**.

Table 1-1. I/O Pins Summary

Pin Name	Function	Driver Type	Hysteresis	Reset State
PTF4/TBCH0	General purpose I/O / Timer B channel 0	Dual State	Yes	Input (Hi-Z)
PTF3/TBCH3	General purpose I/O / Timer B channel 3	Dual State	Yes	Input (Hi-Z)
PTF2/TBCH2	General purpose I/O / Timer B channel 2	Dual State	Yes	Input (Hi-Z)
PTF1/TACH3	General purpose I/O / Timer A channel 3	Dual State	Yes	Input (Hi-Z)
PTF0/TACH2	General purpose I/O / Timer A channel 2	Dual State	Yes	Input (Hi-Z)
PTG2/KBD2–PTG0/KBD0	General purpose I/O with key wakeup feature	Dual State	Yes	Input (Hi-Z)
PTH1/KBD4–PTH0/KBD3	General purpose I/O with key wakeup feature	Dual State	Yes	Input (Hi-Z)
V_{DD}	Logical chip power supply	NA	NA	NA
V_{SS}	Logical chip ground	NA	NA	NA
V_{DDA}	Analog power supply (CGM)	NA	NA	NA
V_{SSA}	Analog ground (CGM)	NA	NA	NA
V_{REFH}	ADC reference voltage	NA	NA	NA
A_{VSS}/V_{REFL}	ADC ground and reference voltage	NA	NA	NA
V_{DDAREF}	ADC power supply	NA	NA	NA
OSC1	External clock in	NA	NA	Input (Hi-Z)
OSC2	External clock out	NA	NA	Output
CGMXFC	PLL loop filter cap	NA	NA	NA
$\overline{IRQ}$	External interrupt request	NA	NA	Input (pullup)
$\overline{RST}$	Reset	NA	NA	Input (pullup)

Details of the clock connections to each of the modules on the MC68HC908AB32 are shown in **Table 1-2**. A short description of each clock source is also given in **Table 1-3**.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0032	Timer B Channel 2 Status and Control Register (TBSC2)	Read:	CH2F	CH2IE	MS2B	MS2A	ELS2B	ELS2A	TOV2	CH2MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0033	Timer B Channel 2 Register High (TBCH2H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0034	Timer B Channel 2 Register Low (TBCH2L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0035	Timer B Channel 3 Status and Control Register (TBSC3)	Read:	CH3F	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	CH3MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0036	Timer B Channel 3 Register High (TACH3H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0037	Timer B Channel 3 Register Low (TBCH3L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0038	Analog-to-Digital Status and Control Register (ADSCR)	Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
$0039	Analog-to-Digital Data Register (ADR)	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003A	Analog-to-Digital Clock Register (ADCLK)	Read:	ADIV2	ADIV1	ADIV0	ADICLK	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003B	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								

= Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 6 of 11)

Section 3. Random-Access Memory (RAM)

3.1 Contents

3.2 Introduction

This section describes the 1024 bytes of RAM (random-access memory).

3.3 Functional Description

Addresses $0050 through $044F are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64K-byte memory space.

NOTE: *For correct operation, the stack pointer must point only to RAM locations.*

Within page zero are 176 bytes of RAM. Because the location of the stack RAM is programmable, all page zero RAM locations can be used for I/O control and user data or code. When the stack pointer is moved from its reset location at $00FF out of page zero, direct addressing mode instructions can efficiently access all page zero RAM locations. Page zero RAM, therefore, provides ideal locations for frequently accessed global variables.

Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers.

NOTE: *For M6805 compatibility, the H register is not stacked.*

Table 7-1. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X CMP *opr*,SP CMP *opr*,SP	Compare A with M	(A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
COM *opr* COMA COMX COM *opr*,X COM ,X COM *opr*,SP	Complement (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	0	–	–	↕	↕	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	4 1 1 4 3 5
CPHX #*opr* CPHX *opr*	Compare H:X with M	(H:X) – (M:M + 1)	↕	–	–	↕	↕	↕	IMM DIR	65 75	ii ii+1 dd	3 4
CPX #*opr* CPX *opr* CPX *opr* CPX ,X CPX *opr*,X CPX *opr*,X CPX *opr*,SP CPX *opr*,SP	Compare X with M	(X) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		2
DBNZ *opr,rel* DBNZA *rel* DBNZX *rel* DBNZ *opr*,X,*rel* DBNZ X,*rel* DBNZ *opr*,SP,*rel*	Decrement and Branch if Not Zero	A ← (A) – 1 or M ← (M) – 1 or X ← (X) – 1 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 4 + *rel* ? (result) ≠ 0	–	–	–	–	–	–	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC *opr* DECA DECX DEC *opr*,X DEC ,X DEC *opr*,SP	Decrement	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1 M ← (M) – 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	–	–	–	–	↕	↕	INH	52		7

8.3.1 Bus Timing

In user mode, the internal bus frequency is either the crystal oscillator output (CGMXCLK) divided by four or the PLL output (CGMVCLK) divided by four. See **Section 9. Clock Generator Module (CGM)**.

8.3.2 Clock Start-Up from POR or LVI Reset

When the power-on reset module or the low-voltage inhibit module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 CGMXCLK cycle POR timeout has been completed. The $\overline{\text{RST}}$ pin is driven low by the SIM during this entire period. The IBUS clocks start upon completion of the timeout.

8.3.3 Clocks in Stop and Wait Modes

Upon exit from stop mode (by an interrupt, break, or reset), the SIM allows CGMXCLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. This timeout is selectable as 4096 or 32 CGMXCLK cycles. (See **8.7.2 Stop Mode**.)

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

8.4 Reset and System Initialization

The MCU has the following reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

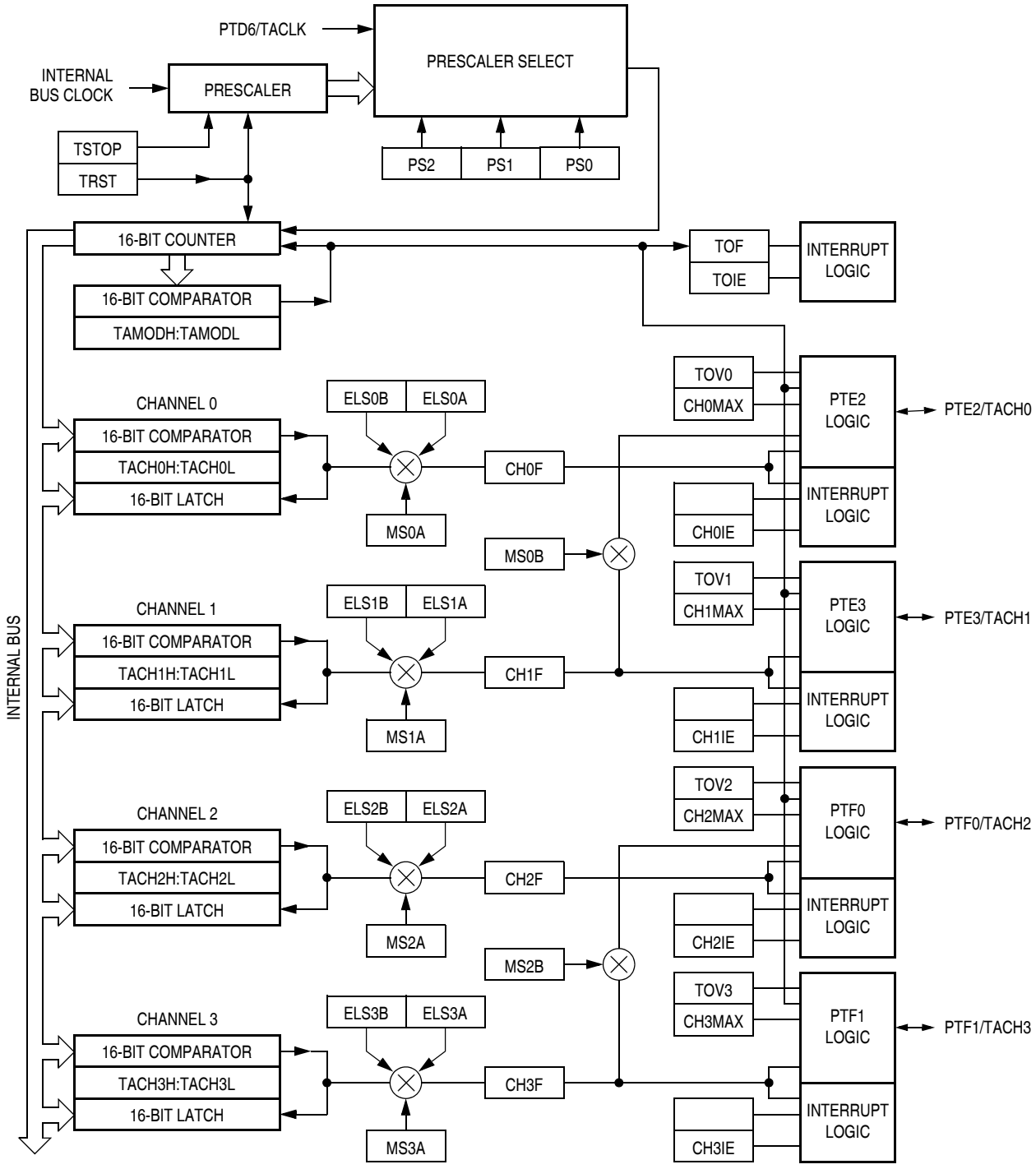

Figure 11-1. TIMA Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$002B	Timer A Channel 1 Register Low (TACH1L)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$002C	Timer A Channel 2 Status and Control Register (TASC2)	Read: Write:	CH2F 0	CH2IE	MS2B	MS2A	ELS2B	ELS2A	TOV2	CH2MAX
		Reset:	0	0	0	0	0	0	0	0
$002D	Timer A Channel 2 Register High (TACH2H)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$002E	Timer A Channel 2 Register Low (TACH2L)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$002F	Timer A Channel 3 Status and Control Register (TASC3)	Read: Write:	CH3F 0	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	CH3MAX
		Reset:	0	0	0	0	0	0	0	0
$0030	Timer A Channel 3 Register High (TACH3H)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0031	Timer A Channel 3 Register Low (TACH3L)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							

= Unimplemented

Figure 11-2. TIMA I/O Register Summary (Sheet 2 of 2)

11.5.2 Input Capture

With the input capture function, the TIMA can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIMA latches the contents of the TIMA counter into the TIMA channel registers, TACHxH:TACHxL. The polarity of the active edge is programmable. Input captures can generate TIMA CPU interrupt requests.

11.5.4.2 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the PTE2/TACH0 pin. The TIMA channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIMA channel 0 status and control register (TASC0) links channel 0 and channel 1. The TIMA channel 0 registers initially control the pulse width on the PTE2/TACH0 pin. Writing to the TIMA channel 1 registers enables the TIMA channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIMA channel registers (0 or 1) that control the pulse width are the ones written to last. TASC0 controls and monitors the buffered PWM function, and TIMA channel 1 status and control register (TASC1) is unused. While the MS0B bit is set, the channel 1 pin, PTE3/TACH1, is available as a general-purpose I/O pin.

Channels 2 and 3 can be linked to form a buffered PWM channel whose output appears on the PTF0/TACH2 pin. The TIMA channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS2B bit in TIMA channel 2 status and control register (TASC2) links channel 2 and channel 3. The TIMA channel 2 registers initially control the pulse width on the PTF0/TACH2 pin. Writing to the TIMA channel 3 registers enables the TIMA channel 3 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIMA channel registers (2 or 3) that control the pulse width are the ones written to last. TASC2 controls and monitors the buffered PWM function, and TIMA channel 3 status and control register (TASC3) is unused. While the MS2B bit is set, the channel 3 pin, PTF1/TACH3, is available as a general-purpose I/O pin.

NOTE: *In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

11.5.4.3 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIMA status and control register (TASC):
   a. Stop the TIMA counter by setting the TIMA stop bit, TSTOP.
   b. Reset the TIMA counter by setting the TIMA reset bit, TRST.
2. In the TIMA counter modulo registers (TAMODH:TAMODL), write the value for the required PWM period.
3. In the TIMA channel x registers (TACHxH:TACHxL), write the value for the required pulse width.
4. In TIMA channel x status and control register (TASCx):
   a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB:MSxA. See **Table 11-3**.
   a. Write 1 to the toggle-on-overflow bit, TOVx.
   b. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB:ELSxA. The output action on compare must force the output to the complement of the pulse width level. See **Table 11-3**.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

5. In the TIMA status control register (TASC), clear the TIMA stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIMA channel 0 registers (TACH0H:TACH0L) initially control the buffered PWM output. TIMA channel 0 status and control register 0 (TASC0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

12.10.4 TIMB Channel Status and Control Registers

Each of the TIMB channel status and control registers does the following:

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIMB overflow
- Selects 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

Address: $0045

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Figure 12-9. TIMB Channel 0 Status and Control Register (TBSC0)

Address: $0048

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Figure 12-10. TIMB Channel 1 Status and Control Register (TBSC1)

With the misaligned character shown in **Figure 15-7**, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 10 bit times × 16 RT cycles + 3 RT cycles = 163 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is

$$\left|\frac{170 - 163}{170}\right| \times 100 = 4.12\%$$

Fast Data Tolerance

Figure 15-8 shows how much a fast received character can be misaligned without causing a noise error or a framing error. The fast stop bit ends at RT10 instead of RT16 but is still there for the stop bit data samples at RT8, RT9, and RT10.

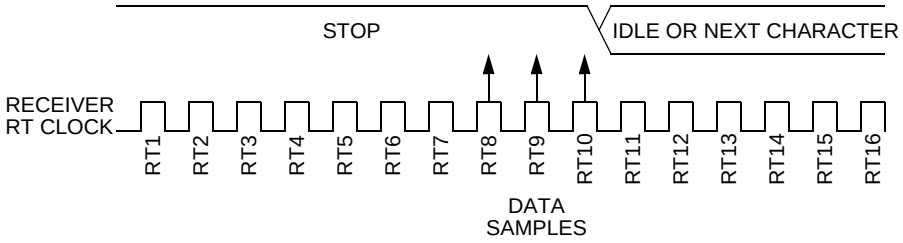

Figure 15-8. Fast Data

For an 8-bit character, data sampling of the stop bit takes the receiver 9 bit times × 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in **Figure 15-8**, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times × 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is

$$\left|\frac{154 - 160}{154}\right| \times 100 = 3.90\dot{}\%$$

15.9.6 SCI Data Register

The SCI data register (SCDR) is the buffer between the internal data bus and the receive and transmit shift registers. Reset has no effect on data in the SCI data register.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	Unaffected by reset							

Figure 15-15. SCI Data Register (SCDR)

R7/T7–R0/T0 — Receive/Transmit Data Bits

Reading address $0018 accesses the read-only received data bits, R7:R0. Writing to address $0018 writes the data to be transmitted, T7:T0. Reset has no effect on the SCI data register.

NOTE: *Do not use read/modify/write instructions on the SCI data register.*

17.6 Port D

Port D is an 8-bit special function port that shares two of its pins with the timer interface module (see **Section 11. Timer Interface Module A (TIMA)** and **Section 12. Timer Interface Module B (TIMB)**). Each port D pin has 15mA current drive (sink) and programmable pullup.

17.6.1 Port D Data Register (PTD)

The port D data register contains a data latch for each of the eight port D pins.

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
Reset:	Unaffected by reset							
Alternative Function:		TACLK		TBCLK				
Additional Functions:	15mA sink	15mA sink	15mA sink	15mA sink	15mA sink	15mA sink	15mA sink	15mA sink
	Input pullup	Input pullup	Input pullup	Input pullup	Input pullup	Input pullup	Input pullup	Input pullup

Figure 17-11. Port D Data Register (PTD)

PTD[7:0] — Port D Data Bits

These read/write bits are software programmable. Data direction of each port D pin is under the control of the corresponding bit in data direction register D. Reset has no effect on port D data.

TACLK — Timer A Clock Input

The PTD6 pin becomes TACLK, the timer A (TIMA) external clock input when the TIMA prescaler select bits, PS[2:0] = 111. See **Section 11. Timer Interface Module A (TIMA)**.

TBCLK — Timer B Clock Input

The PTD4 pin becomes TBCLK, the timer B (TIMB) external clock input when the TIMB prescaler select bits, PS[2:0] = 111. See **Section 12. Timer Interface Module B (TIMB)**.

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