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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908ab32mpb

1.7 I/O Pin Summary

Table 1-1. I/O Pins Summary

Pin Name	Function	Driver Type	Hysteresis	Reset State
PTA7–PTA0	General purpose I/O	Dual State	No	Input (Hi-Z)
PTB7/ATD7–PTB0/ATD0	General purpose I/O / ADC channel	Dual State	No	Input (Hi-Z)
PTC5–PTC3	General purpose I/O	Dual State	No	Input (Hi-Z)
PTC2/MCLK	General purpose I/O / System clock	Dual State	No	Input (Hi-Z)
PTC1–PTC0	General purpose I/O	Dual State	No	Input (Hi-Z)
PTD7	General purpose I/O	Dual State	No	Input (Hi-Z)
PTD6/TACLK	General purpose I/O / Timer external input clock	Dual State	No	Input (Hi-Z)
PTD5	General purpose I/O	Dual State	No	Input (Hi-Z)
PTD4/TBCLK	General purpose I/O / Timer external input clock	Dual State	No	Input (Hi-Z)
PTD3–PTD0	General purpose I/O	Dual State	No	Input (Hi-Z)
PTE7/SPSCK	General purpose I/O / SPI clock	Dual State (open drain)	Yes	Input (Hi-Z)
PTE6/MOSI	General purpose I/O / SPI data path	Dual State (open drain)	Yes	Input (Hi-Z)
PTE5/MISO	General purpose I/O / SPI data path	Dual State (open drain)	Yes	Input (Hi-Z)
PTE4/$\overline{SS}$	General purpose I/O / SPI slave select	Dual State	Yes	Input (Hi-Z)
PTE3/TACH1	General purpose I/O / Timer A channel 1	Dual State	Yes	Input (Hi-Z)
PTE2/TACH0	General purpose I/O / Timer A channel 0	Dual State	Yes	Input (Hi-Z)
PTE1/RxD	General purpose I/O / SCI receive data	Dual State	Yes	Input (Hi-Z)
PTE0/TxD	General purpose I/O / SCI transmit data	Dual State	Yes	Input (Hi-Z)
PTF7–PTF6	General purpose I/O	Dual State	Yes	Input (Hi-Z)
PTF5/TBCH1	General purpose I/O / Timer B channel 1	Dual State	Yes	Input (Hi-Z)

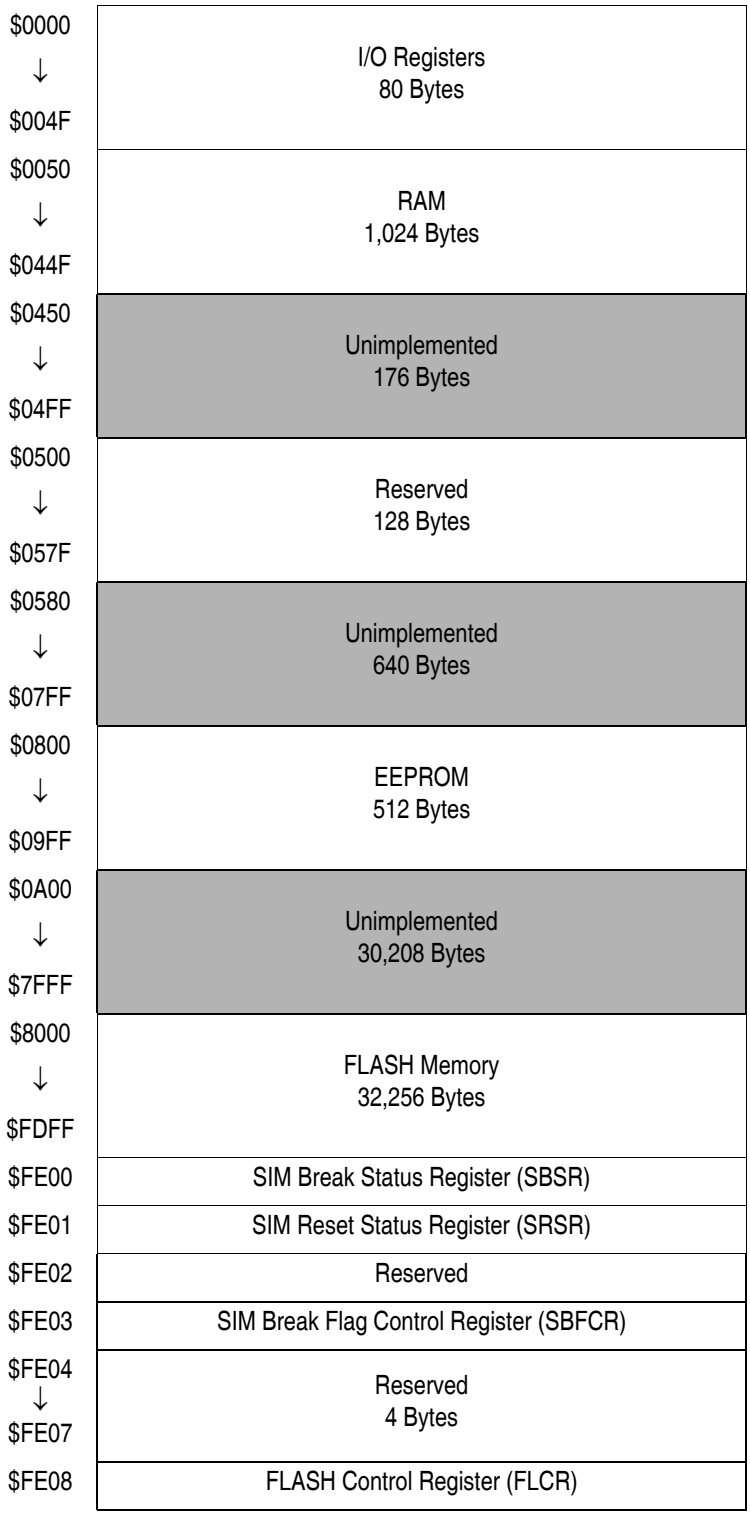


Figure 2-1. Memory Map

Section 4. FLASH Memory

4.1 Contents

4.2 Introduction

This section describes the operation of the embedded FLASH memory. This memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

4.3 Functional Description

The FLASH memory is an array of 32,256 bytes with an additional 48 bytes of user vectors and one byte of block protection. *An erased bit reads as logic 1 and a programmed bit reads as a logic 0*. Memory in the FLASH array is organized into two rows per page basis. For the 32K word by 8-Bit Embedded FLASH Memory, the page size is 128 bytes per

			CON3	CON2	CON1	EEPRTCT	EEBP3	EEBP2	EEBP1	EEBP0
$FE1F	EEPROM Array Configuration Register (EEACR)	Read:								
		Write:								
		Reset:	Contents of EENVR ($FE1C)							

* Non-volatile EEPROM register; write by programming.

= Unimplemented R = Reserved

Figure 5-1. EEPROM I/O Register Summary

5.4 Functional Description

The 512 bytes of EEPROM is located at $0800–$09FF, and can be programmed or erased without an additional external high voltage supply. The program and erase operations are enabled through the use of an internal charge pump. For each byte of EEPROM, the write/erase endurance is 10,000 cycles.

5.5 EEPROM Configuration

The 8-bit EEPROM non-volatile register (EENVR) and the 16-bit EEPROM timebase divider non-volatile register (EEDIVNVR) contain the default settings for the following EEPROM configurations:

- Security option
- Block protection
- EEPROM timebase reference

EENVR and EEDIVNVR are non-volatile, EEPROM registers. They are programmed and erased in the same way as EEPROM bytes. The contents of these registers are loaded into their respective volatile registers during a MCU reset. The values in these read/write, volatile registers define the EEPROM configurations.

For EENVR, the corresponding volatile register is the EEPROM array configuration register (EEACR).

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE: *To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

Z — Zero flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

Table 7-1. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
SUB *#opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		9
TAP	Transfer A to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		2
TAX	Transfer A to X	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to A	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST *opr* TSTA TSTX TST *opr*,X TST ,X TST *opr*,SP	Test for Negative or Zero	(A) – $00 or (X) – $00 or (M) – $00	0	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	–	–	–	–	–	–	INH	95		2
TXA	Transfer X to A	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) – 1	–	–	–	–	–	–	INH	94		2

Table 8-3. Vector Addresses

Vector Priority	Address	Vector
Lowest	$FFD0	ADC Conversion Complete Vector (High)
	$FFD1	ADC Conversion Complete Vector (Low)
	$FFD2	Keyboard Vector (High)
	$FFD3	Keyboard Vector (Low)
	$FFD4	SCI Transmit Vector (High)
	$FFD5	SCI Transmit Vector (Low)
	$FFD6	SCI Receive Vector (High)
	$FFD7	SCI Receive Vector (Low)
	$FFD8	SCI Error Vector (High)
	$FFD9	SCI Error Vector (Low)
	$FFDA	Reserved
	$FFDB	Reserved
	$FFDC	Reserved
	$FFDD	Reserved
	$FFDE	Timer B Channel 3 Vector (High)
	$FFDF	Timer B Channel 3 Vector (Low)
	$FFE0	Timer B Channel 2 Vector (High)
	$FFE1	Timer B Channel 2 Vector (Low)
	$FFE2	SPI Transmit Vector (High)
	$FFE3	SPI Transmit Vector (Low)
	$FFE4	SPI Receive Vector (High)
	$FFE5	SPI Receive Vector (Low)
	$FFE6	Timer B Overflow Vector (High)
	$FFE7	Timer B Overflow Vector (Low)
	$FFE8	Timer B Channel 1 Vector (High)
	$FFE9	Timer B Channel 1 Vector (Low)
	$FFEA	Timer B Channel 0 Vector (High)
	$FFEB	Timer B Channel 0 Vector (Low)
	$FFEC	Timer A Overflow Vector (High)
	$FFED	Timer A Overflow Vector (Low)
	$FFEE	Timer A Channel 3 Vector (High)
	$FFEF	Timer A Channel 3 Vector (Low)
	$FFF0	Timer A Channel 2 Vector (High)
	$FFF1	Timer A Channel 2 Vector (Low)
	$FFF2	Timer A Channel 1 Vector (High)
	$FFF3	Timer A Channel 1 Vector (Low)
	$FFF4	Timer A Channel 0 Vector (High)
	$FFF5	Timer A Channel 0 Vector (Low)
	$FFF6	Programmable Interrupt Timer (High)
	$FFF7	Programmable Interrupt Timer (Low)
	$FFF8	PLL Vector (High)
	$FFF9	PLL Vector (Low)
	$FFFA	IRQ Vector (High)
	$FFFB	IRQ Vector (Low)
	$FFFC	SWI Vector (High)
	$FFFD	SWI Vector (Low)
Highest	$FFFE	Reset Vector (High)
	$FFFF	Reset Vector (Low)

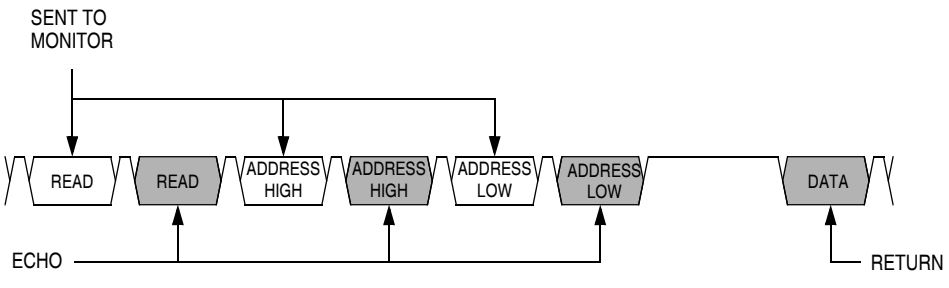
10.4.5 Commands

The monitor ROM uses these commands:

- READ, read memory
- WRITE, write memory
- IREAD, indexed read
- IWRITE, indexed write
- READSP, read stack pointer
- RUN, run user program

A sequence of IREAD or IWRITE commands can access a block of memory sequentially over the full 64k-byte memory map.

Table 10-3. READ (Read Memory) Command

Description	Read byte from memory
Operand	Specifies 2-byte address in high byte:low byte order
Data Returned	Returns contents of specified address
Opcode	$4A
Command Sequence	

Address: $002C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH2F	CH2IE	MS2B	MS2A	ELS2B	ELS2A	TOV2	CH2MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Figure 11-11. TIMA Channel 2 Status and Control Register (TASC2)

Address: $002F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH3F	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	CH3MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Figure 11-12. TIMA Channel 3 Status and Control Register (TASC3)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIMA counter registers matches the value in the TIMA channel x registers.

When TIM CPU interrupt requests are enabled (CHxIE = 1), clear CHxF by reading TIMA channel x status and control register with CHxF set and then writing a logic zero to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing logic zero to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a logic one to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIMA CPU interrupts on channel x.
Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests enabled
0 = Channel x CPU interrupt requests disabled

12.9 I/O Signals

Port F shares four pins with the TIMB and port D shares one. PTD4/TBCLK is an external clock input to the TIMB prescaler. The four TIMB channel I/O pins are PTF4/TBCH0, PTF5/TBCH1, PTF2/TBCH2, and PTF3/TBCH3.

12.9.1 TIMB Clock Pin

PTD4/TBCLK is an external clock input that can be the clock source for the TIMB counter instead of the prescaled internal bus clock. Select the PTD4/TBCLK input by writing logic 1s to the three prescaler select bits, PS[2:0]. See **12.10.1 TIMB Status and Control Register**. The minimum TBCLK pulse width, $TBCLK_{LMIN}$ or $TBCLK_{HMIN}$, is:

$$\frac{1}{\text{bus frequency}} + t_{SU}$$

The maximum TBCLK frequency is:

$$\text{bus frequency} \div 2$$

PTD4/TBCLK is available as a general-purpose I/O pin when not used as the TIMB clock input. When the PTD4/TBCLK pin is the TIMB clock input, it is an input regardless of the state of the DDRD6 bit in data direction register D.

12.9.2 TIMB Channel I/O Pins

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTF2/TBCH2 and PTF5/TBCH1 can be configured as buffered output compare or buffered PWM pins.

PS[2:0] — Prescaler Select Bits

These read/write bits select either the PTD4/TBCLK pin or one of the seven prescaler outputs as the input to the TIMB counter as **Table 12-2** shows. Reset clears the PS[2:0] bits.

Table 12-2. Prescaler Selection

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal Bus Clock ÷1
0	0	1	Internal Bus Clock ÷ 2
0	1	0	Internal Bus Clock ÷ 4
0	1	1	Internal Bus Clock ÷ 8
1	0	0	Internal Bus Clock ÷ 16
1	0	1	Internal Bus Clock ÷ 32
1	1	0	Internal Bus Clock ÷ 64
1	1	1	PTD4/TBCLK

12.10.2 TIMB Counter Registers

The two read-only TIMB counter registers contain the high and low bytes of the value in the TIMB counter. Reading the high byte (TBCNTH) latches the contents of the low byte (TBCNTL) into a buffer. Subsequent reads of TBCNTH do not affect the latched TBCNTL value until TBCNTL is read. Reset clears the TIMB counter registers. Setting the TIMB reset bit (TRST) also clears the TIMB counter registers.

NOTE: *If you read TBCNTH during a break interrupt, be sure to unlatch TBCNTL by reading TBCNTL before exiting the break interrupt. Otherwise, TBCNTL retains the value latched during the break.*

Address: $0041

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-5. TIMB Counter Register High (TBCNTH)

13.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power-consumption standby modes.

13.5.1 Wait Mode

The PIT remains active after the execution of a WAIT instruction. In wait mode the PIT registers are not accessible by the CPU. Any enabled CPU interrupt request from the PIT can bring the MCU out of wait mode.

If PIT functions are not required during wait mode, reduce power consumption by stopping the PIT before executing the WAIT instruction.

13.5.2 Stop Mode

The PIT is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions or the state of the PIT counter. PIT operation resumes when the MCU exits stop mode after an external interrupt.

13.6 PIT During Break Interrupts

A break interrupt stops the PIT counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. See **8.8.3 SIM Break Flag Control Register**.

To allow software to clear status bits during a break interrupt, write a logic one to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a logic zero to the BCFE bit. With BCFE at logic zero (its default state), software can read and write I/O registers during the break state without affecting status

- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight interrupt flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

Table 17-1. Port Control Register Bits Summary (Sheet 1 of 2)

Port	Bit	DDR	Module Control			Pin
			Module	Register	Control Bit	
A	0	DDRA0	—	—	—	PTA0
	1	DDRA1				PTA1
	2	DDRA2				PTA2
	3	DDRA3				PTA3
	4	DDRA4				PTA4
	5	DDRA5				PTA5
	6	DDRA6				PTA6
	7	DDRA7				PTA7
B	0	DDRB0	ADC	ADSCR $0038	ADCH[4:0]	PTB0/ATD0
	1	DDRB1				PTB1/ATD1
	2	DDRB2				PTB2/ATD2
	3	DDRB3				PTB3/ATD3
	4	DDRB4				PTB4/ATD4
	5	DDRB5				PTB5/ATD5
	6	DDRB6				PTB6/ATD6
	7	DDRB7				PTB7/ATD7
C	0	DDRC0	—	—	—	PTC0
	1	DDRC1				PTC1
	2	DDRC2	—	DDRC $0006	MCLKEN	PTC2/MCLK
	3	DDRC3	—	—	—	PTC3
	4	DDRC4				PTC4
	5	DDRC5				PTC5
D	0	DDRD0	—	—	—	PTD0
	1	DDRD1				PTD1
	2	DDRD2				PTD2
	3	DDRD3				PTD3
	4	DDRD4	TIMB	TBSC $0040	PS[2:0]	PTD4/TBCLK
	5	DDRD5	—	—	—	PTD5
	6	DDRD6	TIMA	TASC $0020	PS[2:0]	PTD6/TACLK
	7	DDRD7	—	—	—	PTD7

NOTE: *Avoid glitches on port F pins by writing to the port F data register before changing data direction register F bits from 0 to 1.* ***Figure 17-20*** *shows the port F I/O logic.*

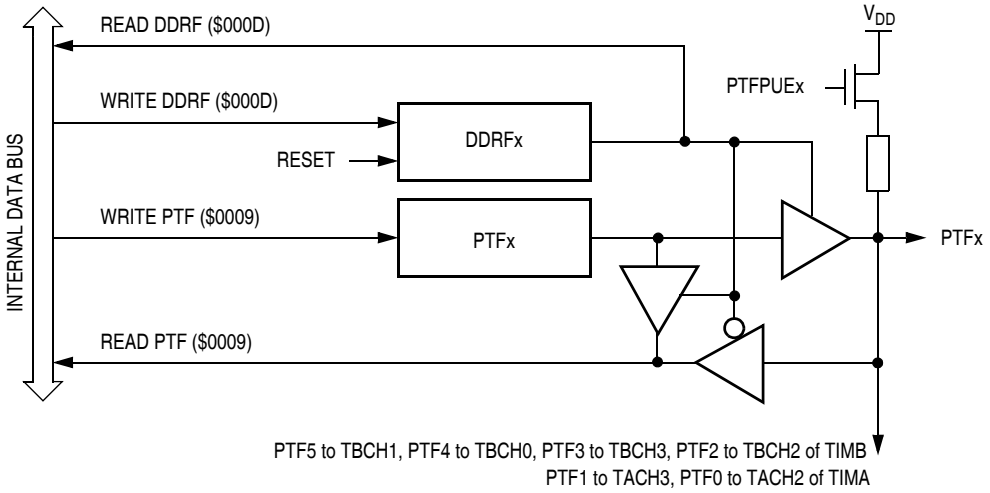


Figure 17-20. Port F I/O Circuit

When DDRFx is a logic 1, reading address $0009 reads the PTFx data latch. When DDRFx is a logic 0, reading address $0009 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

Table 17-7 summarizes the operation of the port F pins.

Table 17-7. Port F Pin Functions

DDRF Bit	PTF Bit	I/O Pin Mode	Accesses to DDRF	Accesses to PTF	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRF[7:0]	Pin	PTF[7:0](3)
1	X	Output	DDRF[7:0]	PTF[7:0]	PTF[7:0]

Notes:
1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect the input.

DDRG[2:0] — Data Direction Register G Bits

These read/write bits control port G data direction. Reset clears DDRG[2:0], configuring all port G pins as inputs.

1 = Corresponding port G pin configured as output
0 = Corresponding port G pin configured as input

NOTE: *Avoid glitches on port G pins by writing to the port G data register before changing data direction register G bits from 0 to 1.* ***Figure 17-24*** *shows the port G I/O logic.*

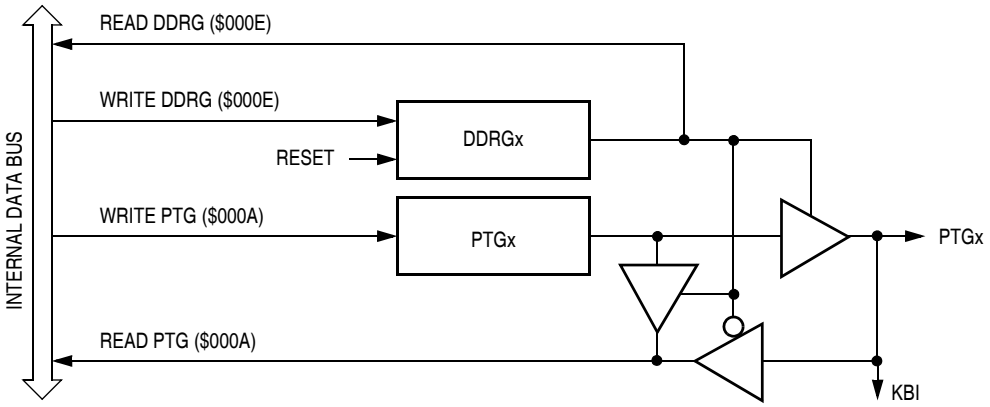


Figure 17-24. Port G I/O Circuit

When DDRGx is a logic 1, reading address $000A reads the PTGx data latch. When DDRGx is a logic 0, reading address $000A reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

Table 17-6 summarizes the operation of the port G pins.

Table 17-8. Port G Pin Functions

DDRG Bit	PTG Bit	I/O Pin Mode	Accesses to DDRG	Accesses to PTG	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRG[2:0]	Pin	PTG[2:0](3)
1	X	Output	DDRG[2:0]	PTG[2:0]	PTG[2:0]

Notes:
1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect the input.

17.10 Port H

Port H is a 2-bit special-function port that shares all two of its pins with the keyboard interrupt (KBI) module.

17.10.1 Port H Data Register (PTH)

The port H data register (PTH) contains a data latch for each of the two port H pins.

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	PTH1	PTH0
Write:								
Reset:	Unaffected by reset							
Alternative Function:							KBD4	KBD3

Figure 17-25. Port H Data Register (PTH)

PTH[1:0] — Port H Data Bits

These read/write bits are software programmable. Data direction of each port H pin is under the control of the corresponding bit in data direction register H. Reset has no effect on port H data.

KBD[4:3] — The keyboard interrupt enable bits, KBIE[4:3], in the keyboard interrupt enable register (KBIER), enable the port H pins as external interrupt pins. See **Section 19. Keyboard Interrupt Module (KBI)**.

17.10.2 Data Direction Register H (DDRH)

Data direction register H determines whether each port H pin is an input or an output. Writing logic 1 to a DDRH bit enables the output buffer for the corresponding port H pin; a logic 0 disables the output buffer.

Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	DDRH1	DDRH0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 17-26. Data Direction Register H (DDRH)

DDRH[1:0] — Data Direction Register H Bits

These read/write bits control port H data direction. Reset clears DDRH[1:0], configuring all port H pins as inputs.

1 = Corresponding port H pin configured as output

0 = Corresponding port H pin configured as input

NOTE: *Avoid glitches on port H pins by writing to the port H data register before changing data direction register H bits from 0 to 1.* ***Figure 17-27*** *shows the port H I/O logic.*

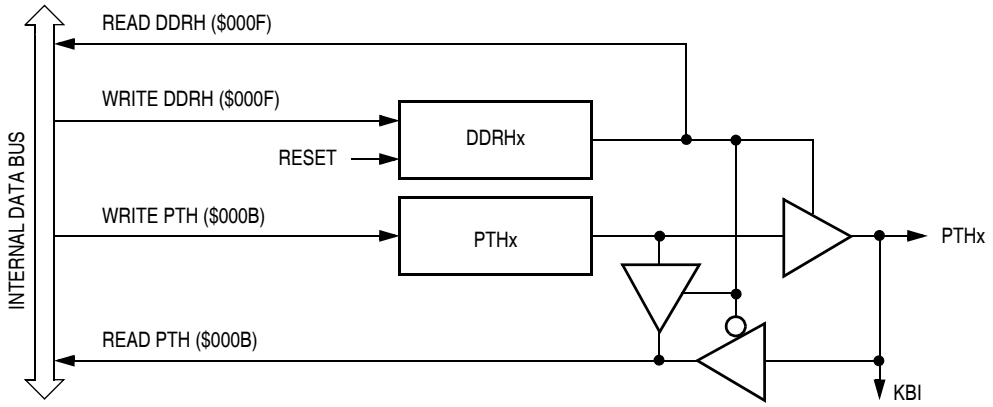


Figure 17-27. Port H I/O Circuit

When DDRHx is a logic 1, reading address $000B reads the PTHx data latch. When DDRHx is a logic 0, reading address $000B reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

Table 17-6 summarizes the operation of the port H pins.