E·XFL

NXP USA Inc. - MC908AB32CFUE Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908ab32cfue

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0	
\$0028	Timer A Channel 0 Register Low	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0	
	(TACH0L)	Reset:		Indeterminate after reset							
	Timer A Channel 1 Status	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX	
\$0029	and Control Register	Write:	0	OTTIL		WOTA	LLUID	LLOIA	1001	OTTWAA	
	(TASC1)	Reset:	0	0	0	0	0	0	0	0	
\$002A	Timer A Channel 1 Register High	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8	
	(TACH1H)	Reset:				Indetermina	te after rese	t		<u> </u>	
\$002B	Timer A Channel 1 Register Low	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0	
	(TACH1L)	Reset:		•		Indetermina	te after rese	t			
	Timer A Channel 2 Status	Read:	CH2F	CH2IE	MS2B	MS2A	ELS2B	ELS2A	TOV2	CH2MAX	
\$002C	and Control Register	Write:	0		MOZD	MOZA	LLOZD	LLOZA	1012		
	(TASC2)	Reset:	0	0	0	0	0	0	0	0	
\$002D	Timer A Channel 2 Register High	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8	
	(TACH2H)	Reset:	Indeterminate after reset								
\$002E	Timer A Channel 2 Register Low	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0	
	(TACH2L)	Reset:	Indeterminate after reset								
	Timer A Channel 3 Status	Read:	CH3F	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	СНЗМАХ	
\$002F	and Control Register	Write:	0	CHOIL		IVISSA	ELSSE	ELSSA	1003	CHOWAX	
	(TASC3)	Reset:	0	0	0	0	0	0	0	0	
\$0030	Timer A Channel 3 Register High	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8	
(TACH3)		Reset:		•		Indetermina	ate after reset				
\$0031	Timer A Channel 3 Register Low	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0	
	(TACH3L)	Reset:		•		Indetermina	te after rese	t		·	
		[= Unimple	mented		R	= Reserve	d		

Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 11)

Memory Map

Lowest SFFD0 ADC Conversion Complete Vector (High) SFFD1 ADC Conversion Complete Vector (Low) SFFD2 Keyboard Vector (High) SFFD3 SCI Transmit Vector (High) SFFD6 SCI Transmit Vector (Low) SFFD6 SCI Receive Vector (High) SFFD7 SCI Receive Vector (High) SFFD8 SCI Error Vector (High) SFFD8 SCI Error Vector (High) SFFD9 SCI Error Vector (Low) SFFD8 Reserved SFFD0 Reserved SFFD0 Reserved SFFD0 Reserved SFFD0 Timer B Channel 3 Vector (Low) SFFE0 Timer B Channel 3 Vector (Low) SFFE1 Timer B Channel 3 Vector (Low) SFFE2 SPI Transmit Vector (High) SFFE4 SPI Receive Vector (High) SFFE5 SPI Reserved SFFE6 Timer B Channel 2 Vector (Low) SFFE6 Timer B Channel 2 Vector (Low) SFFE7 Timer B Channel 2 Vector (Low) SFFE6 Timer B Channel 2 Vector (Low) SFFE7 SPI Receive Vector (High) SFFE7 Timer B Overflow Vector (High) SFFE7 Timer B Overflow Vector (High) SFFE6 Timer B Channel 1 Vector (Low) SFFE8 Timer B Channel 1 Vector (Low) SFFE8 Timer B Channel 1 Vector (Low) SFFE8 Timer B Channel 1 Vector (Low) SFFE9 Timer A Channel 1 Vector (Low) SFFE9 Timer A Channel 3 Vector (Low) SFFE9 Timer A Channel 3 Vector (Low) SFFFE9 Timer A Channel 3 Vector (Low) SFFFE0 Timer A Channel 3 Vector (Low) SFFF6 Timer A Channel 3 Vector (Low) SFFF6 Timer A Channel 1 Vector (Low) SFFF6 Timer A Channel 1 Vector (Low) SFFF6 Timer A Channel 1 Vector (Low) SFFF6 PLL Vector (Low) SFFF6 PLL Vector (Low) SFFF6 Timer A Channel 1 Vector (Low) SFFF6 PLL Vector (High) SFFF7 Programmable Interrupt Timer (High) SFFF7 Re IRQ Vector (High) SFFF7 Re IRQ Vector (High) SFFF6 Reset Vector (High) SFFF6 Reset Vector (High)	Vector Priority	Address	Vector
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\$FFE9 Timer B Channel 1 Vector (Low) \$FFEA Timer B Channel 0 Vector (High) \$FFEB Timer B Channel 0 Vector (Low) \$FFEC Timer A Overflow Vector (Low) \$FFED Timer A Overflow Vector (Low) \$FFEE Timer A Channel 3 Vector (High) \$FFEE Timer A Channel 3 Vector (High) \$FFFE Timer A Channel 2 Vector (High) \$FFF70 Timer A Channel 2 Vector (Low) \$FFF71 Timer A Channel 1 Vector (Low) \$FFF72 Timer A Channel 1 Vector (Low) \$FFF73 Timer A Channel 1 Vector (Low) \$FFF74 Timer A Channel 0 Vector (Low) \$FFF75 Timer A Channel 0 Vector (Low) \$FFF76 Programmable Interrupt Timer (High) \$FFF77 Programmable Interrupt Timer (Low) \$FFF78 PLL Vector (Low) \$FFF79 PLL Vector (Low) \$FFF78 IRQ Vector (High) \$FFF79 PLL Vector (Low) \$FFF70 SWI Vector (Low) \$FFF78 IRQ Vector (Low) \$FFF79 SWI Vector (Low) \$FFF60 SWI Vector (Low) \$FFF78 IRQ Vector (H		\$FFE7	Timer B Overflow Vector (Low)
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\$FFEE Timer A Channel 3 Vector (High) \$FFEF Timer A Channel 3 Vector (Low) \$FFF0 Timer A Channel 2 Vector (High) \$FFF1 Timer A Channel 2 Vector (Low) \$FFF2 Timer A Channel 1 Vector (Low) \$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (Low) \$FFF8 PLL Vector (Low) \$FFF9 PLL Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF8 IRQ Vector (Low) \$FFF9 SWI Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF8 IRQ Vector (High) \$FFF6 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF8 Reset Vector (High)		\$FFEC	Timer A Overflow Vector (High)
\$FFEF Timer A Channel 3 Vector (Low) \$FFF0 Timer A Channel 2 Vector (High) \$FFF1 Timer A Channel 2 Vector (Low) \$FFF2 Timer A Channel 1 Vector (Low) \$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (Low) \$FFF78 PLL Vector (Low) \$FFF79 PLL Vector (Low) \$FFF78 IRQ Vector (Low) \$FFF79 PLL Vector (Low) \$FFF76 SWI Vector (Low) \$FFF70 SWI Vector (Low) \$FFF76 Reset Vector (High)		\$FFED	Timer A Overflow Vector (Low)
\$FFF0 Timer A Channel 2 Vector (High) \$FFF1 Timer A Channel 2 Vector (Low) \$FFF2 Timer A Channel 1 Vector (High) \$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (Low) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (Low) \$FFF9 PLL Vector (Low) \$FFF6 IRQ Vector (Low) \$FFF7 SWI Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF7 Reset Vector (High)		\$FFEE	Timer A Channel 3 Vector (High)
\$FFF1 Timer A Channel 2 Vector (Low) \$FFF2 Timer A Channel 1 Vector (High) \$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFF7 IRQ Vector (Low) \$FFF8 IRQ Vector (Low) \$FFF5 SWI Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 Reset Vector (Low)		\$FFEF	Timer A Channel 3 Vector (Low)
\$FFF2 Timer A Channel 1 Vector (High) \$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 IRQ Vector (Low) \$FFF5 IRQ Vector (Low) \$FFF6 SWI Vector (Low) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (High)		\$FFF0	Timer A Channel 2 Vector (High)
\$FFF3 Timer A Channel 1 Vector (Low) \$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (Low) \$FFFB IRQ Vector (Low) \$FFFFD SWI Vector (Low) \$FFFFD SWI Vector (Low) \$FFFFE Reset Vector (High)		\$FFF1	Timer A Channel 2 Vector (Low)
\$FFF4 Timer A Channel 0 Vector (High) \$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFF8 IRQ Vector (Low) \$FFF6 IRQ Vector (Low) \$FFF7 SWI Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 SWI Vector (Low) \$FFF6 SWI Vector (Low) \$FFF7 Reset Vector (High)		\$FFF2	Timer A Channel 1 Vector (High)
\$FFF5 Timer A Channel 0 Vector (Low) \$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (High) \$FFFB IRQ Vector (Low) \$FFFFD SWI Vector (Low) \$FFFFD SWI Vector (Low) \$FFFFE Reset Vector (High)		\$FFF3	Timer A Channel 1 Vector (Low)
\$FFF6 Programmable Interrupt Timer (High) \$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (High) \$FFFB IRQ Vector (Low) \$FFFC SWI Vector (Low) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (Low)		\$FFF4	Timer A Channel 0 Vector (High)
\$FFF7 Programmable Interrupt Timer (Low) \$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (High) \$FFFB IRQ Vector (Low) \$FFFC SWI Vector (Low) \$FFFD SWI Vector (Low) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (High)		\$FFF5	Timer A Channel 0 Vector (Low)
\$FFF8 PLL Vector (High) \$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (High) \$FFFB IRQ Vector (Low) \$FFFC SWI Vector (High) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (Low) \$FFFE Reset Vector (High)		\$FFF6	Programmable Interrupt Timer (High)
\$FFF9 PLL Vector (Low) \$FFFA IRQ Vector (High) \$FFFB IRQ Vector (Low) \$FFFC SWI Vector (High) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (Low) \$FFFE Reset Vector (High)		\$FFF7	Programmable Interrupt Timer (Low)
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SFFFB IRQ Vector (Low) \$FFFC SWI Vector (High) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (High)		\$FFF9	PLL Vector (Low)
\$FFFC SWI Vector (High) \$FFFD SWI Vector (Low) \$FFFE Reset Vector (High)		\$FFFA	IRQ Vector (High)
\$FFFD SWI Vector (Low) \$FFFE Reset Vector (High)		\$FFFB	IRQ Vector (Low)
Highest \$FFFE Reset Vector (High)	↓	\$FFFC	SWI Vector (High)
HIDDEST	V	\$FFFD	SWI Vector (Low)
\$FFFF Reset Vector (Low)	Highost	\$FFD5SCI Transmit Vector (Low)\$FFD6SCI Receive Vector (High)\$FFD7SCI Receive Vector (Low)\$FFD8SCI Error Vector (Low)\$FFD9SCI Error Vector (Low)\$FFD9SCI Error Vector (Low)\$FFD0Reserved\$FFD0Reserved\$FFD0Reserved\$FFD1Timer B Channel 3 Vector (High)\$FF07Timer B Channel 3 Vector (Loc\$FF07Timer B Channel 2 Vector (Loc\$FF18Timer B Channel 2 Vector (Loc\$FF20SPI Transmit Vector (Low)\$FF21SPI Transmit Vector (Low)\$FF23SPI Transmit Vector (Low)\$FF44SPI Receive Vector (Low)\$FF55SPI Receive Vector (Low)\$FF56Timer B Overflow Vector (Low)\$FF57Timer B Channel 1 Vector (Low)\$FF58Timer B Channel 1 Vector (Low)\$FF58Timer B Channel 1 Vector (Low)\$FF59Timer A Channel 0 Vector (Low)\$FF51Timer A Channel 3 Vector (Low)\$FF52Timer A Channel 3 Vector (Low)\$FF54Timer A Channel 3 Vector (Low)\$FF55Timer A Channel 3 Vector (Low)\$FF76Timer A Channel 3 Vector (Low)\$FF77Programmable Interrupt Time\$FF73Timer A Channel 1 Vector (Low)\$FF74Timer A Channel 1 Vector (Low)\$FF75Timer A Channel 0 Vector (Low)\$FF76Programmable Interrupt Time\$FF79PLL Vector (Low)\$FF78PLL Vector (Low) <trr>\$FF79SWI Vector (Hig</trr>	Reset Vector (High)
	nignest	\$FFFF	Reset Vector (Low)

Table 2-1. Vector Addresses



Central Processor Unit (CPU)

Source Form	Operation	Description	Effect CC				on		Address Mode	Opcode	Operand	es
, on the second se			v	н	I	Ν	z	С	bod Mod	Opc	Ope	Cycles
EOR #opr EOR opr EOR opr,X EOR opr,X EOR ,X EOR ,X EOR opr,SP EOR opr,SP	Exclusive OR M with A	A ← (A ⊕ M)		_	_	\$	\$	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh II ee ff ff ee ff	2 3 4 3 2 4 5
INC opr INCA INCX INC opr,X INC ,X INC opr,SP	Increment	$\begin{split} M \leftarrow (M) + 1 \\ A \leftarrow (A) + 1 \\ X \leftarrow (X) + 1 \\ M \leftarrow (M) + 1 \end{split}$	\$	_	_	\$	\$	_	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 4 3 5
JMP opr JMP opr JMP opr,X JMP opr,X JMP ,X	Jump	PC ← Jump Address	_	_	_	_	_	_	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh II ee ff ff	2 3 4 3 2
JSR opr JSR opr JSR opr,X JSR opr,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) - 1 Push (PCH); SP ← (SP) - 1 PC ← Unconditional Address	_	_	_	_	_	_	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh II ee ff ff	4 5 6 5 4
LDA #opr LDA opr LDA opr LDA opr,X LDA opr,X LDA ,X LDA opr,SP LDA opr,SP	Load A from M	A ← (M)		_	_	\$	\$	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh II ee ff ff ee ff	2 3 4 3 2 4 5
LDHX #opr LDHX opr	Load H:X from M	H:X ← (M:M + 1)	0	-	-	€	€	_	IMM DIR	45 55	ii jj dd	3 4
LDX #opr LDX opr LDX opr LDX opr,X LDX opr,X LDX ,X LDX opr,SP LDX opr,SP	Load X from M	X ← (M)	0	_	_	€	\$	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh II ee ff ff ee ff	2 3 4 3 2 4 5
LSL opr LSLA LSLX LSL opr,X LSL ,X LSL opr,SP	Logical Shift Left (Same as ASL)		¢	_	_	¢	\$	\$	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 4 3 5

Table 7-1. Instruction Set Summary (Continued)



Clock Generator Module (CGM)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
		ad: PLLIE	PLLF	PLLON	BCS	1	1	1	1
\$001C	PLL Control Register (PCTL) Wr	ite:		1 LLOIN	200				
	Res	set: 0	0	1	0	1	1	1	1
	Re PLL Bandwidth Control	ad: AUTO	LOCK	ACQ	XLD	0	0	0	0
\$001D	Register Wr								
	(PBWC) Res	set: 0	0	0	0	0	0	0	0
	Re PLL Programming	ad: MUL7	MUL6	MUL5	MUL4	VRS7	VRS6	VRS5	VRS4
\$001E	Register Wr (PPG)	ite:							
	Re	set: 0	1	1	0	0	1	1	0
			= Unimple	mented					

NOTES:

1. When AUTO = 0, PLLIE is forced to logic zero and is read-only.

- 2. When AUTO = 0, PLLF and LOCK read as logic zero.
- 3. When AUTO = 1, \overline{ACQ} is read-only.
- 4. When PLLON = 0 or VRS[7:4] = \$0, BCS is forced to logic zero and is read-only.
- 5. When PLLON = 1, the PLL programming register is read-only.
- 6. When BCS = 1, PLLON is forced set and is read-only.

Figure 9-4. CGM I/O Register Summary

9.6.1 PLL Control Register (PCTL)

The PLL control register contains the interrupt enable and flag bits, the on/off switch, and the base clock selector bit.

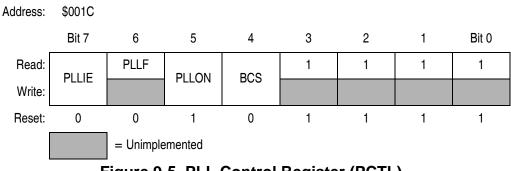


Figure 9-5. PLL Control Register (PCTL)

Technical Data

Clock Generator Module (CGM)

The crystal loss detect function works only when the BCS bit is set, selecting CGMVCLK to drive CGMOUT. When BCS is clear, XLD always reads as 0.

Bits [3:0] — Reserved for test

These bits enable test functions not available in user mode. To ensure software portability from development systems to user applications, software should write zeros to Bits [3:0] whenever writing to PBWC.

9.6.3 PLL Programming Register (PPG)

The PLL programming register contains the programming information for the modulo feedback divider and the programming information for the hardware configuration of the VCO.

Address: \$001E

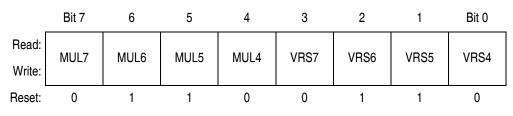


Figure 9-8. PLL Programming Register (PPG)

MUL[7:4] - Multiplier Select Bits

These read/write bits control the modulo feedback divider that selects the VCO frequency multiplier, N. (See 9.4.2.1 PLL Circuits and 9.4.2.4 Programming the PLL). A value of \$0 in the multiplier select bits configures the modulo feedback divider the same as a value of \$1. Reset initializes these bits to \$6 to give a default multiply value of 6.



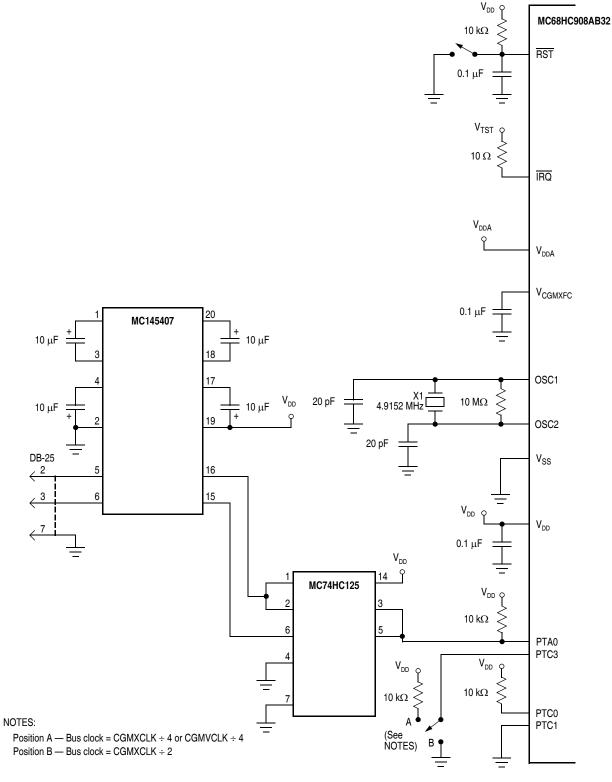


Figure 10-1. Monitor Mode Circuit

Monitor ROM (MON)

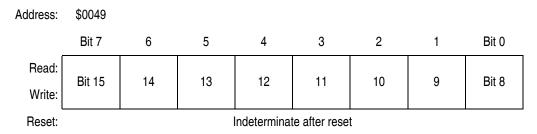
Description	Write byte to memory					
Operand	Operand Specifics 2-byte address in high byte:low byte order; low byte followed by data byte					
Data Returned	None					
Opcode	\$49					
Command Sequence						
SENT TO MONITOR						
V WRITE V ADDRESS V ADDRES						

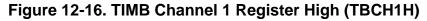
Table 10-4. WRITE (Write Memory) Command

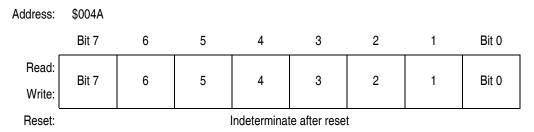
Table 10-5. IREAD (Indexed Read) Command

Description	Read next 2 bytes in memory from last address accessed				
Operand	Specifies 2-byte address in high byte:low byte order				
Data Returned	Returne contents of next two addresses				
Opcode	\$1A				
	Command Sequence				











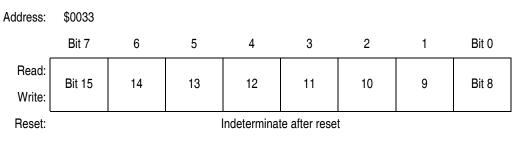






Figure 12-19. TIMB Channel 2 Register Low (TBCH2L)



bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at logic zero. After the break, doing the second step clears the status bit.

13.7 I/O Registers

The following I/O registers control and monitor operation of the PIT:

- PIT status and control register (PSC)
- PIT counter registers (PCNTH:PCNTL)
- PIT counter modulo registers (PMODH:PMODL)

13.7.1 PIT Status and Control Register

The PIT status and control register does the following:

- Enables PIT interrupt
- Flags PIT overflows
- Stops the PIT counter
- Resets the PIT counter
- Prescales the PIT counter clock

Address: \$004B

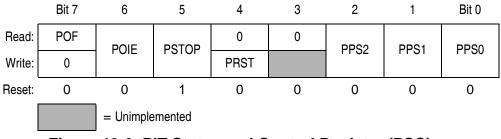


Figure 13-3. PIT Status and Control Register (PSC)



- Two receiver wakeup methods:
 - Idle line wakeup
 - Address mark wakeup
- Interrupt-driven operation with eight interrupt flags:
 - Transmitter empty
 - Transmission complete
 - Receiver full
 - Idle receiver input
 - Receiver overrun
 - Noise error
 - Framing error
 - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

Serial Communications Interface

TE — Transmitter Enable Bit

Setting this read/write bit begins the transmission by sending a preamble of 10 or 11 logic 1s from the transmit shift register to the PTE0/TxD pin. If software clears the TE bit, the transmitter completes any transmission in progress before the PTE0/TxD returns to the idle condition (logic 1). Clearing and then setting TE during a transmission queues an idle character to be sent after the character currently being transmitted. Reset clears the TE bit.

- 1 = Transmitter enabled
- 0 = Transmitter disabled
- **NOTE:** Writing to the TE bit is not allowed when the enable SCI bit (ENSCI) is clear. ENSCI is in SCI control register 1.
 - RE Receiver Enable Bit

Setting this read/write bit enables the receiver. Clearing the RE bit disables the receiver but does not affect receiver interrupt flag bits. Reset clears the RE bit.

- 1 = Receiver enabled
- 0 =Receiver disabled
- **NOTE:** Writing to the RE bit is not allowed when the enable SCI bit (ENSCI) is clear. ENSCI is in SCI control register 1.

RWU — Receiver Wakeup Bit

This read/write bit puts the receiver in a standby state during which receiver interrupts are disabled. The WAKE bit in SCC1 determines whether an idle input or an address mark brings the receiver out of the standby state and clears the RWU bit. Reset clears the RWU bit.

- 1 = Standby state
- 0 = Normal operation

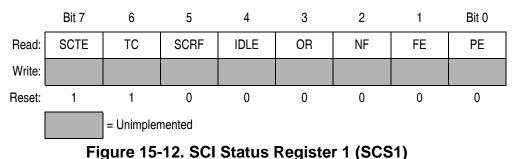


15.9.4 SCI Status Register 1

SCI status register 1 (SCS1) contains flags to signal these conditions:

- Transfer of SCDR data to transmit shift register complete
- Transmission complete
- Transfer of receive shift register data to SCDR complete
- Receiver input idle
- Receiver overrun
- Noisy data
- Framing error
- Parity error

Address: \$0016



SCTE — SCI Transmitter Empty Bit

This clearable, read-only bit is set when the SCDR transfers a character to the transmit shift register. SCTE can generate an SCI transmitter CPU interrupt request. When the SCTIE bit in SCC2 is set, SCTE generates an SCI transmitter CPU interrupt request. In normal operation, clear the SCTE bit by reading SCS1 with SCTE set and then writing to SCDR. Reset sets the SCTE bit.

1 = SCDR data transferred to transmit shift register

0 = SCDR data not transferred to transmit shift register

SCR2, SCR1, and SCR0	Baud Rate Divisor (BD)
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Table	15-7. 8	SCI Baud	Rate	Selection
-------	---------	----------	------	-----------

Use this formula to calculate the SCI baud rate:

baud rate =
$$\frac{\text{SCI clock source}}{64 \times \text{PD} \times \text{BD}}$$

where:

SCI clock source = CGMXCLK

(See 9.5.6 Crystal Output Frequency Signal (CGMXCLK).)

PD = prescaler divisor

BD = baud rate divisor

This makes the formula:

baud rate = $\frac{CGMXCLK}{64 \times PD \times BD}$

Table 15-8 shows the SCI baud rates that can be generated with a4.9152MHz CGMXCLK.



Section 16. Serial Peripheral Interface Module (SPI)

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16.2 Introduction

This section describes the serial peripheral interface (SPI) module, which allows full-duplex, synchronous, serial communications with peripheral devices.

16.3 Features

Features of the SPI module include the following:

- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four master mode frequencies (maximum = bus frequency ÷ 2)
- Maximum slave mode frequency = bus frequency
- Serial clock with programmable polarity and phase
- Two separately enabled interrupts:
 - SPRF (SPI receiver full)
 - SPTE (SPI transmitter empty)
- Mode fault error flag with CPU interrupt capability
- Overflow error flag with CPU interrupt capability
- Programmable wired-OR mode
- I²C (inter-integrated circuit) compatibility
- I/O (input/output) port bit(s) software configurable with pullup device(s) if configured as input port bit(s)

17.3 Port A

Port A is an 8-bit general-purpose bidirectional I/O port.

17.3.1 Port A Data Register (PTA)

The port A data register contains a data latch for each of the eight port A pins.



	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Reset:	Unaffected by Reset							

Figure 17-2. Port A Data Register (PTA)

PTA[7:0] - Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

17.3.2 Data Direction Register A (DDRA)

Data direction register A determines whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

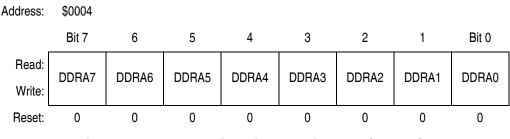


Figure 17-3. Data Direction Register A (DDRA)

17.7 Port E

Port E is an 8-bit special function port that shares two of its pins with the timer interface module (TIMA), two of its pins with the serial communications interface module (SCI) and four of its pins with the serial peripheral interface module (SPI).

17.7.1 Port E Data Register (PTE)

The port E data register contains a data latch for each of the eight port E pins.

Address:	\$0008							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0
Reset:	Unaffected by reset							
Alternative Function:	SPSCK	MOSI	MISO	SS	TACH1	TACH0	RxD	TxD
Figure 47.45 Deet 5 Dete Desister (DT5)								

Figure 17-15. Port E Data Register (PTE)

PTE[7:0] - Port E Data Bits

These read/write bits are software programmable. Data direction of each port E pin is under the control of the corresponding bit in data direction register E. Reset has no effect on port E data.

SPSCK — SPI Serial Clock

The PTE7/SPSCK pin is the serial clock input of a SPI slave module and serial clock output of a SPI master modules. When the SPE bit is clear, the PTE7/SPSCK pin is available for general-purpose I/O. See **16.14.1 SPI Control Register**.

MOSI — Master Out/Slave In

The PTE6/MOSI pin is the master out/slave in terminal of the SPI module. When the SPE bit is clear, the PTE6/MOSI pin is available for general-purpose I /O. See **16.14.1 SPI Control Register**.

Technical Data

Input/Output (I/O) Ports

17.8.3 Port F Input Pullup Enable Register (PTFPUE)

The port F input pullup enable register (PTFPUE) controls the input pullup device for each of the eight port F pins. Each bit is individually configurable and requires that the data direction register, DDRF, bit be configured as an input. Each pullup is automatically and dynamically disabled when a port bit's DDRF is configured for output mode.

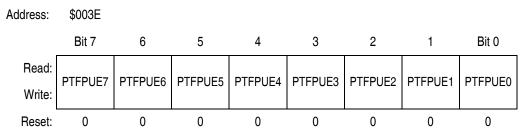


Figure 17-21. Port F Input Pullup Enable Register (PTFPUE)

PTFPUE[7:0] — Port F Input Pullup Enable Bits

These writable bits are software programmable to enable pullup devices on an input port pin.

1 = Corresponding port F pin configured to have internal pullup

0 = Corresponding port F pin internal pullup disconnected

17.9 Port G

Port G is a 3-bit special-function port that shares all three of its pins with the keyboard interrupt (KBI) module.

17.9.1 Port G Data Register (PTG)

The port G data register (PTG) contains a data latch for each of the three port G pins.

DDRG[2:0] — Data Direction Register G Bits

These read/write bits control port G data direction. Reset clears DDRG[2:0], configuring all port G pins as inputs.

- 1 = Corresponding port G pin configured as output
- 0 = Corresponding port G pin configured as input
- **NOTE:** Avoid glitches on port G pins by writing to the port G data register before changing data direction register G bits from 0 to 1. Figure 17-24 shows the port G I/O logic.

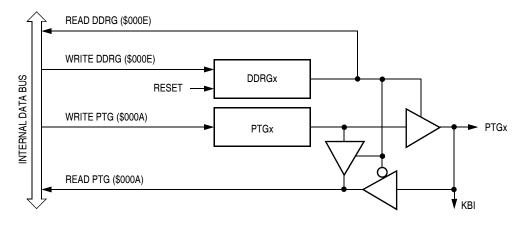


Figure 17-24. Port G I/O Circuit

When DDRGx is a logic 1, reading address \$000A reads the PTGx data latch. When DDRGx is a logic 0, reading address \$000A reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

 Table 17-6 summarizes the operation of the port G pins.

 Table 17-8. Port G Pin Functions

DDRG Bit	PTG Bit	I/O Pin Mode	Accesses to DDRG	Accesses to PTG		
Bit		Mode	Read/Write	Read	Write	
0	X ⁽¹⁾	Input, Hi-Z ⁽²⁾	DDRG[2:0]	Pin	PTG[2:0] ⁽³⁾	
1	Х	Output	DDRG[2:0]	PTG[2:0]	PTG[2:0]	

Notes:

1. X = don't care.

2. Hi-Z = high impedance.

3. Writing affects data register, but does not affect the input.

Technical Data

Break Module (BRK)

22.6.4 SIM Break Flag Control Register

The SIM break flag control register (SBFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: \$FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BCFE	R	R	R	R	R	R	R
Write:	b		11					
Reset:	0							
	R	= Reserved	1					

Figure 22-7. SIM Break Flag Control Register (SBFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break