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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	16
Voltage - Supply	5.5V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	54-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e624acdwb

INTERNAL BLOCK DIAGRAM

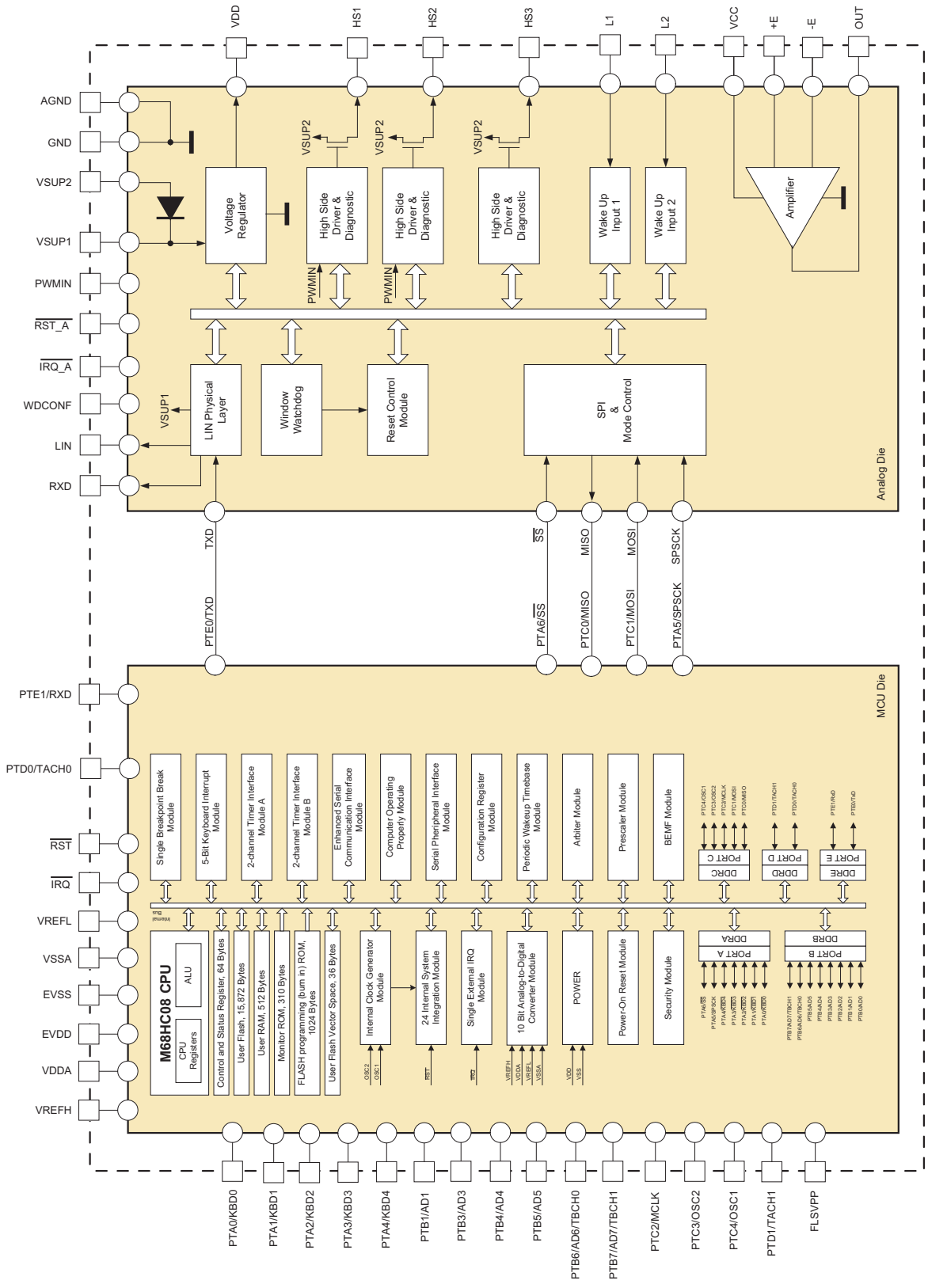


Figure 2. 908E624 Simplified Internal Block Diagram

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Die	Pin	Pin Name	Formal Name	Definition
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	17	PWMIN	Direct High Side Control Input	This pin allows the enabling and PWM control of the high side HS1 and HS2 pins.
Analog	18	RST_A	Internal Reset Output	This pin is the reset output pin of the analog die.
Analog	19	IRQ_A	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	23 24	L1 L2	Wake-Up Inputs	These pins are the wake-up inputs of the analog chip.
Analog	25 26 27	HS3 HS2 HS1	High Side Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	31 28	VSUP1 VSUP2	Power Supply Pins	These pins are device power supply pins.
Analog	29	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	30 34	GND AGND	Power Ground Pins	These pins are device power ground connections.
Analog	33	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	35	VCC	Amplifier Power Supply	This pin is the single +5.0 V power supply for the current sense operational amplifier.
Analog	36	OUT	Amplifier Output	This pin is the output of the current sense operational amplifier.
Analog	37 38	-E +E	Amplifier Inputs	These pins are the current sense operational amplifier inverted and non-inverted inputs.
Analog	39	WDCONF	Window Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
Analog	40	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 27 -0.3 to 40 -0.3 to 5.5	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to V_{DD}+0.3 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins except VDD, VSS, PTA0:PTA6, PTC0:PTC1 PTA0:PTA6, PTC0:PTC1 Pins	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
Current Sense Operational Amplifier Maximum Input Voltage, +E, -E Pins Maximum Input Current, +E, -E Pins Maximum Output Voltage, OUT Pin Maximum Output Current, OUT Pin	 V_{+E-E} I_{+E-E} V_{OUT} I_{OUT}	 -0.3 to 7.0 ±20 -0.3 to V_{CC}+0.3 ±20	 V mA V mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 13)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
L1 and L2 Pin Voltage Normal Operation with a 33 kΩ resistor (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 13)	 $V_{WAKE(SS)}$ $V_{WAKE(PK)}$	 -18 to 40 -100 to 100	V
ESD Voltage Human Body Model (1) Machine Model (1) Charge Device Model (1)	 V_{ESD1} V_{ESD2} V_{ESD3}	 ±2000 ±100 ±500	V

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Package Operating Ambient Temperature [4] MM908E624ACPEW MM908E624AYPEW	T_A	 -40 to 85 -40 to 125	°C
Operating Junction Temperature [2][4] MM908E624ACPEW MM908E624AYPEW	T_J	 -40 to 125 -40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[3][5]	T_{PPRT}	Note 5	°C

Notes

2. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation of the analog die. The analog die junction temperature must not exceed 150°C under these conditions.
3. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Independent of T_A, device parametrics are only guaranteed for -40 < T_J < 125 °C. Please see note 2. T_J is a factor of power dissipation, package thermal resistance, and available heat sinking.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low-voltage Reset (LVR) Threshold	V_{LVRON}	3.6	4.0	4.4	V
Low-voltage Interrupt (LVI) Threshold Hysteresis	 V_{LVI} V_{LVI_HYS}	 5.7 —	 6.0 1.0	 6.6 —	V
High-voltage Interrupt (HVI) Threshold Hysteresis	 V_{HVI} V_{HVI_HYS}	 18 —	 19.25 220	 20.5 —	 V mV
VOLTAGE REGULATOR (10)					
Normal Mode Output Voltage 2.0 mA < I_{DD} < 50 mA, 5.5 V < V_{SUP} < 27 V	V_{DDRUN}	4.75	5.0	5.25	V
Normal Mode Output Current Limitation (11)	I_{DDRUN}	50	110	200	mA
Dropout Voltage V_{SUP} = 4.9 V, I_{DD} = 50 mA	V_{DDDROP}	—	0.1	0.2	V
Stop Mode Output Voltage (12)	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Regulator Current Limitation	I_{DDSTOP}	4.0	8.0	14	mA
Line Regulation Normal Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA Stop Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	 V_{LRRUN} V_{LRSTOP}	 — —	 20 10	 150 100	mV
Load Regulation Normal Mode, 1.0 mA < I_{DD} < 50 mA, V_{SUP} = 18 V Stop Mode, 1.0 mA < I_{DD} < 5.0 mA, V_{SUP} = 18 V	 V_{LRRUN} V_{LDSTOP}	 — —	 40 40	 150 150	mV
Over-temperature Prewarning (Junction) (13)	T_{PRE}	120	135	160	°C
Thermal Shutdown Temperature (Junction) (13)	T_{SD}	155	170	—	°C
Temperature Threshold Difference T_{SD}-T_{PRE}	ΔT_{SD}-T_{PRE}	20	30	45	°C

Notes

10. Specification with external capacitor 2.0 μF< C < 10 μF and 200 mΩ ≤ ESR ≤ 10 Ω. Capacitor value up to 47 μF can be used.
11. Total V_{DD} regulator current. A 5.0 mA current for current sense operational amplifier is included. Digital output supplied from VDD.
12. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.
13. This parameter is guaranteed by process monitoring but not production tested

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUT HS3					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25 °C, I_{LOAD} = 50 m A, V_{SUP} > 9.0 V		—	—	7.0	
T_J = 125 °C, I_{LOAD} = 50 mA, V_{SUP} > 9.0 V		—	—	10	
T_J = 125 °C, I_{LOAD} = 30 mA, 5.5 V < V_{SUP} > 9.0 V		—	—	14	
Output Current Limitation	I_{LIM}	60	100	200	mA
Over-temperature Shutdown (17), (18)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	µA
CURRENT SENSE OPERATIONAL AMPLIFIER					
Rail-to-Rail Input Voltage	V_{IMC}	-0.1	—	V_{CC}+0.1	V
Output Voltage Range					V
Output Current ±1.0 mA	V_{OUT1}	0.1	—	V_{CC}-0.1	
Output Current ±5.0 mA	V_{OUT2}	0.3	—	V_{CC}-0.3	
Input Bias Current	I_B	—	—	250	nA
Input Offset Current	I_O	-100	—	100	nA
Input Offset Voltage	V_{IO}	-25	—	25	mV
L1 AND L2 INPUTS					
Low Detection Threshold	V_{THL}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
High Detection Threshold	V_{THH}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.5	—	1.3	
Input Current	I_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	

Notes
17. This parameter is guaranteed by process monitoring but it is not production tested
18. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate (19), (20)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1	-10.44	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2	—	—	11	µs
Driver Characteristics for Slow Slew Rate (19), (21)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1S	-22	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2S	—	—	23	µs
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	15	—	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay (22)	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay (22)	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	$t_{PROP}WL$	35	—	150	µs
Bus Wake-up Event Reported (23)	t_{WAKE}	—	20	—	µs

Notes

19. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
20. See Figure 6, page 14.
21. See Figure 7, page 14.
22. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
23. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 8 and Figure 9, page 15. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD pin.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER (CONTINUED)					
Output Current Shutdown Delay	$t_{OV-DELAY}$	—	10	—	µs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	f_{SPIOP}	0.25	—	4.0	MHz
L1 AND L2 INPUTS					
Wake-up Filter Time (24)	t_{WUF}	8.0	20	38	µs
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
Watchdog Period	t_{PWD}				ms
External Resistor R_{EXT} = 10 kΩ (1%)		—	10.558	—	
External Resistor R_{EXT} = 100 kΩ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Pin Open)		97	150	205	
STATE MACHINE TIMING					
Reset Low Level Duration after V_{DD} High (28)	$t_{\overline{RST}}$	0.65	1.0	1.35	ms
Interrupt Low Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Normal Request Mode Timeout (28)	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On (25), (26)	t_{S-HSON}	—	3.0	10	µs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off (25), (26)	$t_{S-HSOFF}$	—	3.0	10	µs
Delay Between Normal Request and Normal Mode After W/D Trigger Command (27)	t_{S-NR2N}	6.0	35	70	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and Normal Request Mode (VDD On and Reset High)	$t_{W-\overline{SS}}$	15	40	80	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and First Accepted SPI Command	t_{W-SPI}	90	—	N/A	µs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{S-1STSPI}$	30	—	N/A	µs
Minimum Time Between Two Rising Edges on $\overline{SS}$	$t_{2\overline{SS}}$	15	—	—	µs

Notes
24. This parameter is guaranteed by process monitoring but is not production tested.
25. Delay between turn-on or turn-off command and high side on or high side off, excluding rise or fall time due to external load.
26. Delay between the end of the SPI command (rising edge of the $\overline{SS}$) and start of device activation/deactivation.
27. This parameter is guaranteed by process monitoring but it is not production tested.
28. Also see Figure 10 on page 15

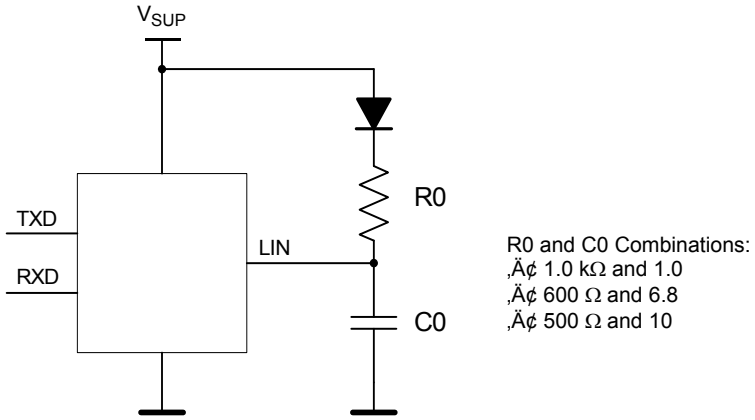


Figure 5. Test Circuit for LIN Timing Measurements

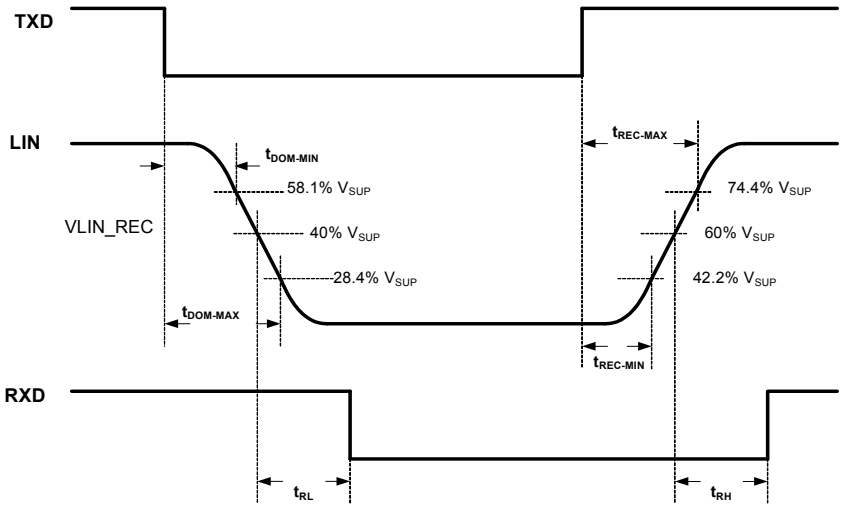


Figure 6. LIN Timing Measurements for Normal Slew Rate

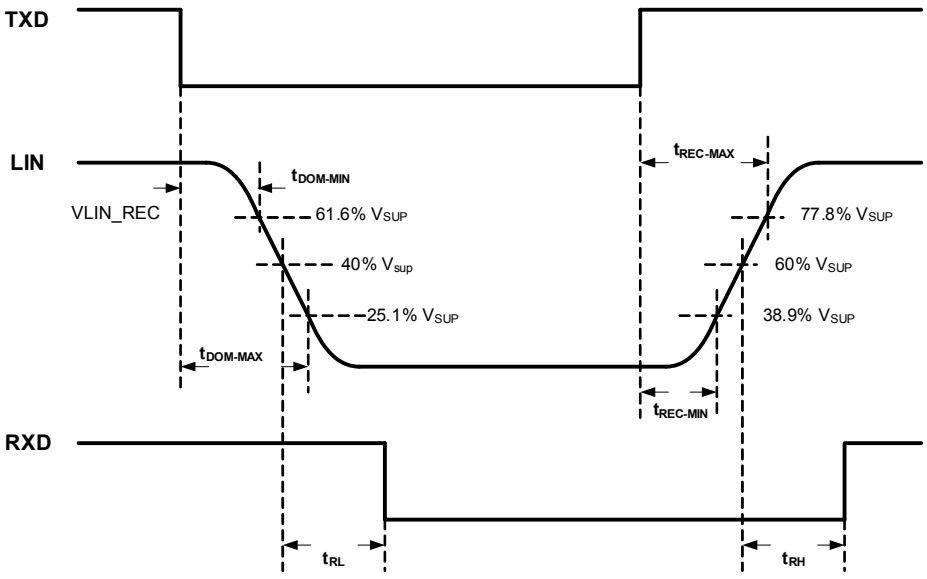


Figure 7. LIN Timing Measurements for Slow Slew Rate

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E624 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E624 is well suited to perform relay control in applications like window lift, sunroof, etc., via a three-wire LIN bus.

The device combines an HC908EY16 MCU core with flash memory together with a *SmartMOS* IC chip. The *SmartMOS* IC chip combines power and control in one chip. Power switches are provided on the *SmartMOS* IC configured as high side outputs. Other ports are also provided, which include a current sense operational amplifier port and two wake-up pins. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Figure 1, 908E624 Simplified Application Diagram, page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details, refer to the 68HC908EY16 data sheet.

PORT B I/O PINS (PTB1:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

The PTB0/AD0 and PTB2/AD2 pins are not accessible in this device.

For details, refer to the 68HC908EY16 data sheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details, refer to the 68HC908EY16 data sheet.

PORT D I/O PINS (PTD:0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

For details, refer to the 68HC908EY16 data sheet.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

Important To ensure proper operation, do not add any external pull-up resistor.

For details, refer to the 68HC908EY16 data sheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins, respectively. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 data sheet.

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	$\overline{\text{RST\_A}}$ Output	Watchdog Function	HS1, HS2, and HS3	LIN Interface	Sense Amplifier
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Recessive only	Not active
Normal Request	V_{DD} ON	N/A	HIGH	150 ms time out if WD enabled	Enabled	Transmit and receive	Not active
Normal (Run)	V_{DD} ON	N/A	HIGH	Window WD if enabled	Enabled	Transmit and receive	Active
Stop	V_{DD} ON with limited current capability	LIN wake-up, L1, L2 state change, $\overline{\text{SS}}$ rising edge	HIGH	Disabled	Disabled	Recessive state with wake-up capability	Not active
Sleep	V_{DD} OFF	LIN wake-up L1, L2 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability	Not active

INTERRUPTS

In Normal (Run) mode the 908E624 has four different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ pin is generated to report a fault to the MCU. All interrupts are not maskable and cannot be disabled.

After an Interrupt the INTSRC bit in the SPI Status register is set, indicating the source of the event. This interrupt source information is only transferred once, and the INTSRC bit is cleared automatically.

Low-Voltage Interrupt

Low-voltage interrupt (LVI) is related to external supply voltage VSUP1. If this voltage falls below the LVI threshold, it will set the LVF bit in the SPI Status register and an interrupt will be initiated. The LVF bit remains set as long as the Low-voltage condition is present.

During Sleep and Stop mode the low-voltage interrupt circuitry is disabled.

High-voltage Interrupt

High-voltage interrupt (HVI) is related to external supply voltage VSUP1. If this voltage rises above the HVI threshold, it will set the HVF bit in the SPI Status register and an interrupt will be initiated. The HVF bit remains set as long as the high-voltage condition is present.

During Sleep and Stop mode the high-voltage interrupt circuitry is disabled.

Wake-up Interrupts

In Stop mode the $\overline{\text{IRQ\_A}}$ pin reports wake-up events on the L1, L2, or the LIN bus to the MCU. All wake-up interrupts are not maskable and cannot be disabled.

After a wake-up interrupt, the INTSRC bit in the Serial Peripheral Interface (SPI) Status register is set, indicating the source of the event. This wake-up source information is only transferred once, and the INTSRC bit is cleared automatically.

Figure 12, page 21, describes the Stop/Wake-up procedure.

Voltage Regulator Temperature Prewarning (VDDT)

Voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Status register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop mode the voltage regulator temperature prewarning circuitry is disabled.

High Side Switch Thermal Shutdown (HSST)

The high side switch thermal shutdown HSST is generated if one of the high side switches HS1:HS3 is above the HSST threshold, it will shutdown all high side switches, set the HSST flag in the SPI Status register and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present.

During Sleep and Stop mode the high side switch thermal shutdown circuitry is disabled.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled in Normal and Normal Request mode.

An over-current condition (e.g. LIN bus short to V_{BAT}) or a over-temperature in the output low side FET will shutdown the transmitter and set the LINFAIL flag in the SPI Status Register.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN pin can be disconnected, with the LIN-PU bit in the SPI Control Register, and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

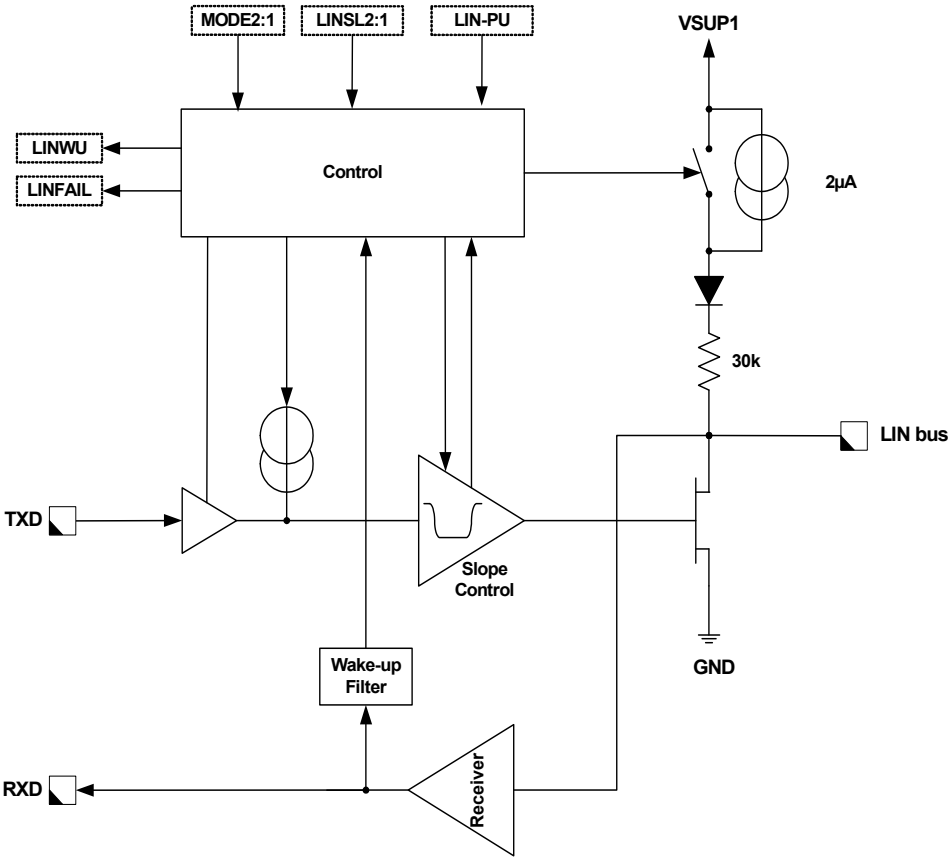


Figure 15. LIN Interface

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see Figure 2, page 2). When TXD is LOW, the LIN pin is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD pin has an internal pull-up current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a wake-up interrupt and set the LINWF flag in the SPI Status Register. Also see Figure 9, page 15.

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is

disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register. Also see Figure 8, page 15).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF pin. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to Table 8, page 26).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST\_A}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

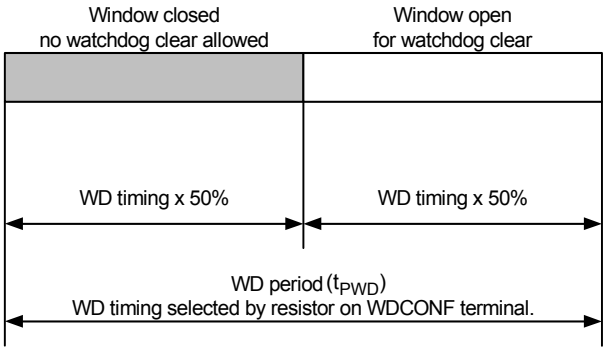


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF pin must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD}\ [ms] = 0.991 * R_{EXT}\ [k\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Over-current) Protection

The voltage regulator has current limit to protect the device against over-current and short-circuit conditions.

Over-temperature Protection

The voltage regulator also features an over-temperature protection having an over-temperature warning (Interrupt - VDDT) and an over-temperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease of use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25%, due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at the address $FDC2. After trimming the ICG, a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 µF) V_{DD} = 5.0 V, $T_{Ambient}$~23 °C) and will vary over-temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values must be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

Table 7. SPI Register Overview

Read/Write Information	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
Write	LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
Read	INTSRC (30)	LINWU or LINFAIL	HVF	LVF or BATFAIL (31)	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes
30. D7 signals interrupts and wake-up interrupts, D6:D0 indicated the source.
31. The first SPI read after reset returns the BATFAIL flag state on bit D4.

SPI Control Register (Write)

Table 8 shows the SPI Control register bits by name.

Table 8. Control Bits Function (Write Operation)

D7	D6	D5	D4	D3	D2	D1	D0
LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1

LINSL2:1—LIN Baud Rate and Low-power Mode Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 9. Reset clears the LINSL2:1 bits.

Table 9. LIN Baud Rate and Low-power Mode Selection Bits

LINSL2	LINSL1	Description
0	0	Baud Rate up to 20 kbps (normal)
0	1	Baud Rate up to 10 kbps (slow)
1	0	Fast Program Download Baud Rate up to 100 kbps
1	1	Low-power Mode (Sleep or Stop) Request

LIN-PU—LIN Pull-up Enable Bit

This bit controls the LIN pull-up resistor during Sleep and Stop modes.

- 1 = Pull-up disconnected in Sleep and Stop modes.
- 0 = Pull-up connected in Sleep and Stop modes.

If the Pull-up is disconnected, a small current source is used to pull the LIN pin in recessive state. In case of an erroneous short of the LIN bus to ground, this will significantly reduce the power consumption, e.g. in combination with STOP/SLEEP mode.

HS3ON:HS1ON—High Side H3:HS1 Enable Bits

These bits enable the HSx. Reset clears the HSxON bit.

- 1 = HSx switched on (refer to Note below).
- 0 = HSx switched off.

Note If no PWM on HS1 and HS2 is required, the PWMIN pin must be connected to the VDD pin.

MODE2:1—Mode Section Bits

The MODE2:1 bits control the operating modes and the watchdog in accordance with Table 10.

Table 10. Mode Selection Bits

MODE2	MODE1	Description
0	0	Sleep Mode (32)
0	1	Stop Mode (32)
1	0	Watchdog Clear (33)
1	1	Run (Normal) Mode

Notes
32. To enter Sleep and Stop mode, a special sequence of SPI commands is implemented.
33. The device stays in Run (Normal) mode.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence

The Sleep command, as shown in Table 11, must be sent twice.

Table 11. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	0

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale website: www.freescale.com.

VSUP Pins (VSUP1 and VSUP2)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN Pin

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) it is recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU Digital Supply Pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU Analog Supply Pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins it is important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 20 and Figure 21 show the recommendations on schematics and layout level and Table 15 indicates recommended external components and layout considerations.

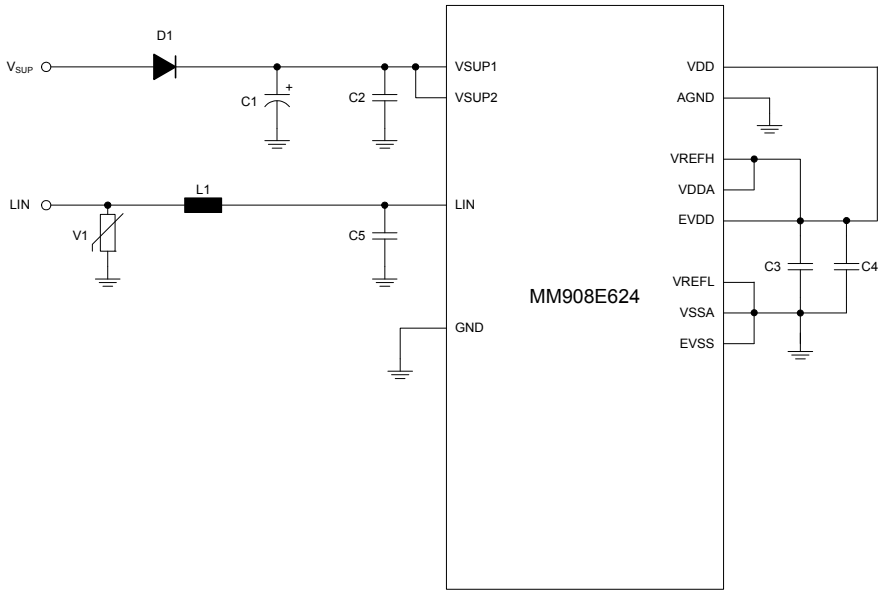


Figure 20. EMC/EMI Recommendations

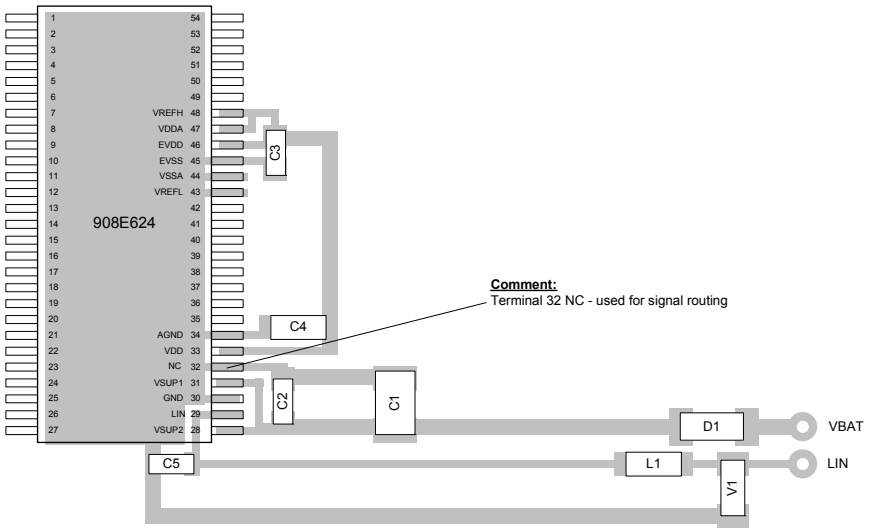


Figure 21. PCB Layout Recommendations

Table 15. Component Value Recommendation

Component	Recommended Value[39]	Comments / Signal routing
D1		Reverse battery protection
C1	Bulk Capacitor	
C2	100 nF, SMD Ceramic	Close (<5.0 mm) to VSUP1, VSUP2 pins with good ground return
C3	100 nF, SMD Ceramic	Close (<3.0 mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4.7 µF, SMD Ceramic or Low ESR	Bulk Capacitor
C5	180 pF, SMD Ceramic	Close (<5.0 mm) to LIN pin. Total Capacitance per LIN node has to be below 220 pF. (C_{TOTAL} = $C_{LIN-PIN}$ + C5 + $C_{VARISTOR}$ ~ 10 pF + 180 pF + 15 pF)
V1[40]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[40]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

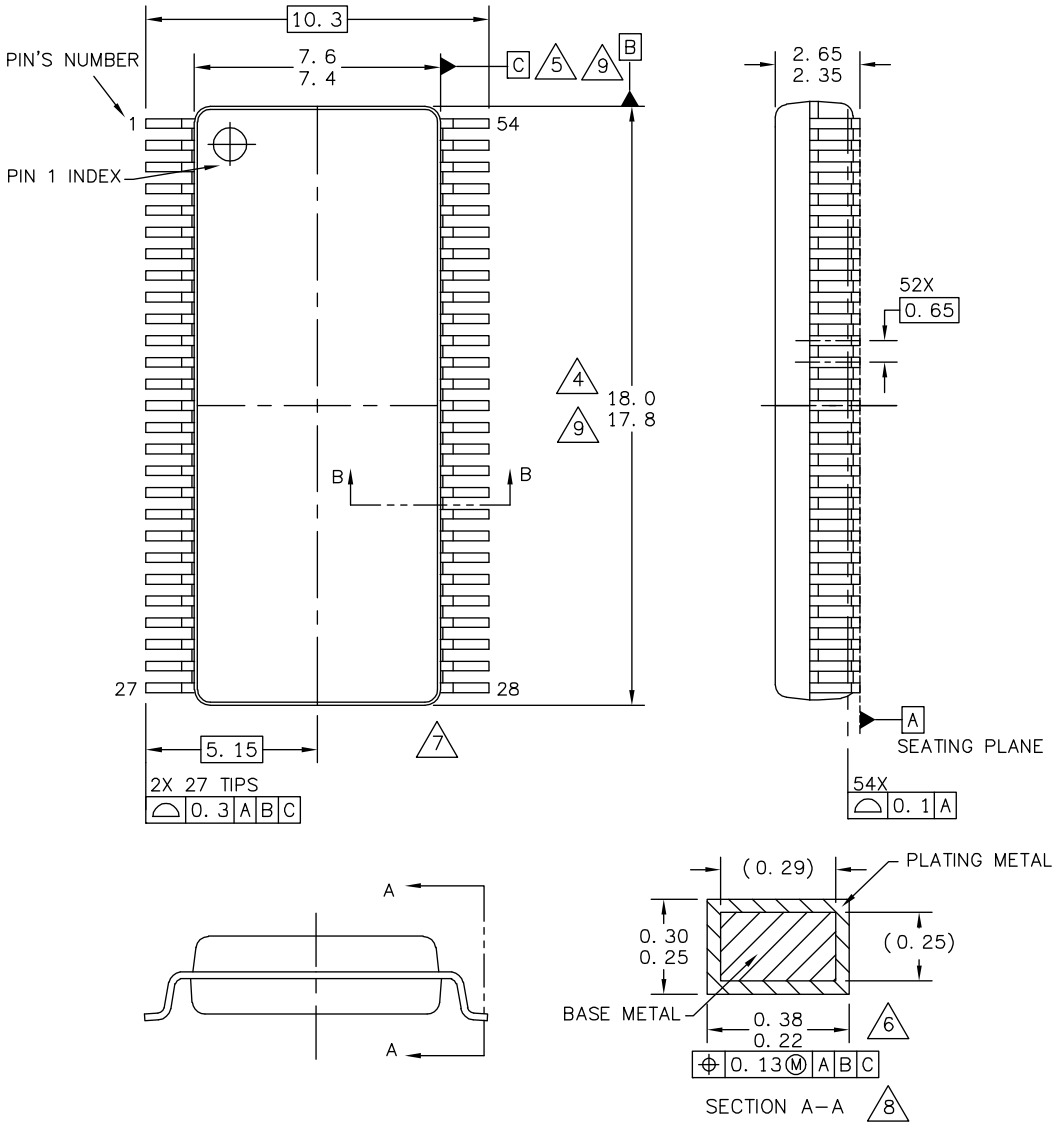
Notes

39. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
40. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ASA99294D drawing number below. Dimensions shown are provided for reference ONLY.



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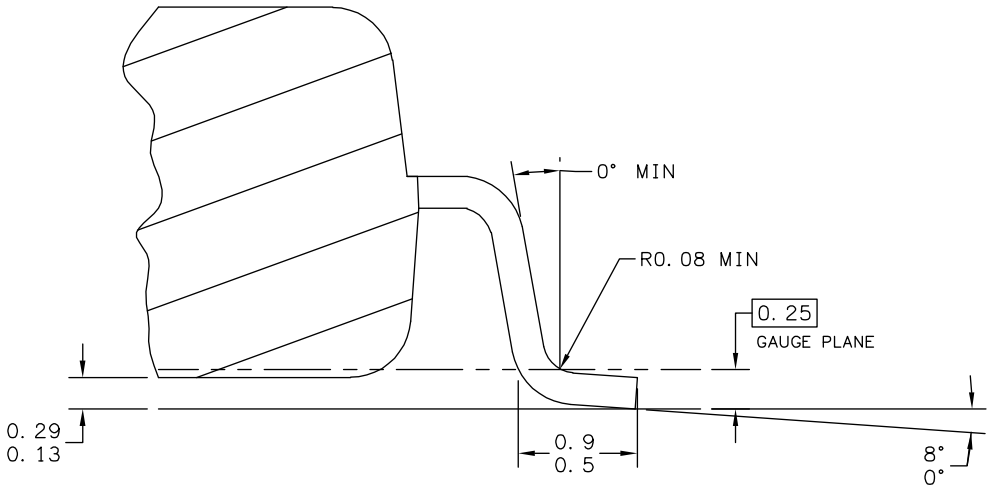
TITLE: 54LD SOIC W/B, 0.65 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365-01	12 APR 2005
	STANDARD: NON-JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

908E624



SECTION B–B

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	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	5/2006	• Implemented Revision History page • Added Pb-Free package option (Suffix EW) and higher Soldering temperature • Added “Y” temperature (T_J -40°C to 125°C) code option (MM908E624AYEW) and updated condition statement for Static and Dynamic Electrical Characteristics • Corrected Figure 11, Operating Modes and Transitions (“STOP command” for transition from Normal to Stop state) • Updated Figure 21, PCB Layout Recommendations, comment NC Pin used for signal routing • Updated Table 15, Component Value Recommendation • Corrected Figure 23, Device on Thermal Test Board • Removed reference to Note 11, Voltage Regulator - Dropout Voltage • Added comment “LIN in recessive state” to Supply Current Range in Stop Mode and Sleep Mode • Updated format to match current data sheet standard. • Added Figure 10, Power On Reset and Normal Request Timeout Timing • Added LIN P/L details • Made clarifications on Max Ratings Table for T_A and T_J Thermal Ratings and the accompanying Note
8.0	3/2007	• Removed “Advance Information” watermark from first page.
9.0	9/2010	• Changed Peak Package Reflow Temperature During Reflow(3)(5) description. • Added note (5)
10.0	8/2011	• Deleted MM908E624ACDWB/R2 • Added MM908E624ACPEW/R2 and MM908E624AYPEW/R2 • Update Freescale form and style. • Updated package drawing
11.0	4/2012	• Removed part number MM908E624ACEW/ R2 and MM908E624AYEW/ R2. • Update Freescale form and style.

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