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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	16
Voltage - Supply	5.5V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	54-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e624acdwbr2

INTERNAL BLOCK DIAGRAM

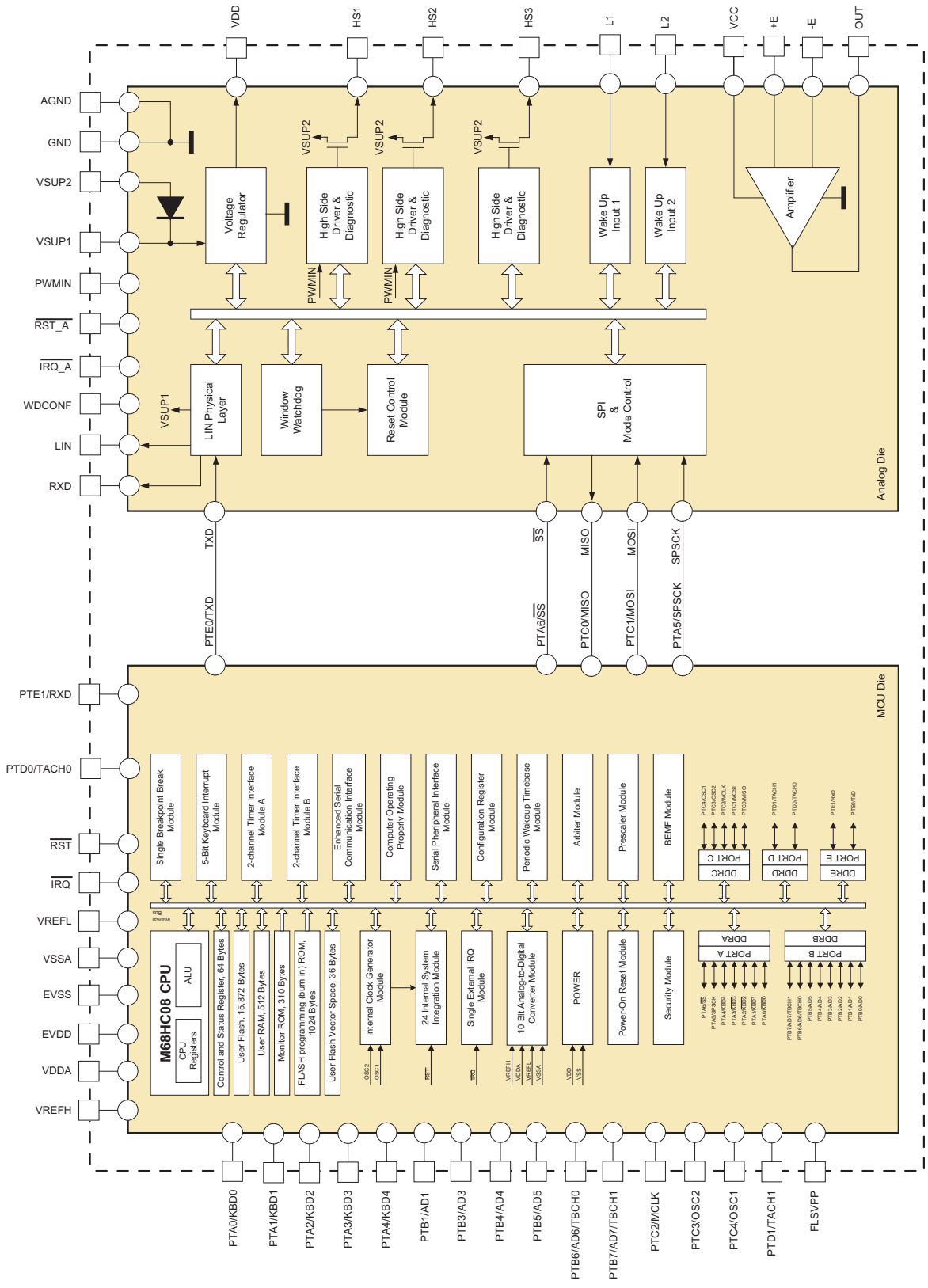


Figure 2. 908E624 Simplified Internal Block Diagram

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Die	Pin	Pin Name	Formal Name	Definition
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	17	PWMIN	Direct High Side Control Input	This pin allows the enabling and PWM control of the high side HS1 and HS2 pins.
Analog	18	RST_A	Internal Reset Output	This pin is the reset output pin of the analog die.
Analog	19	IRQ_A	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	23 24	L1 L2	Wake-Up Inputs	These pins are the wake-up inputs of the analog chip.
Analog	25 26 27	HS3 HS2 HS1	High Side Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	31 28	VSUP1 VSUP2	Power Supply Pins	These pins are device power supply pins.
Analog	29	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	30 34	GND AGND	Power Ground Pins	These pins are device power ground connections.
Analog	33	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	35	VCC	Amplifier Power Supply	This pin is the single +5.0 V power supply for the current sense operational amplifier.
Analog	36	OUT	Amplifier Output	This pin is the output of the current sense operational amplifier.
Analog	37 38	-E +E	Amplifier Inputs	These pins are the current sense operational amplifier inverted and non-inverted inputs.
Analog	39	WDCONF	Window Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
Analog	40	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low-voltage Reset (LVR) Threshold	V_{LVRON}	3.6	4.0	4.4	V
Low-voltage Interrupt (LVI) Threshold Hysteresis	 V_{LVI} V_{LVI_HYS}	 5.7 —	 6.0 1.0	 6.6 —	V
High-voltage Interrupt (HVI) Threshold Hysteresis	 V_{HVI} V_{HVI_HYS}	 18 —	 19.25 220	 20.5 —	 V mV
VOLTAGE REGULATOR (10)					
Normal Mode Output Voltage 2.0 mA < I_{DD} < 50 mA, 5.5 V < V_{SUP} < 27 V	V_{DDRUN}	4.75	5.0	5.25	V
Normal Mode Output Current Limitation (11)	I_{DDRUN}	50	110	200	mA
Dropout Voltage V_{SUP} = 4.9 V, I_{DD} = 50 mA	V_{DDDROP}	—	0.1	0.2	V
Stop Mode Output Voltage (12)	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Regulator Current Limitation	I_{DDSTOP}	4.0	8.0	14	mA
Line Regulation Normal Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA Stop Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	 V_{LRRUN} V_{LRSTOP}	 — —	 20 10	 150 100	mV
Load Regulation Normal Mode, 1.0 mA < I_{DD} < 50 mA, V_{SUP} = 18 V Stop Mode, 1.0 mA < I_{DD} < 5.0 mA, V_{SUP} = 18 V	 V_{LRRUN} V_{LDSTOP}	 — —	 40 40	 150 150	mV
Over-temperature Prewarning (Junction) (13)	T_{PRE}	120	135	160	°C
Thermal Shutdown Temperature (Junction) (13)	T_{SD}	155	170	—	°C
Temperature Threshold Difference T_{SD}-T_{PRE}	ΔT_{SD}-T_{PRE}	20	30	45	°C

Notes

10. Specification with external capacitor 2.0 μF< C < 10 μF and 200 mΩ ≤ ESR ≤ 10 Ω. Capacitor value up to 47 μF can be used.
11. Total V_{DD} regulator current. A 5.0 mA current for current sense operational amplifier is included. Digital output supplied from VDD.
12. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.
13. This parameter is guaranteed by process monitoring but not production tested

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
External Resistor Range	R_{EXT}	10	—	100	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) (14)	WD_{CACC}	-15	—	15	%
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	2.0	—	µA
Output Current Shutdown Threshold	$I_{OV\text{-}CUR}$	50	75	150	mA
Leakage Current to GND	I_{BUS}				µA
VSUP Disconnected, V_{BUS} at 18 V		—	1.0	10	
Recessive State, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}		0.0	3.0	20	
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V		-1.0	—	1.0	
LIN Receiver					V_{SUP}
Receiver Threshold Dominant	V_{BUS_DOM}	—	—	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	—	—	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	—	—	0.175	
HIGH SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	2.0	2.5	
T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	—	4.5	
T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} > 9.0 V		—	3.0	—	
Output Current Limit	I_{LIM}	300	—	600	mA
Over-temperature Shutdown (15), (16)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	µA
Output Clamp Voltage	V_{CL}				V
I_{OUT} = -100 mA		-6.0	—	—	

Notes

14. Watchdog timing period calculation formula: P_{WD} = 0.991 * R_{EXT}+0.648 (R_{EXT} in kΩ and P_{WD} in ms).
15. This parameter is guaranteed by process monitoring but it is not production tested
16. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUT HS3					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25 °C, I_{LOAD} = 50 m A, V_{SUP} > 9.0 V		—	—	7.0	
T_J = 125 °C, I_{LOAD} = 50 mA, V_{SUP} > 9.0 V		—	—	10	
T_J = 125 °C, I_{LOAD} = 30 mA, 5.5 V < V_{SUP} > 9.0 V		—	—	14	
Output Current Limitation	I_{LIM}	60	100	200	mA
Over-temperature Shutdown (17), (18)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	µA
CURRENT SENSE OPERATIONAL AMPLIFIER					
Rail-to-Rail Input Voltage	V_{IMC}	-0.1	—	V_{CC}+0.1	V
Output Voltage Range					V
Output Current ±1.0 mA	V_{OUT1}	0.1	—	V_{CC}-0.1	
Output Current ±5.0 mA	V_{OUT2}	0.3	—	V_{CC}-0.3	
Input Bias Current	I_B	—	—	250	nA
Input Offset Current	I_O	-100	—	100	nA
Input Offset Voltage	V_{IO}	-25	—	25	mV
L1 AND L2 INPUTS					
Low Detection Threshold	V_{THL}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
High Detection Threshold	V_{THH}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.5	—	1.3	
Input Current	I_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	

Notes
17. This parameter is guaranteed by process monitoring but it is not production tested
18. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

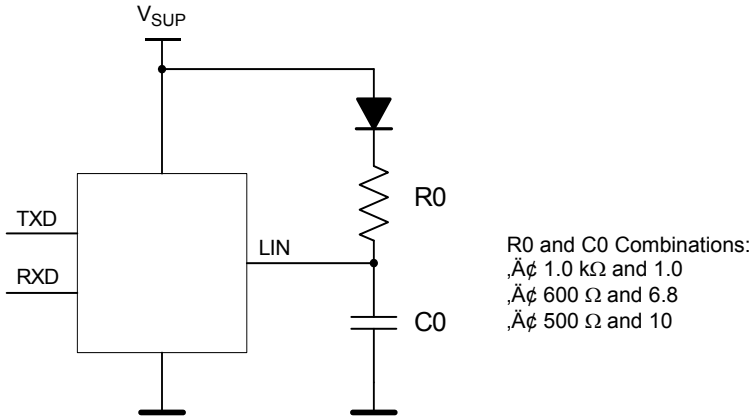


Figure 5. Test Circuit for LIN Timing Measurements

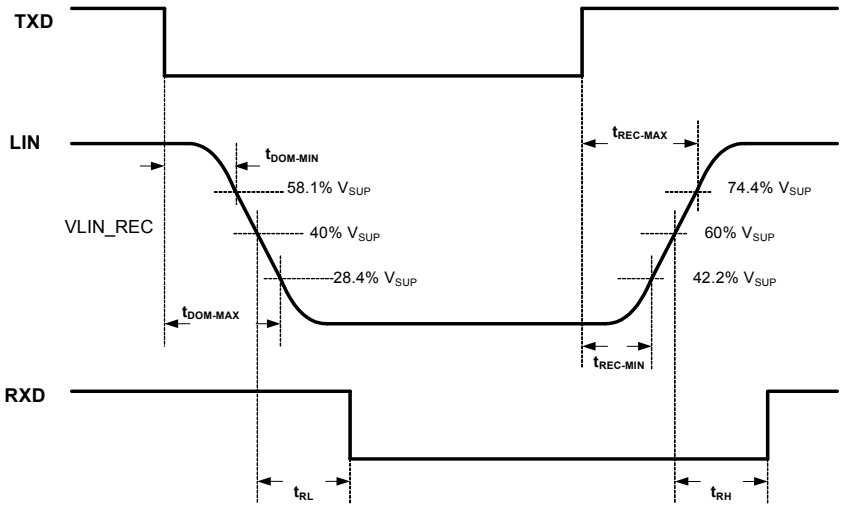


Figure 6. LIN Timing Measurements for Normal Slew Rate

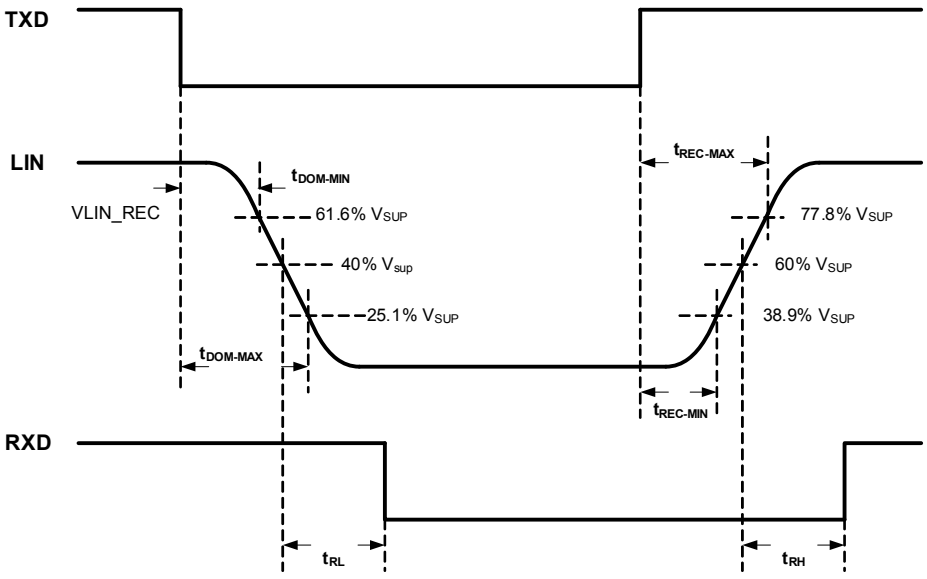


Figure 7. LIN Timing Measurements for Slow Slew Rate

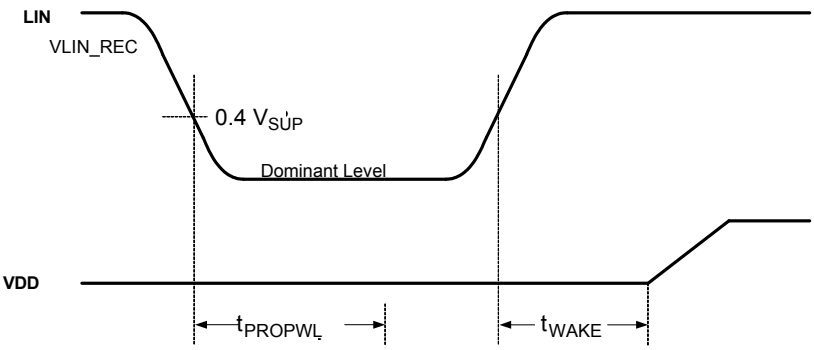


Figure 8. Wake-up Sleep Mode Timing

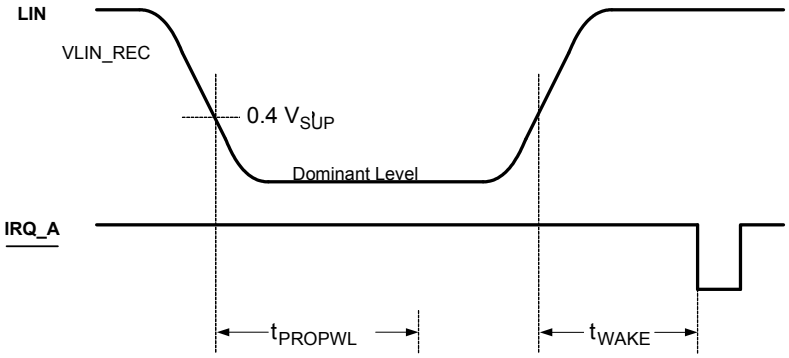


Figure 9. Wake-up Stop Mode Timing

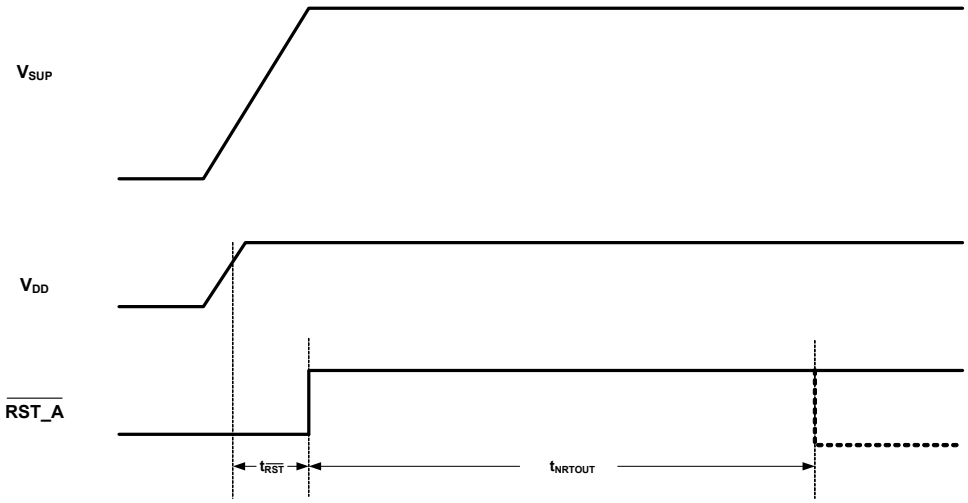


Figure 10. Power On Reset and Normal Request Timeout Timing

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details, refer to the 68HC908EY16 data sheet.

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSSA via separate traces.

For details, refer to the 68HC908EY16 data sheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. Do not connect in the application or connect to GND.

PWMIN PIN (PWMIN)

This pin is the direct PWM input for high side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD to enable the HS1 and HS2 outputs.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the reset output pin of the analog die and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

Important To ensure proper operation, do not add any external pull-up resistor.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. This pin must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

This pin is the configuration pin for the internal watchdog. A resistor is connected to this pin. The resistor value defines the watchdog period. If the pin is open, the watchdog period is fixed to its default value.

The watchdog can be disabled (e.g., for flash programming or software debugging) by connecting this pin to GND.

POWER SUPPLY PINS (VSUP1 AND VSUP2)

This VSUP1 power supply pin supplies the voltage regulator, the internal logic, and LIN transceiver.

This VSUP2 power supply pin is the positive supply for the high side switches.

POWER GROUND PIN (GND)

This pin is the device ground connection.

HIGH SIDE OUTPUT PINS (HS1 AND HS2)

These pins are high side switch outputs to drive loads such as relays or lamps. Each switch is protected with over-temperature and current limit (over-current). The output has an internal clamp circuitry for inductive load. The HS1 and HS2 outputs are controlled by the SPI and have a direct enabled input (PWMIN) for PWM capability.

HIGH SIDE OUTPUT PIN (HS3)

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. The switch is protected with over-temperature and current limit (over-current). The output is controlled only by the SPI.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

WAKE-UP PINS (L1 AND L2)

These pins are high-voltage capable inputs used to sense external switches and to wake-up the device from Sleep or Stop mode. During Normal mode the state of these pins can be read through the SPI.

Important If unused, these pins should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode, this could lead to random wake-up events.

CURRENT SENSE OPERATIONAL AMPLIFIER PINS (E+, E-, OUT, VCC)

These are the pins of the single supply current sense operational amplifier.

- The E+ and E- input pins are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT pin is the output pin of the current sense operational amplifier.
- The VCC pin is the +5.0 V single supply connection.

Note If the operational amplifier is not used, it is possible to connect all pins (E+, E-, OUT and VCC) to GND. In this case, all of the four pins must be grounded.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller. The pin is protected against shorts to GND with an integrated current limit (temperature shutdown could occur).

Important The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR AND CURRENT SENSE AMPLIFIER GROUND PIN (AGND)

The AGND pin is the ground pin of the voltage regulator and the current sense operational amplifier.

Important GND, AGND, VSS, EVSS, VSSA, and VREFL pins must be connected together.

NO CONNECT PINS (NC)

The NC pins are not connected internally.

Note Each of the NC pins can be left open or connected to ground (recommended).

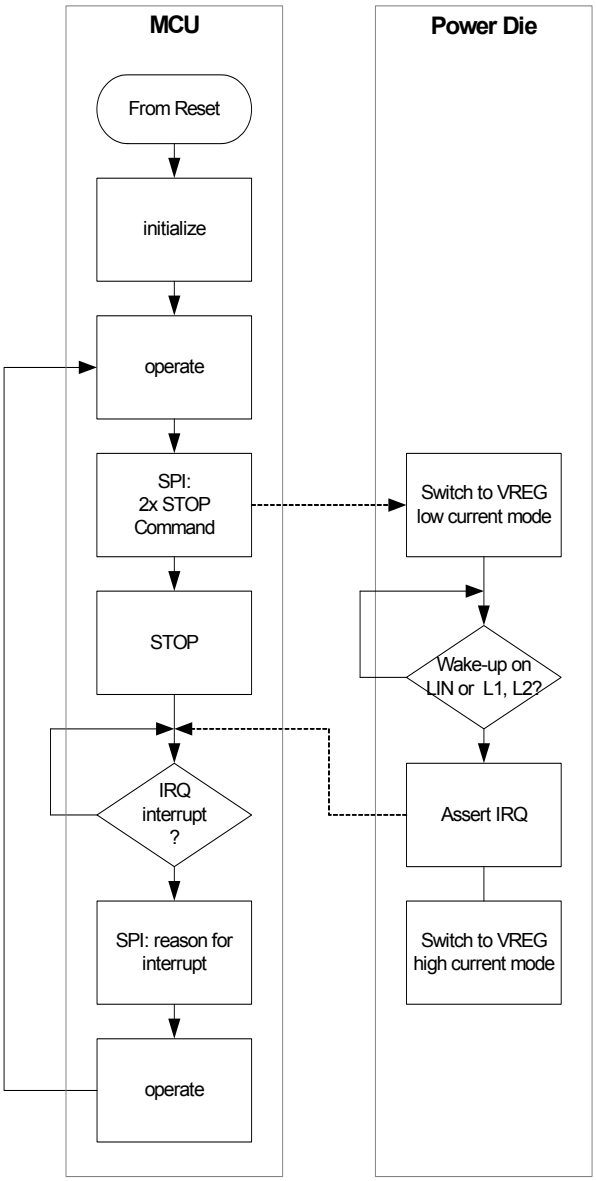


Figure 12. Stop Mode/Wake-up Procedure

ANALOG DIE INPUTS/OUTPUTS

High Side Output Pins HS1 and HS2

These are two high side switches used to drive loads such as relays or lamps. They are protected with over-temperature and current limit (over-current) and include an active internal clamp circuitry for inductive load drive. Control is done using the SPI Control register. PWM capability is offered through the PWMIN input pin.

The high side switch is turned on if both the HSxON bit in the SPI Control register is set and the PWMIN input is HIGH (refer to Figure 13, page 22). In order to have HS1 on, the PWMIN must be HIGH and bit HS1ON must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD pin.

Current Limit (Over-current) Protection

These high side switches feature current limit to protect them against over-current and short circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop modes the high sides are disabled.

High Side Output HS3

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done using the SPI Control register. No direct PWM control is possible on this pin (refer to Figure 14, page 22).

Current Limit (Over-current) Protection

This high side feature switch feature current limit to protect it against over-current and short-circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop mode the high side is disabled.

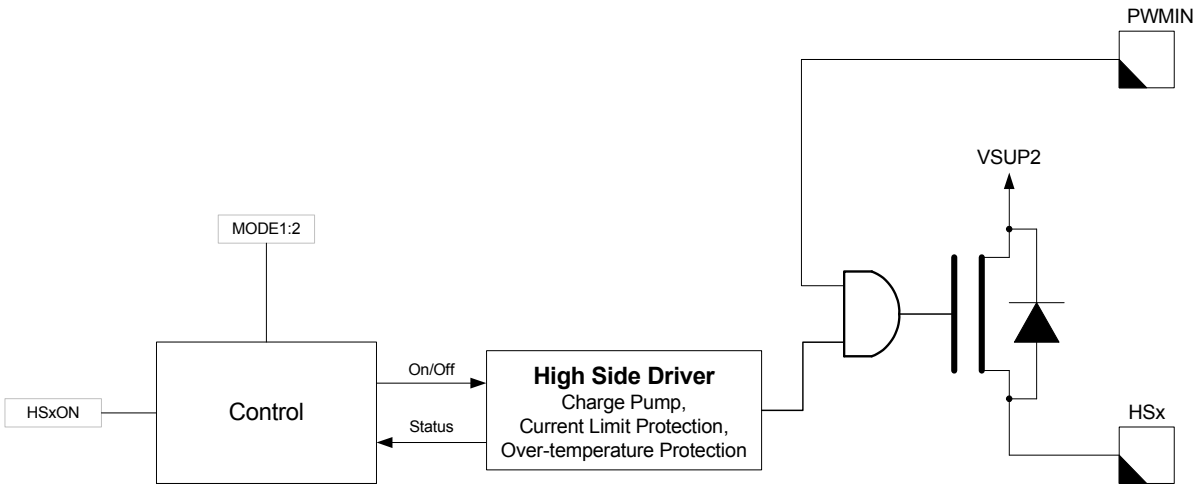


Figure 13. High Side HS1 and HS2 Circuitry

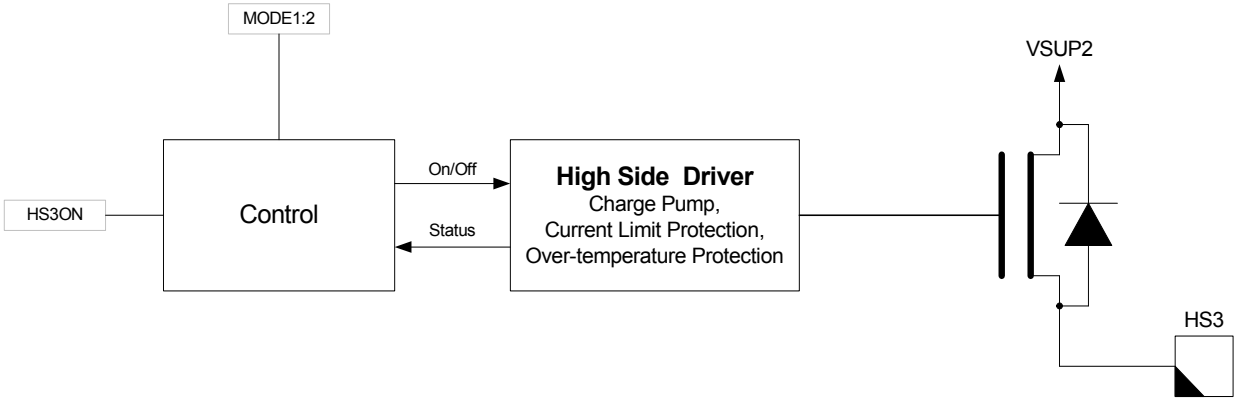


Figure 14. High Side HS3 Circuitry

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with over-current protection and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LINSL2:1 in the SPI Control Register. The initial slew rate is optimized for 20 kBit/s.

Table 7. SPI Register Overview

Read/Write Information	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
Write	LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
Read	INTSRC (30)	LINWU or LINFAIL	HVF	LVF or BATFAIL (31)	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes
30. D7 signals interrupts and wake-up interrupts, D6:D0 indicated the source.
31. The first SPI read after reset returns the BATFAIL flag state on bit D4.

SPI Control Register (Write)

Table 8 shows the SPI Control register bits by name.

Table 8. Control Bits Function (Write Operation)

D7	D6	D5	D4	D3	D2	D1	D0
LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1

LINSL2:1—LIN Baud Rate and Low-power Mode Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 9. Reset clears the LINSL2:1 bits.

Table 9. LIN Baud Rate and Low-power Mode Selection Bits

LINSL2	LINSL1	Description
0	0	Baud Rate up to 20 kbps (normal)
0	1	Baud Rate up to 10 kbps (slow)
1	0	Fast Program Download Baud Rate up to 100 kbps
1	1	Low-power Mode (Sleep or Stop) Request

LIN-PU—LIN Pull-up Enable Bit

This bit controls the LIN pull-up resistor during Sleep and Stop modes.

- 1 = Pull-up disconnected in Sleep and Stop modes.
- 0 = Pull-up connected in Sleep and Stop modes.

If the Pull-up is disconnected, a small current source is used to pull the LIN pin in recessive state. In case of an erroneous short of the LIN bus to ground, this will significantly reduce the power consumption, e.g. in combination with STOP/SLEEP mode.

HS3ON:HS1ON—High Side H3:HS1 Enable Bits

These bits enable the HSx. Reset clears the HSxON bit.

- 1 = HSx switched on (refer to Note below).
- 0 = HSx switched off.

Note If no PWM on HS1 and HS2 is required, the PWMIN pin must be connected to the VDD pin.

MODE2:1—Mode Section Bits

The MODE2:1 bits control the operating modes and the watchdog in accordance with Table 10.

Table 10. Mode Selection Bits

MODE2	MODE1	Description
0	0	Sleep Mode (32)
0	1	Stop Mode (32)
1	0	Watchdog Clear (33)
1	1	Run (Normal) Mode

Notes
32. To enter Sleep and Stop mode, a special sequence of SPI commands is implemented.
33. The device stays in Run (Normal) mode.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence

The Sleep command, as shown in Table 11, must be sent twice.

Table 11. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	0

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E624 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12 V supply voltage some additional items have to be considered:

- nominal 12 V rather than 5.0 or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin
- MCU monitoring (Normal request timeout) has to be disabled

For a detailed information on the MCU related development support see the MC68HC908EY16 data sheet - section development support.

The programming is principally possible at two stages in the manufacturing process — first on chip level, before the IC is soldered onto a PCB board and second after the IC is soldered onto the PCB board.

Chip Level Programming

On Chip level the easiest way is to only power the MCU with +5.0 V (see Figure 18) and not to provide the analog chip with VSUP, in this setup all the analog pin should be left open (e.g. VSUP[1:2]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 data sheet - section development support.

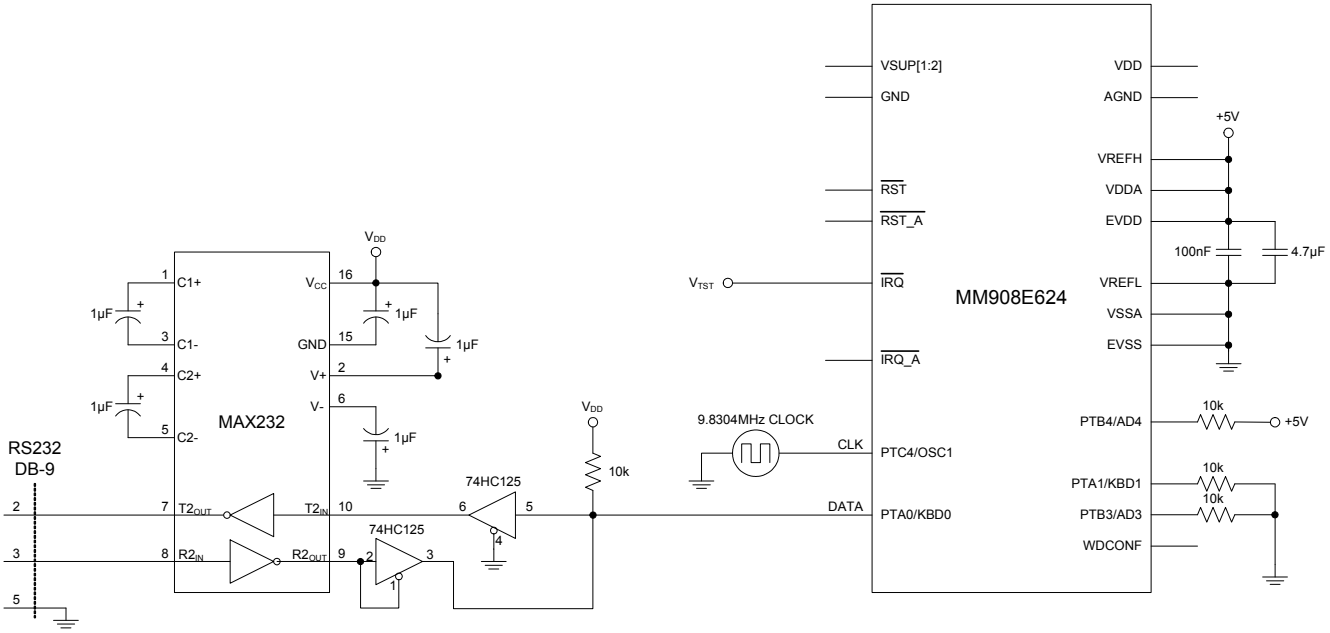


Figure 18. Normal Monitor Mode Circuit (MCU only)

Of course it is also possible to supply the whole system with VSUP (12 V) instead as described in Figure 19, page 29.

PCB Level Programming

If the IC is soldered onto the PCB board, it is typically not possible to separately power the MCU with +5.0 V, the whole system has to be powered up providing V_{SUP} (see Figure 19).

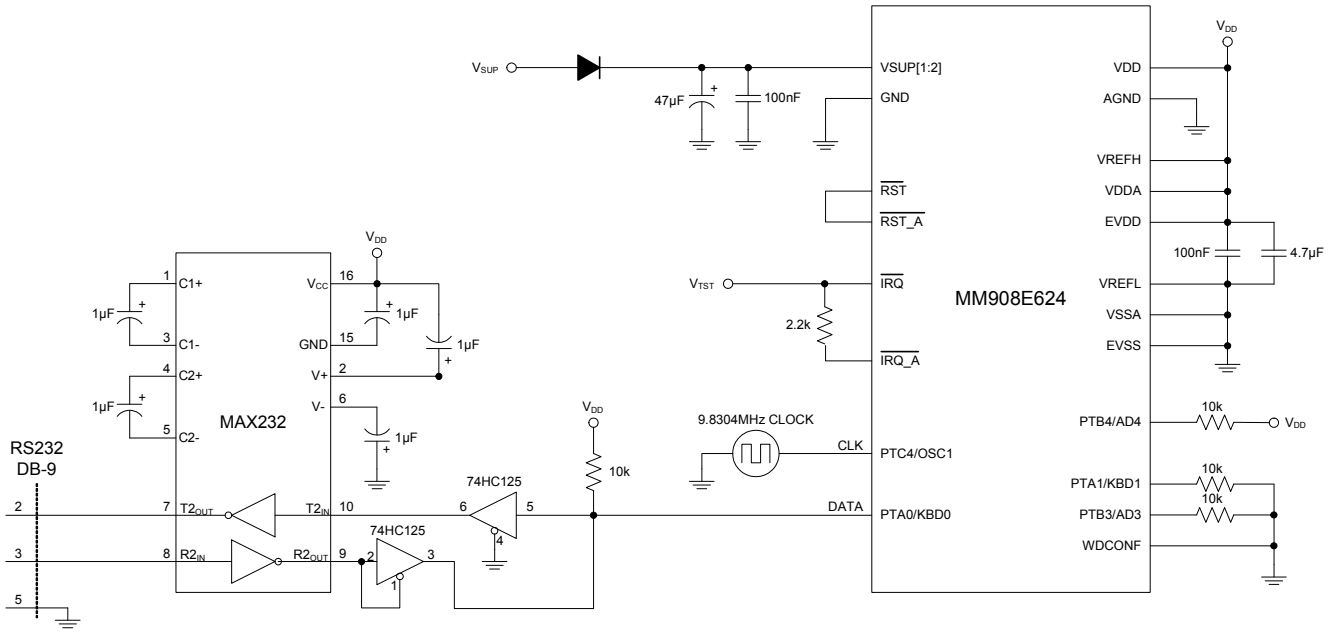


Figure 19. Normal Monitor Mode Circuit

Table 14 summarizes the possible configurations and the necessary setups.

Table 14. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	WDCONF	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
					PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	GND	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	GND	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND								ON	disabled	disabled	—	Nominal 1.6 MHz	Nominal 6300
User	V_{DD}	V_{DD}	R_{EXT}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6 MHz	Nominal 6300

Notes

34. PTA0 must have a pull-up resistor to V_{DD} in monitor mode.
35. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1.
36. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256.
37. X = don't care.
38. V_{TST} is a high voltage V_{DD} + 3.5 V ≤ V_{TST} ≤ V_{DD} + 4.5 V.

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale website: www.freescale.com.

VSUP Pins (VSUP1 and VSUP2)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN Pin

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) it is recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU Digital Supply Pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU Analog Supply Pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins it is important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 20 and Figure 21 show the recommendations on schematics and layout level and Table 15 indicates recommended external components and layout considerations.

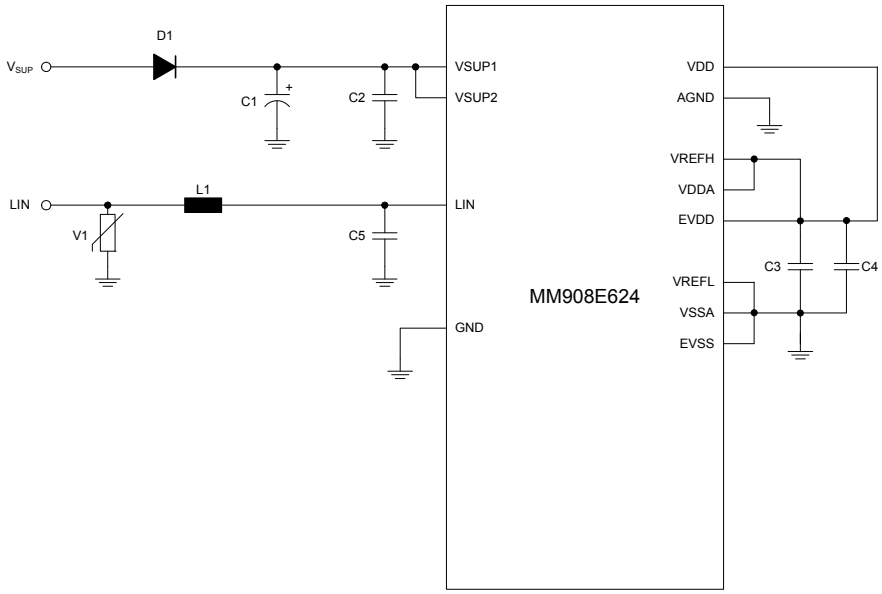
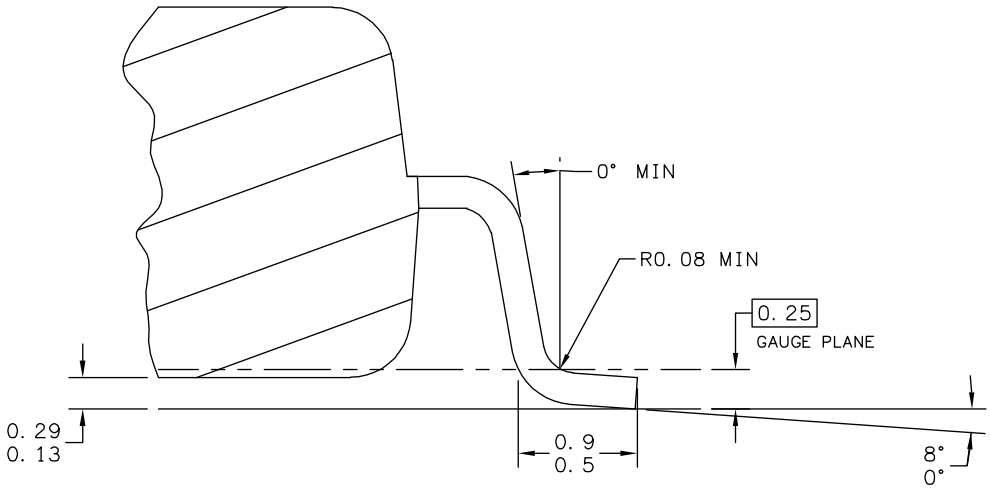


Figure 20. EMC/EMI Recommendations



SECTION B–B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH CASE–OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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TITLE: 54LD SOIC W/B, 0.65 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

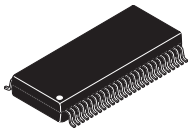
908E624

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 3.0)

908E624

54-Pin SOICW



EW (Pb-FREE) SUFFIX
98ASA99294D
54-Pin SOICW

Note For package dimensions, refer to 98ASA99294D.

INTRODUCTION

This thermal addendum is provided as a supplement to the MM908E624 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MM908E624 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

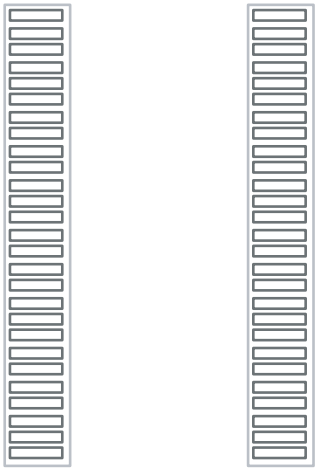
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below

Standards

Table 16. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	40	31	36
$R_{\theta JBmn}$ (2)(3)	25	16	21
$R_{\theta JAmn}$ (1)(4)	57	47	52
$R_{\theta JCmn}$ (5)	21	12	16

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC
0.65 mm Pitch
17.9 mm x 7.5 mm Body

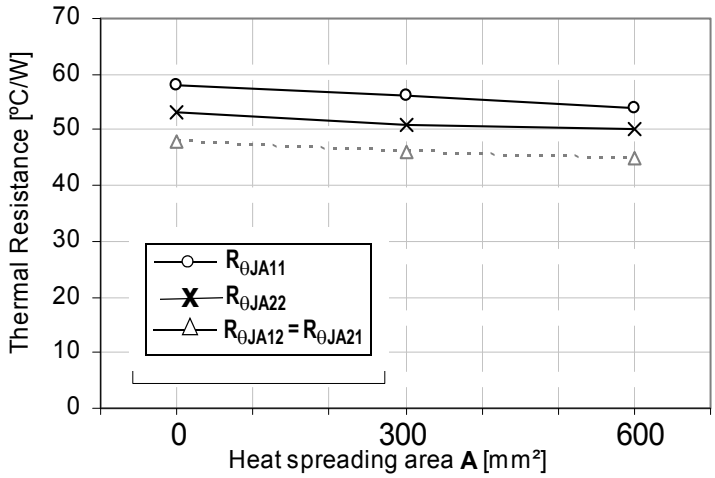


Figure 23. Device on Thermal Test Board

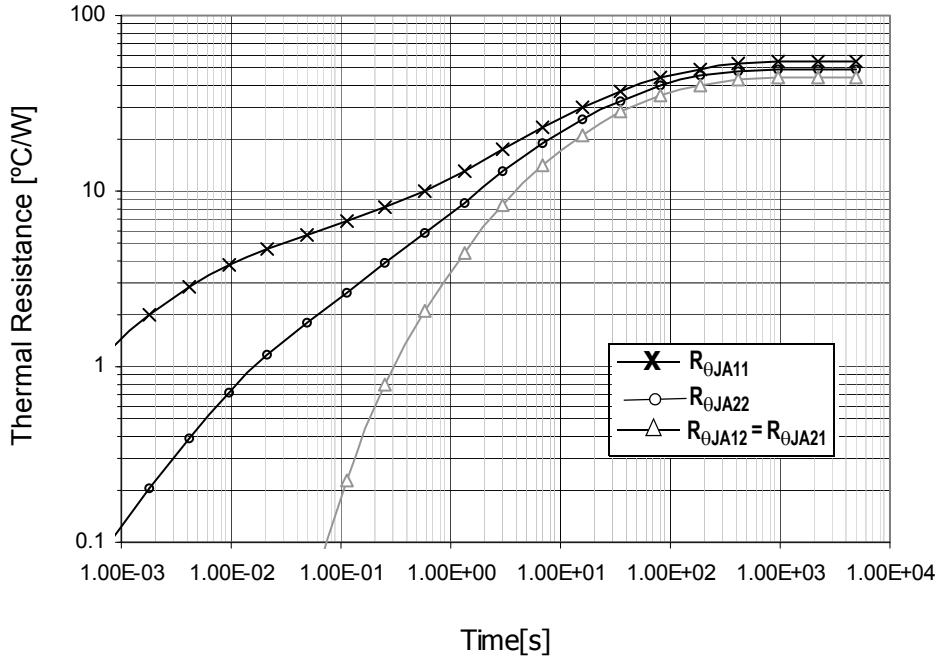


Figure 24. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

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