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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	16
Voltage - Supply	5.5V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	54-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e624acew

PIN CONNECTIONS

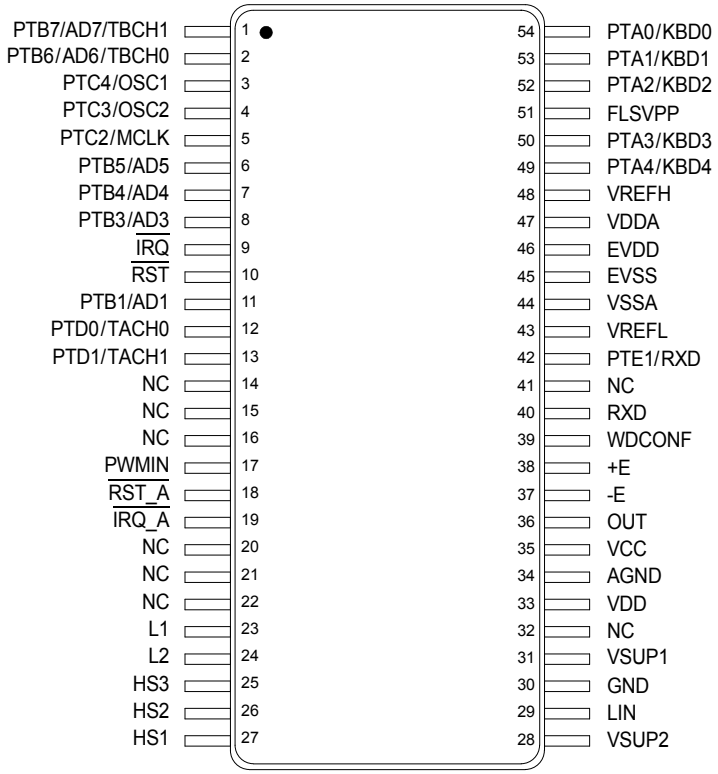


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0 PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
—	14, 15, 16, 20, 21, 22, 32, 41	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin, that can is shared with other functional modules in the MCU.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP}	5.5	—	18	V
Functional Operating Voltage (6)	V_{SUPOP}	—	—	27	V
SUPPLY CURRENT RANGE					
Normal Mode (7) V_{SUP} = 13.5 V, Analog Chip in Normal Mode, MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	20	—	mA
Stop Mode (7), (8) V_{SUP} = 13.5 V, LIN in recessive state	I_{STOP}	—	60	75	µA
Sleep Mode (7), (8) V_{SUP} = 13.5 V, LIN in recessive state	I_{SLEEP}	—	35	45	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pin $\overline{RST\_A}$					
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	V
High-state Output Current (V_{OUT} > 3.5 V)	I_{OH}	—	250	—	µA
Pull-down Current Limitation	I_{OL_MAX}	-1.5	—	-8.0	mA
Output Pin $\overline{IRQ\_A}$					V
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	
High-state Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	—	—	
Output Pin RXD					
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	V
High-state Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	—	—	V
Capacitance (9)	C_{IN}	—	4.0	—	pF
Input Pin PWMIN					
Input Logic Low Voltage	V_{IL}	—	—	1.5	V
Input Logic High Voltage	V_{IH}	3.5	—	—	V
Input Current	I_{IN}	-10	—	10	µA
Capacitance (9)	C_{IN}	—	4.0	—	pF
Pin TXD, $\overline{SS}$–Pull-up Current	I_{PU}	—	40	—	µA

Notes

6. Device is fully functional. All functions are operating. Over-temperature may occur.
7. Total current (I_{VSUP1} + I_{VSUP2}) measured at GND pin.
8. Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
9. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
External Resistor Range	R_{EXT}	10	—	100	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) (14)	WD_{CACC}	-15	—	15	%
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	2.0	—	µA
Output Current Shutdown Threshold	$I_{OV\text{-}CUR}$	50	75	150	mA
Leakage Current to GND	I_{BUS}				µA
VSUP Disconnected, V_{BUS} at 18 V		—	1.0	10	
Recessive State, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}		0.0	3.0	20	
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V		-1.0	—	1.0	
LIN Receiver					V_{SUP}
Receiver Threshold Dominant	V_{BUS_DOM}	—	—	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	—	—	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	—	—	0.175	
HIGH SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	2.0	2.5	
T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	—	4.5	
T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} > 9.0 V		—	3.0	—	
Output Current Limit	I_{LIM}	300	—	600	mA
Over-temperature Shutdown (15), (16)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	µA
Output Clamp Voltage	V_{CL}				V
I_{OUT} = -100 mA		-6.0	—	—	

Notes

14. Watchdog timing period calculation formula: P_{WD} = 0.991 * R_{EXT}+0.648 (R_{EXT} in kΩ and P_{WD} in ms).
15. This parameter is guaranteed by process monitoring but it is not production tested
16. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate (19), (20)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1	-10.44	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2	—	—	11	µs
Driver Characteristics for Slow Slew Rate (19), (21)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1S	-22	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2S	—	—	23	µs
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	15	—	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay (22)	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay (22)	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	$t_{PROP}WL$	35	—	150	µs
Bus Wake-up Event Reported (23)	t_{WAKE}	—	20	—	µs

Notes

19. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
20. See Figure 6, page 14.
21. See Figure 7, page 14.
22. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
23. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 8 and Figure 9, page 15. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD pin.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER (CONTINUED)					
Output Current Shutdown Delay	$t_{OV-DELAY}$	—	10	—	µs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	f_{SPIOP}	0.25	—	4.0	MHz
L1 AND L2 INPUTS					
Wake-up Filter Time (24)	t_{WUF}	8.0	20	38	µs
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
Watchdog Period	t_{PWD}				ms
External Resistor R_{EXT} = 10 kΩ (1%)		—	10.558	—	
External Resistor R_{EXT} = 100 kΩ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Pin Open)		97	150	205	
STATE MACHINE TIMING					
Reset Low Level Duration after V_{DD} High (28)	$t_{\overline{RST}}$	0.65	1.0	1.35	ms
Interrupt Low Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Normal Request Mode Timeout (28)	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On (25), (26)	t_{S-HSON}	—	3.0	10	µs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off (25), (26)	$t_{S-HSOFF}$	—	3.0	10	µs
Delay Between Normal Request and Normal Mode After W/D Trigger Command (27)	t_{S-NR2N}	6.0	35	70	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and Normal Request Mode (VDD On and Reset High)	$t_{W-\overline{SS}}$	15	40	80	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and First Accepted SPI Command	t_{W-SPI}	90	—	N/A	µs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{S-1STSPI}$	30	—	N/A	µs
Minimum Time Between Two Rising Edges on $\overline{SS}$	$t_{2\overline{SS}}$	15	—	—	µs

Notes
24. This parameter is guaranteed by process monitoring but is not production tested.
25. Delay between turn-on or turn-off command and high side on or high side off, excluding rise or fall time due to external load.
26. Delay between the end of the SPI command (rising edge of the $\overline{SS}$) and start of device activation/deactivation.
27. This parameter is guaranteed by process monitoring but it is not production tested.
28. Also see Figure 10 on page 15

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Supply Voltage Rejection Ratio (29)	SVR	60	—	—	dB
Common Mode Rejection Ratio (29)	CMR	70	—	—	dB
Gain Bandwidth (29)	GBP	1.0	—	—	MHz
Slew Rate	SR	0.5	—	—	V/μs
Phase Margin (for Gain = 1, Load 100 pF/ 5.0 kΩ (29)	PHMO	40	—	—	°
Open Loop Gain	OLG	—	85	—	dB

Notes

29. This parameter is guaranteed by process monitoring but it is not production tested.

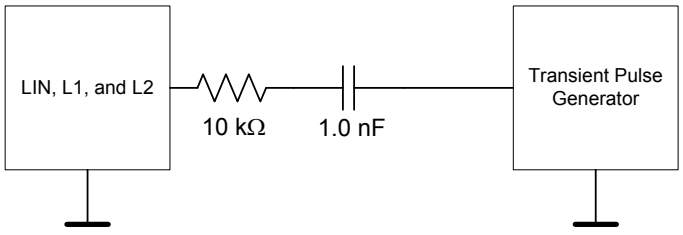
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 data sheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note Waveform in accordance with ISO7637 Part 1, Test Pulses 1, 2, 3a, and 3b.

Figure 4. Test Circuit for Transient Test Pulses

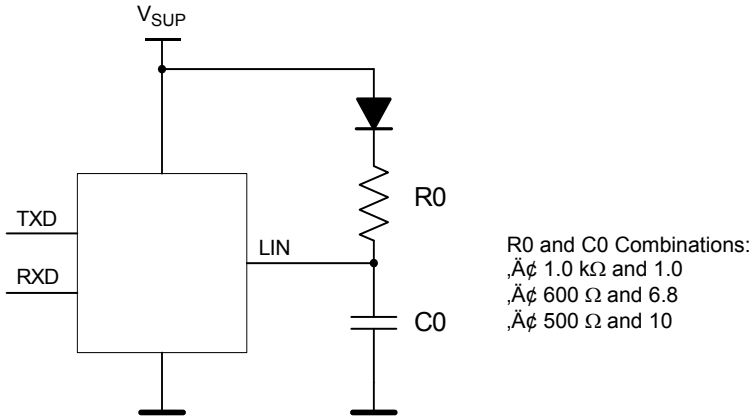


Figure 5. Test Circuit for LIN Timing Measurements

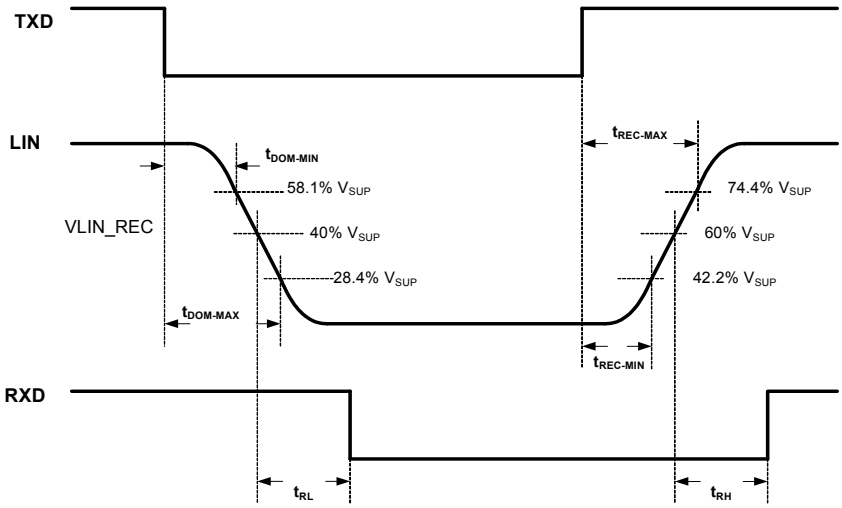


Figure 6. LIN Timing Measurements for Normal Slew Rate

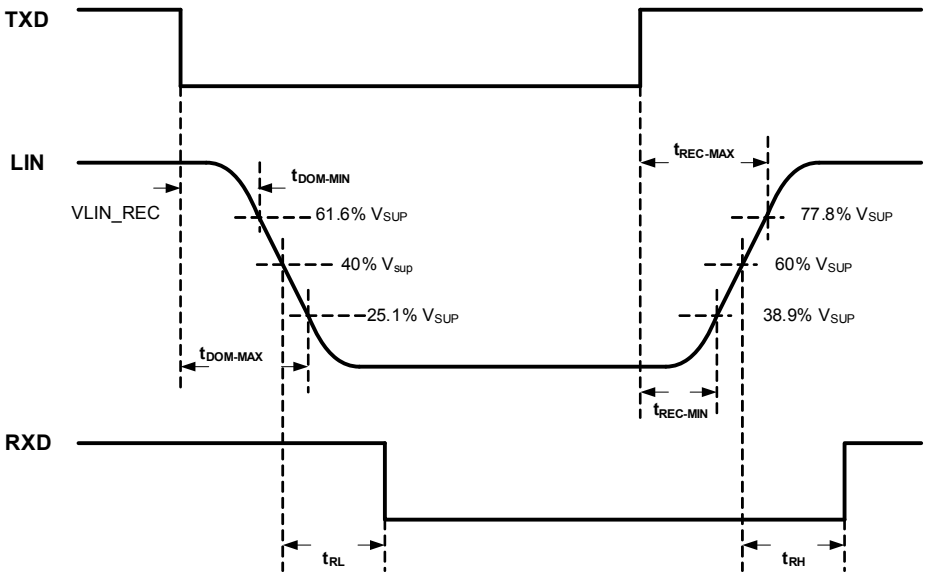


Figure 7. LIN Timing Measurements for Slow Slew Rate

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E624 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E624 is well suited to perform relay control in applications like window lift, sunroof, etc., via a three-wire LIN bus.

The device combines an HC908EY16 MCU core with flash memory together with a *SmartMOS* IC chip. The *SmartMOS* IC chip combines power and control in one chip. Power switches are provided on the *SmartMOS* IC configured as high side outputs. Other ports are also provided, which include a current sense operational amplifier port and two wake-up pins. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Figure 1, 908E624 Simplified Application Diagram, page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details, refer to the 68HC908EY16 data sheet.

PORT B I/O PINS (PTB1:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

The PTB0/AD0 and PTB2/AD2 pins are not accessible in this device.

For details, refer to the 68HC908EY16 data sheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details, refer to the 68HC908EY16 data sheet.

PORT D I/O PINS (PTD:0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

For details, refer to the 68HC908EY16 data sheet.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

Important To ensure proper operation, do not add any external pull-up resistor.

For details, refer to the 68HC908EY16 data sheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins, respectively. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 data sheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details, refer to the 68HC908EY16 data sheet.

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSSA via separate traces.

For details, refer to the 68HC908EY16 data sheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. Do not connect in the application or connect to GND.

PWMIN PIN (PWMIN)

This pin is the direct PWM input for high side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD to enable the HS1 and HS2 outputs.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the reset output pin of the analog die and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

Important To ensure proper operation, do not add any external pull-up resistor.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. This pin must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

This pin is the configuration pin for the internal watchdog. A resistor is connected to this pin. The resistor value defines the watchdog period. If the pin is open, the watchdog period is fixed to its default value.

The watchdog can be disabled (e.g., for flash programming or software debugging) by connecting this pin to GND.

POWER SUPPLY PINS (VSUP1 AND VSUP2)

This VSUP1 power supply pin supplies the voltage regulator, the internal logic, and LIN transceiver.

This VSUP2 power supply pin is the positive supply for the high side switches.

POWER GROUND PIN (GND)

This pin is the device ground connection.

HIGH SIDE OUTPUT PINS (HS1 AND HS2)

These pins are high side switch outputs to drive loads such as relays or lamps. Each switch is protected with over-temperature and current limit (over-current). The output has an internal clamp circuitry for inductive load. The HS1 and HS2 outputs are controlled by the SPI and have a direct enabled input (PWMIN) for PWM capability.

HIGH SIDE OUTPUT PIN (HS3)

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. The switch is protected with over-temperature and current limit (over-current). The output is controlled only by the SPI.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

WAKE-UP PINS (L1 AND L2)

These pins are high-voltage capable inputs used to sense external switches and to wake-up the device from Sleep or Stop mode. During Normal mode the state of these pins can be read through the SPI.

Important If unused, these pins should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode, this could lead to random wake-up events.

CURRENT SENSE OPERATIONAL AMPLIFIER PINS (E+, E-, OUT, VCC)

These are the pins of the single supply current sense operational amplifier.

- The E+ and E- input pins are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT pin is the output pin of the current sense operational amplifier.
- The VCC pin is the +5.0 V single supply connection.

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	$\overline{\text{RST\_A}}$ Output	Watchdog Function	HS1, HS2, and HS3	LIN Interface	Sense Amplifier
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Recessive only	Not active
Normal Request	V_{DD} ON	N/A	HIGH	150 ms time out if WD enabled	Enabled	Transmit and receive	Not active
Normal (Run)	V_{DD} ON	N/A	HIGH	Window WD if enabled	Enabled	Transmit and receive	Active
Stop	V_{DD} ON with limited current capability	LIN wake-up, L1, L2 state change, $\overline{\text{SS}}$ rising edge	HIGH	Disabled	Disabled	Recessive state with wake-up capability	Not active
Sleep	V_{DD} OFF	LIN wake-up L1, L2 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability	Not active

INTERRUPTS

In Normal (Run) mode the 908E624 has four different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ pin is generated to report a fault to the MCU. All interrupts are not maskable and cannot be disabled.

After an Interrupt the INTSRC bit in the SPI Status register is set, indicating the source of the event. This interrupt source information is only transferred once, and the INTSRC bit is cleared automatically.

Low-Voltage Interrupt

Low-voltage interrupt (LVI) is related to external supply voltage VSUP1. If this voltage falls below the LVI threshold, it will set the LVF bit in the SPI Status register and an interrupt will be initiated. The LVF bit remains set as long as the Low-voltage condition is present.

During Sleep and Stop mode the low-voltage interrupt circuitry is disabled.

High-voltage Interrupt

High-voltage interrupt (HVI) is related to external supply voltage VSUP1. If this voltage rises above the HVI threshold, it will set the HVF bit in the SPI Status register and an interrupt will be initiated. The HVF bit remains set as long as the high-voltage condition is present.

During Sleep and Stop mode the high-voltage interrupt circuitry is disabled.

Wake-up Interrupts

In Stop mode the $\overline{\text{IRQ\_A}}$ pin reports wake-up events on the L1, L2, or the LIN bus to the MCU. All wake-up interrupts are not maskable and cannot be disabled.

After a wake-up interrupt, the INTSRC bit in the Serial Peripheral Interface (SPI) Status register is set, indicating the source of the event. This wake-up source information is only transferred once, and the INTSRC bit is cleared automatically.

Figure 12, page 21, describes the Stop/Wake-up procedure.

Voltage Regulator Temperature Prewarning (VDDT)

Voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Status register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop mode the voltage regulator temperature prewarning circuitry is disabled.

High Side Switch Thermal Shutdown (HSST)

The high side switch thermal shutdown HSST is generated if one of the high side switches HS1:HS3 is above the HSST threshold, it will shutdown all high side switches, set the HSST flag in the SPI Status register and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present.

During Sleep and Stop mode the high side switch thermal shutdown circuitry is disabled.

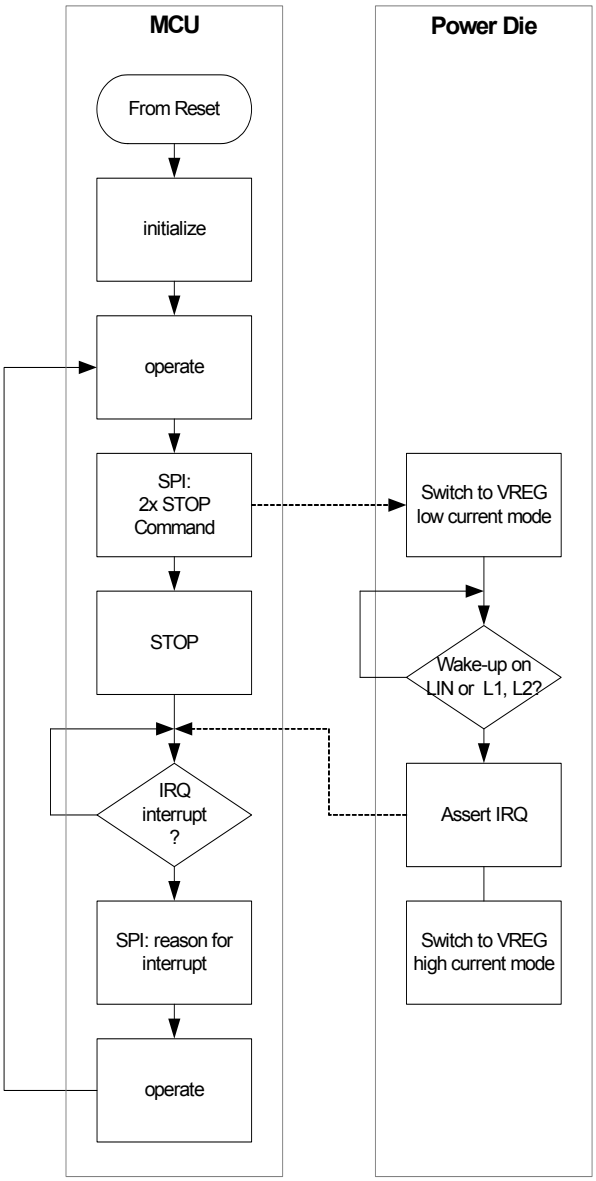


Figure 12. Stop Mode/Wake-up Procedure

ANALOG DIE INPUTS/OUTPUTS

High Side Output Pins HS1 and HS2

These are two high side switches used to drive loads such as relays or lamps. They are protected with over-temperature and current limit (over-current) and include an active internal clamp circuitry for inductive load drive. Control is done using the SPI Control register. PWM capability is offered through the PWMIN input pin.

The high side switch is turned on if both the HSxON bit in the SPI Control register is set and the PWMIN input is HIGH (refer to Figure 13, page 22). In order to have HS1 on, the PWMIN must be HIGH and bit HS1ON must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD pin.

Current Limit (Over-current) Protection

These high side switches feature current limit to protect them against over-current and short circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled in Normal and Normal Request mode.

An over-current condition (e.g. LIN bus short to V_{BAT}) or a over-temperature in the output low side FET will shutdown the transmitter and set the LINFAIL flag in the SPI Status Register.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN pin can be disconnected, with the LIN-PU bit in the SPI Control Register, and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

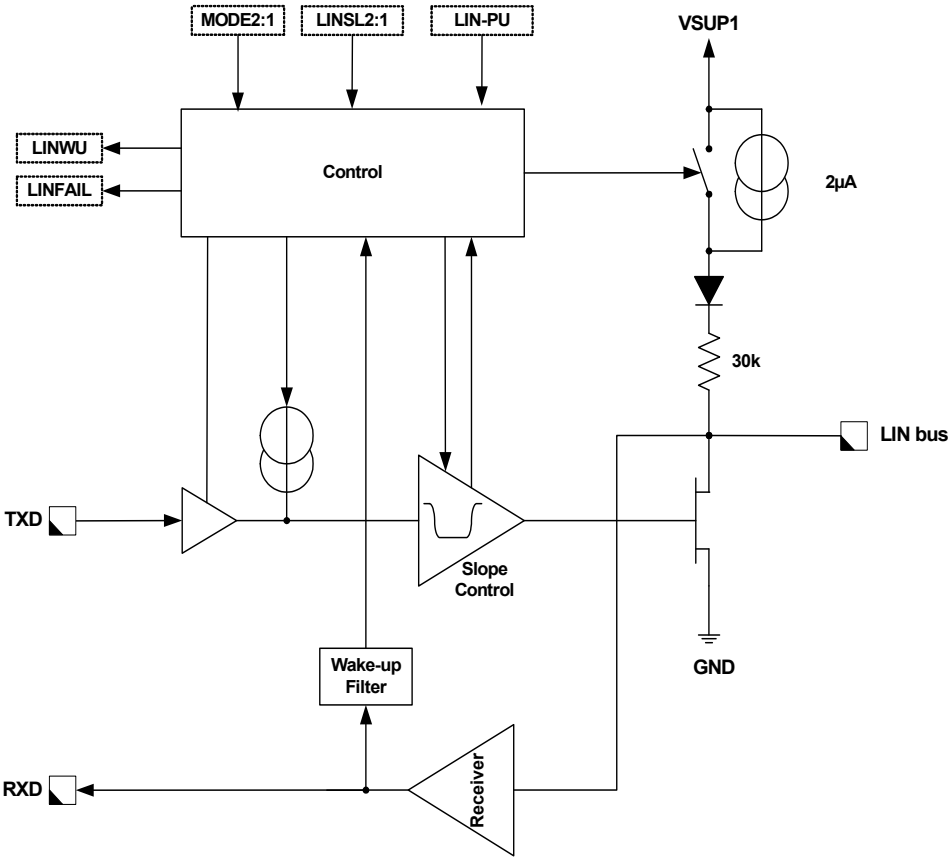


Figure 15. LIN Interface

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see Figure 2, page 2). When TXD is LOW, the LIN pin is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD pin has an internal pull-up current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a wake-up interrupt and set the LINWF flag in the SPI Status Register. Also see Figure 9, page 15.

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is

disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register. Also see Figure 8, page 15).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF pin. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to Table 8, page 26).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST\_A}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

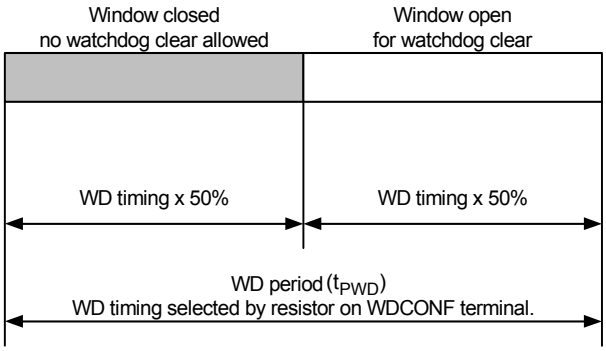


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF pin must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD}\ [ms] = 0.991 * R_{EXT}\ [k\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Over-current) Protection

The voltage regulator has current limit to protect the device against over-current and short-circuit conditions.

Over-temperature Protection

The voltage regulator also features an over-temperature protection having an over-temperature warning (Interrupt - VDDT) and an over-temperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease of use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25%, due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at the address $FDC2. After trimming the ICG, a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 µF) V_{DD} = 5.0 V, $T_{Ambient}$~23 °C) and will vary over-temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values must be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

Stop Mode Sequence

The Stop command, as shown in Table 12, must be sent twice.

Table 12. Stop Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	1

SPI Status Register (Read)

Table 13 shows the SPI Status register bits by name.

Table 13. Control Bits Function (Read Operation)

D7	D6	D5	D4	D3	D2	D1	D0
INTSRC	LINWU or LINFAIL	HVF	LVF or BATFAIL	VDDT	HSST	L2	L1

INTSCR—Register Content Flags or Interrupt Source

This bit indicates if the register contents reflect the flags or an interrupt/wake-up interrupt source.

- 1 = D6:D0 reflects the interrupt or wake-up source.
- 0 = No interrupt occurred. Other SPI bits report real time status.

LINWU/LINFAIL—LIN Status Flag Bit

This bit indicates a LIN wake-up condition.

- 1 = LIN bus wake-up occurred or LIN over-current/over-temperature occurred.
- 0 = No LIN bus wake-up occurred.

In case of a LIN over-current/over-temperature condition the LIN transmitter is disabled. To reenable the LIN transmitter, the error condition must be GONE and the LINWU/LINFAIL flag must be cleared.

The flag is cleared by reading the flag when it is set (SPI command).

HVF —High-voltage Flag Bit

This flag is set on an over-voltage (VSUP1) condition.

- 1 = High-voltage condition has occurred.
- 0 = no High-voltage condition.

LVF/BATFAIL—Low-voltage Flag Bit

This flag is set on an under-voltage (VSUP1) condition.

- 1 = Low-voltage condition has occurred.
- 0 = No low-voltage condition.

VDDT—Voltage Regulator Status Flag Bit

This flag is set as prewarning in case of an over-temperature condition on the voltage regulator.

- 1 = Voltage regulator over-temperature condition, prewarning.
- 0 = No over-temperature detected.

HSST—High Side Status Flag Bit

This flag is set on over-temperature conditions on one of the high side outputs.

- 1 = HSx off due to over-temperature.
- 0 = No over-temperature.

In case one of the high sides has an over-temperature condition all high side switches are disabled.

To reenable the high side switches, the flags have to be cleared, by reading the flag when it is set and by writing a one to high side HSxON bit (two SPI commands are necessary).

L2:L1—Wake-up Inputs L1, L2 Status Flag Bit

These flags reflect the status of the L2 and L1 input pins and indicate the wake-up source.

- 1 = L2:L1 input high or wake-up by L2:L1 (first register read after wake-up indicated with INTSRC = 1).
- 0 = L2:L1 input low.

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale website: www.freescale.com.

VSUP Pins (VSUP1 and VSUP2)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN Pin

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) it is recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU Digital Supply Pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU Analog Supply Pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins it is important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 20 and Figure 21 show the recommendations on schematics and layout level and Table 15 indicates recommended external components and layout considerations.

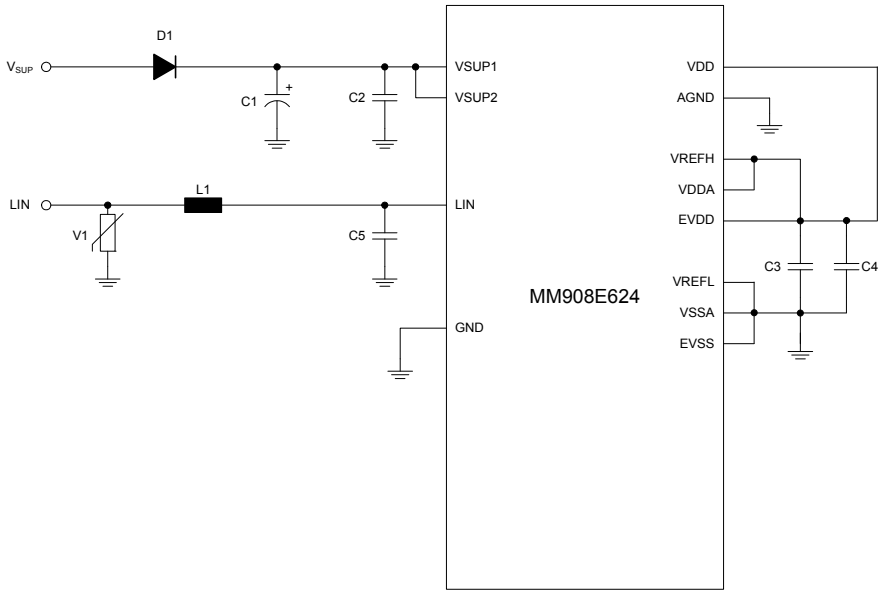


Figure 20. EMC/EMI Recommendations

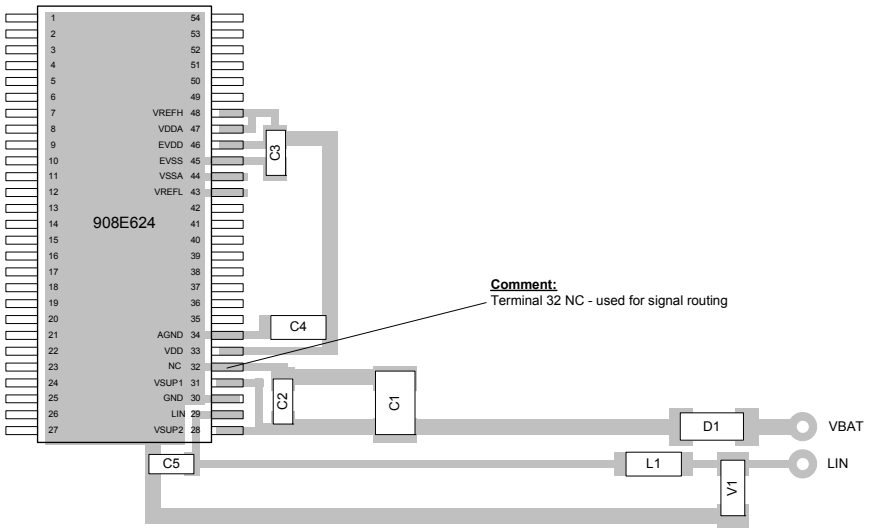


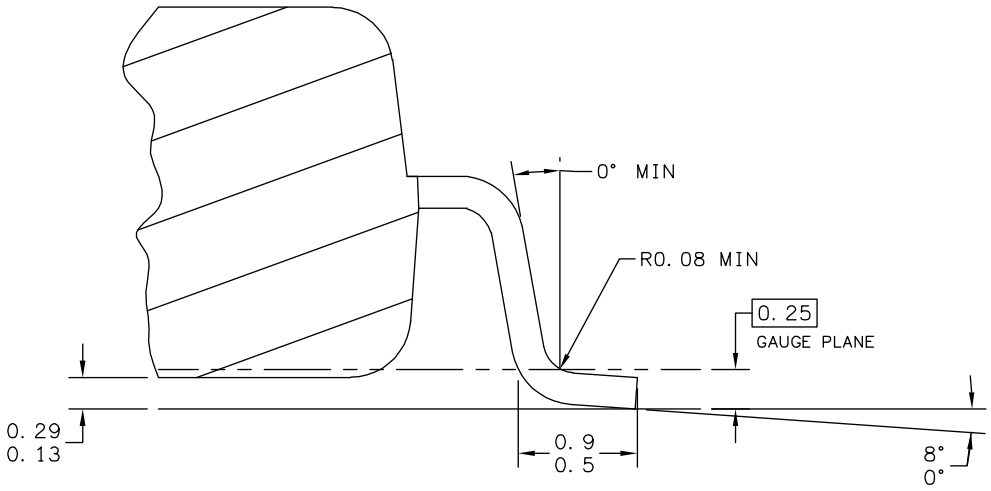
Figure 21. PCB Layout Recommendations

Table 15. Component Value Recommendation

Component	Recommended Value[39]	Comments / Signal routing
D1		Reverse battery protection
C1	Bulk Capacitor	
C2	100 nF, SMD Ceramic	Close (<5.0 mm) to VSUP1, VSUP2 pins with good ground return
C3	100 nF, SMD Ceramic	Close (<3.0 mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4.7 µF, SMD Ceramic or Low ESR	Bulk Capacitor
C5	180 pF, SMD Ceramic	Close (<5.0 mm) to LIN pin. Total Capacitance per LIN node has to be below 220 pF. (C_{TOTAL} = $C_{LIN-PIN}$ + C5 + $C_{VARISTOR}$ ~ 10 pF + 180 pF + 15 pF)
V1[40]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[40]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

Notes

39. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
40. Components are recommended to improve EMC and ESD performance.



SECTION B–B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH CASE–OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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TITLE: 54LD SOIC W/B, 0.65 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

908E624

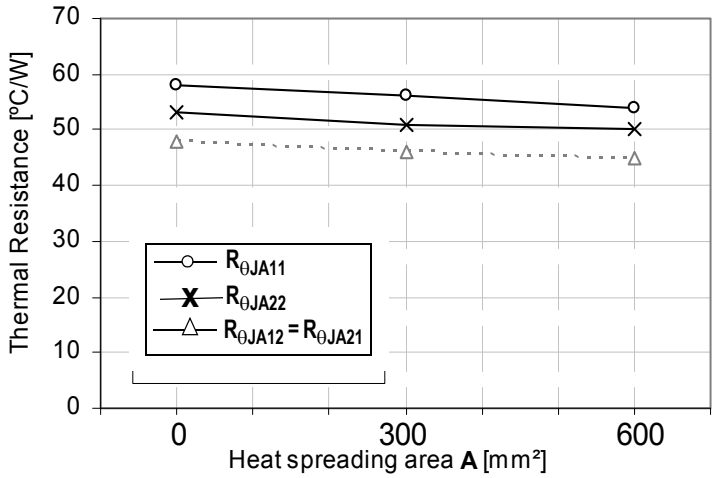

Figure 23. Device on Thermal Test Board

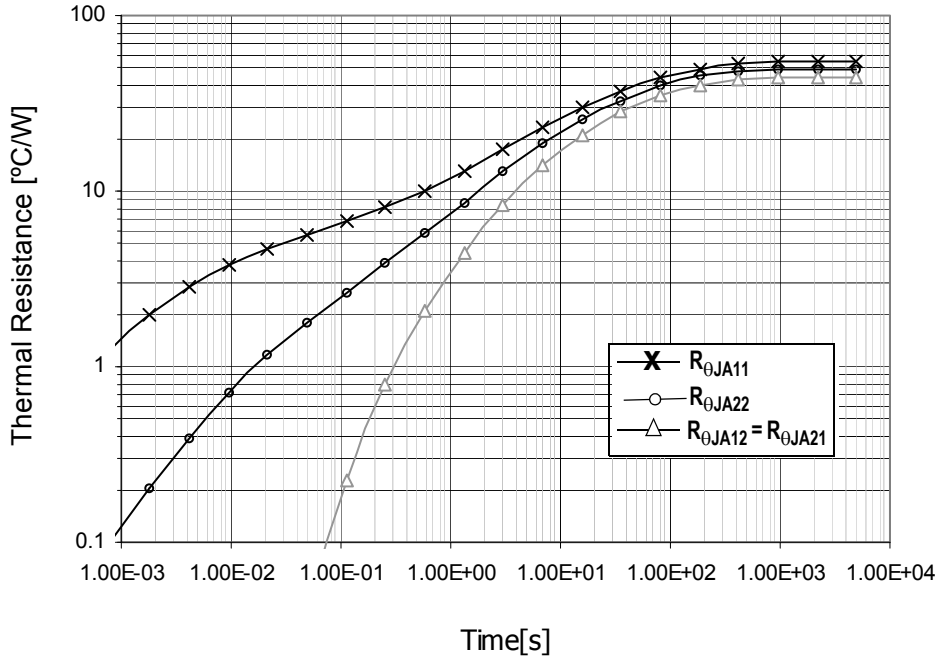

Figure 24. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

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4/2012