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Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	16
Voltage - Supply	5.5V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	54-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e624acpewr2

INTERNAL BLOCK DIAGRAM

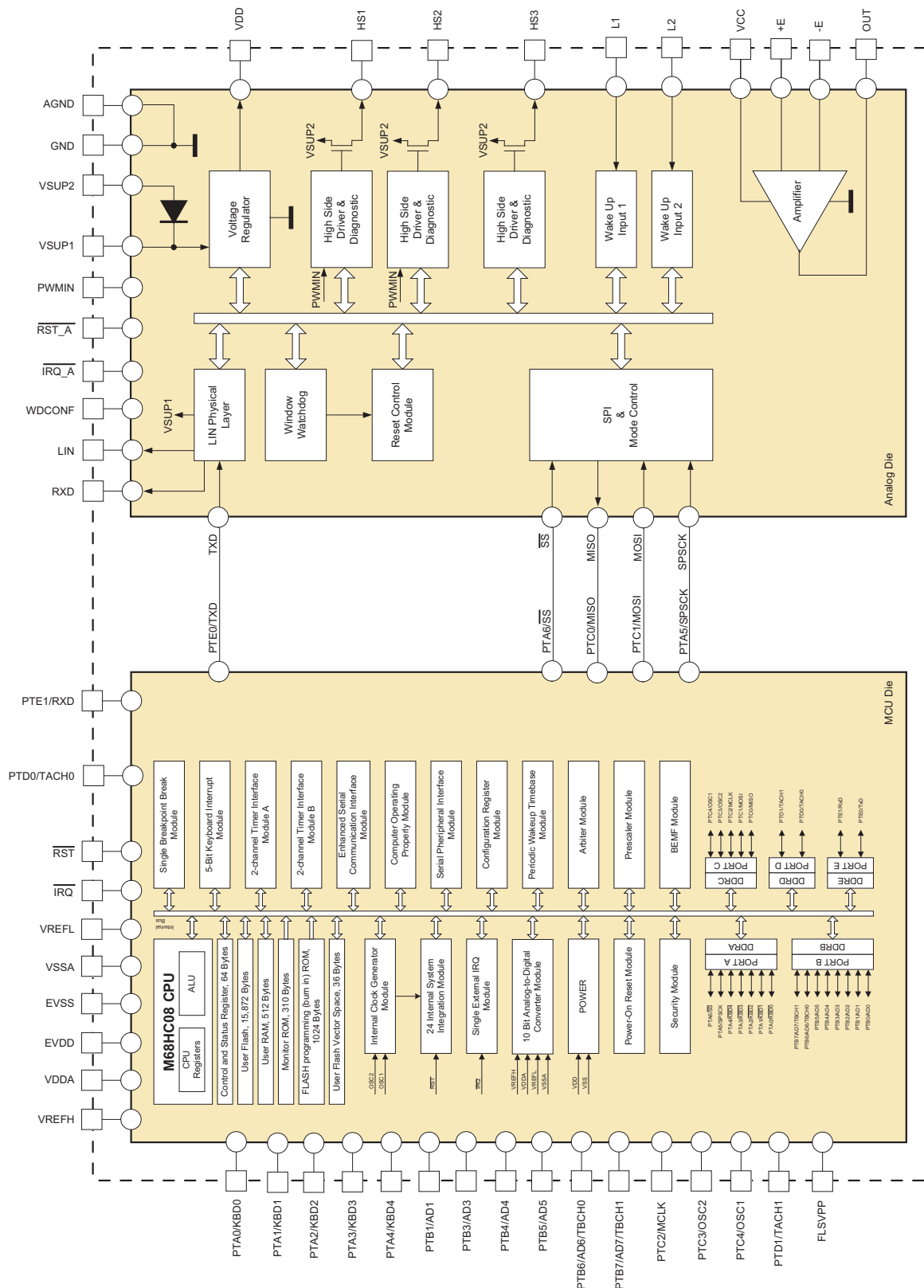


Figure 2. 908E624 Simplified Internal Block Diagram

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on page [16](#).

Die	Pin	Pin Name	Formal Name	Definition
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	17	PWMIN	Direct High Side Control Input	This pin allows the enabling and PWM control of the high side HS1 and HS2 pins.
Analog	18	RST_A	Internal Reset Output	This pin is the reset output pin of the analog die.
Analog	19	IRQ_A	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	23 24	L1 L2	Wake-Up Inputs	These pins are the wake-up inputs of the analog chip.
Analog	25 26 27	HS3 HS2 HS1	High Side Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	31 28	VSUP1 VSUP2	Power Supply Pins	These pins are device power supply pins.
Analog	29	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	30 34	GND AGND	Power Ground Pins	These pins are device power ground connections.
Analog	33	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	35	VCC	Amplifier Power Supply	This pin is the single +5.0 V power supply for the current sense operational amplifier.
Analog	36	OUT	Amplifier Output	This pin is the output of the current sense operational amplifier.
Analog	37 38	-E +E	Amplifier Inputs	These pins are the current sense operational amplifier inverted and non-inverted inputs.
Analog	39	WDCONF	Window Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
Analog	40	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-state)	$V_{SUP(SS)}$	-0.3 to 27	
Analog Chip Supply Voltage under Transient Conditions	$V_{SUP(PK)}$	-0.3 to 40	
MCU Chip Supply Voltage	V_{DD}	-0.3 to 5.5	
Input Pin Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to $V_{DD}+0.3$	
Microcontroller Chip	$V_{IN(MCU)}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	
Maximum Microcontroller Current per Pin			mA
All Pins except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
PTA0:PTA6, PTC0:PTC1 Pins	$I_{PIN(2)}$	±25	
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
Current Sense Operational Amplifier			
Maximum Input Voltage, +E, -E Pins	V_{+E-E}	-0.3 to 7.0	V
Maximum Input Current, +E, -E Pins	I_{+E-E}	±20	mA
Maximum Output Voltage, OUT Pin	V_{OUT}	-0.3 to $V_{CC}+0.3$	V
Maximum Output Current, OUT Pin	I_{OUT}	±20	mA
LIN Supply Voltage			V
Normal Operation (Steady-state)	$V_{BUS(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4 , page 13)	$V_{BUS(PK)}$	-150 to 100	
L1 and L2 Pin Voltage			V
Normal Operation with a 33 kΩ resistor (Steady-state)	$V_{WAKE(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4 , page 13)	$V_{WAKE(PK)}$	-100 to 100	
ESD Voltage			V
Human Body Model ⁽¹⁾	V_{ESD1}	±2000	
Machine Model ⁽¹⁾	V_{ESD2}	±100	
Charge Device Model ⁽¹⁾	V_{ESD3}	±500	

Notes

- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0$ Ω), and the Charge Device Model, Robotic ($C_{ZAP} = 4.0$ pF).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_{\text{J}} \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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SUPPLY VOLTAGE RANGE

Nominal Operating Voltage	V_{SUP}	5.5	—	18	V
Functional Operating Voltage ⁽⁶⁾	V_{SUPOP}	—	—	27	V

SUPPLY CURRENT RANGE

Normal Mode ⁽⁷⁾ $V_{\text{SUP}} = 13.5\text{ V}$, Analog Chip in Normal Mode, MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	20	—	mA
Stop Mode ^{(7), (8)} $V_{\text{SUP}} = 13.5\text{ V}$, LIN in recessive state	I_{STOP}	—	60	75	μA
Sleep Mode ^{(7), (8)} $V_{\text{SUP}} = 13.5\text{ V}$, LIN in recessive state	I_{SLEEP}	—	35	45	μA

DIGITAL INTERFACE RATINGS (ANALOG DIE)

Output Pin $\overline{\text{RST_A}}$ Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Current ($V_{\text{OUT}} > 3.5\text{ V}$) Pull-down Current Limitation	V_{OL} I_{OH} $I_{\text{OL_MAX}}$	— — -1.5	— 250 —	0.4 — -8.0	V μA mA
Output Pin $\overline{\text{IRQ_A}}$ Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Voltage ($I_{\text{OUT}} = 250\text{ }\mu\text{A}$)	V_{OL} V_{OH}	— 3.85	— —	0.4 —	V
Output Pin RXD Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Voltage ($I_{\text{OUT}} = 250\text{ }\mu\text{A}$) Capacitance ⁽⁹⁾	V_{OL} V_{OH} C_{IN}	— 3.85 —	— — 4.0	0.4 — —	V V pF
Input Pin PWMIN Input Logic Low Voltage Input Logic High Voltage Input Current Capacitance ⁽⁹⁾	V_{IL} V_{IH} I_{IN} C_{IN}	— 3.5 -10 —	— — — 4.0	1.5 — 10 —	V V μA pF
Pin TXD, $\overline{\text{SS}}$ —Pull-up Current	I_{PU}	—	40	—	μA

Notes

- Device is fully functional. All functions are operating. Over-temperature may occur.
- Total current ($I_{\text{VSUP1}} + I_{\text{VSUP2}}$) measured at GND pin.
- Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
- This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

External Resistor Range	R_{EXT}	10	—	100	$\text{k}\Omega$
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) ⁽¹⁴⁾	WD_{CACC}	-15	—	15	%

LIN PHYSICAL LAYER

LIN Transceiver Output Voltage Recessive State, TXD HIGH, $I_{\text{OUT}} = 1.0\text{ }\mu\text{A}$ Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	$V_{\text{LIN_REC}}$ $V_{\text{LIN_DOM}}$	$V_{\text{SUP}} - 1$ —	— —	— 1.4	V
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	$\text{k}\Omega$
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	2.0	—	μA
Output Current Shutdown Threshold	$I_{\text{OV-CUR}}$	50	75	150	mA
Leakage Current to GND VSUP Disconnected, V_{BUS} at 18 V Recessive State, $8.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $8.0\text{ V} \leq V_{\text{BUS}} \leq 18\text{ V}$, $V_{\text{BUS}} \geq V_{\text{SUP}}$ GND Disconnected, $V_{\text{GND}} = V_{\text{SUP}}$, V_{BUS} at -18 V	I_{BUS}	— 0.0 -1.0	1.0 3.0 —	10 20 1.0	μA
LIN Receiver Receiver Threshold Dominant Receiver Threshold Recessive Receiver Threshold Center Receiver Threshold Hysteresis	$V_{\text{BUS_DOM}}$ $V_{\text{BUS_REC}}$ $V_{\text{BUS_CNT}}$ $V_{\text{BUS_HYS}}$	— 0.6 0.475 —	— — 0.5 —	0.4 — 0.525 0.175	V_{SUP}

HIGH SIDE OUTPUTS HS1 AND HS2

Switch On Resistance $T_J = 25\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 150\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 150\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 120\text{ mA}$, $5.5\text{ V} < V_{\text{SUP}} > 9.0\text{ V}$	$R_{\text{DS(ON)}}$	— — —	2.0 — 3.0	2.5 4.5 —	Ω
Output Current Limit	I_{LIM}	300	—	600	mA
Over-temperature Shutdown ^{(15), (16)}	T_{HSSD}	155	—	190	$^{\circ}\text{C}$
Leakage Current	I_{LEAK}	—	—	10	μA
Output Clamp Voltage $I_{\text{OUT}} = -100\text{ mA}$	V_{CL}	-6.0	—	—	V

Notes

14. Watchdog timing period calculation formula: $P_{\text{WD}} = 0.991 \cdot R_{\text{EXT}} + 0.648$ (R_{EXT} in $\text{k}\Omega$ and P_{WD} in ms).
15. This parameter is guaranteed by process monitoring but it is not production tested
16. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUT HS3					
Switch On Resistance $T_J = 25\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 30\text{ mA}$, $5.5\text{ V} < V_{\text{SUP}} > 9.0\text{ V}$	$R_{\text{DS(ON)}}$	— — —	— — —	7.0 10 14	Ω
Output Current Limitation	I_{LIM}	60	100	200	mA
Over-temperature Shutdown (17), (18)	T_{HSSD}	155	—	190	$^{\circ}\text{C}$
Leakage Current	I_{LEAK}	—	—	10	μA

CURRENT SENSE OPERATIONAL AMPLIFIER

Rail-to-Rail Input Voltage	V_{IMC}	-0.1	—	$V_{\text{CC}}+0.1$	V
Output Voltage Range Output Current $\pm 1.0\text{ mA}$ Output Current $\pm 5.0\text{ mA}$	V_{OUT1} V_{OUT2}	0.1 0.3	— —	$V_{\text{CC}}-0.1$ $V_{\text{CC}}-0.3$	V
Input Bias Current	I_{B}	—	—	250	nA
Input Offset Current	I_{O}	-100	—	100	nA
Input Offset Voltage	V_{IO}	-25	—	25	mV

L1 AND L2 INPUTS

Low Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 6.0\text{ V}$ $6.0\text{ V} < V_{\text{SUP}} < 18\text{ V}$ $18\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{THL}	2.0 2.5 2.7	2.5 3.0 3.2	3.0 3.5 3.7	V
High Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 6.0\text{ V}$ $6.0\text{ V} < V_{\text{SUP}} < 18\text{ V}$ $18\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{THH}	2.7 3.0 3.5	3.3 4.0 4.2	3.8 4.5 4.7	V
Hysteresis $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{HYS}	0.5	—	1.3	V
Input Current $-0.2\text{ V} < V_{\text{IN}} < 40\text{ V}$	I_{IN}	-10	—	10	μA

Notes

17. This parameter is guaranteed by process monitoring but it is not production tested
18. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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LIN PHYSICAL LAYER (CONTINUED)

Output Current Shutdown Delay	$t_{\text{OV-DELAY}}$	—	10	—	μs
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SPI INTERFACE TIMING

SPI Operating Recommended Frequency	f_{SPIOP}	0.25	—	4.0	MHz
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L1 AND L2 INPUTS

Wake-up Filter Time ⁽²⁴⁾	t_{WUF}	8.0	20	38	μs
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WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

Watchdog Period	t_{PWD}	—	10.558	—	ms
External Resistor $R_{\text{EXT}} = 10\text{ k}\Omega$ (1%)		—	99.748	—	
External Resistor $R_{\text{EXT}} = 100\text{ k}\Omega$ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Pin Open)		97	150	205	

STATE MACHINE TIMING

Reset Low Level Duration after V_{DD} High ⁽²⁸⁾	t_{RST}	0.65	1.0	1.35	ms
Interrupt Low Level Duration	t_{INT}	7.0	10	13	μs
Normal Request Mode Timeout ⁽²⁸⁾	t_{NRTOU}	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On ^{(25), (26)}	$t_{\text{S-HSON}}$	—	3.0	10	μs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off ^{(25), (26)}	$t_{\text{S-HSOFF}}$	—	3.0	10	μs
Delay Between Normal Request and Normal Mode After W/D Trigger Command ⁽²⁷⁾	$t_{\text{S-NR2N}}$	6.0	35	70	μs
Delay Between $\overline{\text{SS}}$ Wake-Up ($\overline{\text{SS}}$ LOW to HIGH) and Normal Request Mode (V_{DD} On and Reset High)	$t_{\text{W-SS}}$	15	40	80	μs
Delay Between $\overline{\text{SS}}$ Wake-Up ($\overline{\text{SS}}$ LOW to HIGH) and First Accepted SPI Command	$t_{\text{W-SPI}}$	90	—	N/A	μs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{\text{S-1STSPI}}$	30	—	N/A	μs
Minimum Time Between Two Rising Edges on $\overline{\text{SS}}$	$t_{2\overline{\text{SS}}}$	15	—	—	μs

Notes

24. This parameter is guaranteed by process monitoring but is not production tested.
25. Delay between turn-on or turn-off command and high side on or high side off, excluding rise or fall time due to external load.
26. Delay between the end of the SPI command (rising edge of the $\overline{\text{SS}}$) and start of device activation/deactivation.
27. This parameter is guaranteed by process monitoring but it is not production tested.
28. Also see [Figure 10](#) on page [15](#)

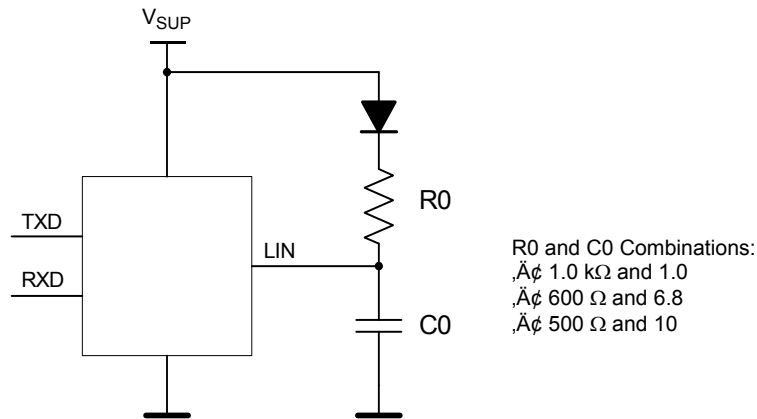


Figure 5. Test Circuit for LIN Timing Measurements

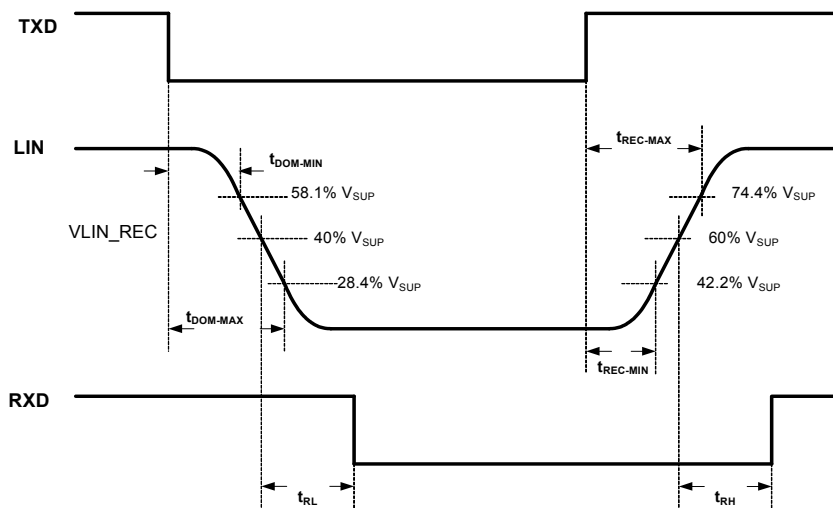


Figure 6. LIN Timing Measurements for Normal Slew Rate

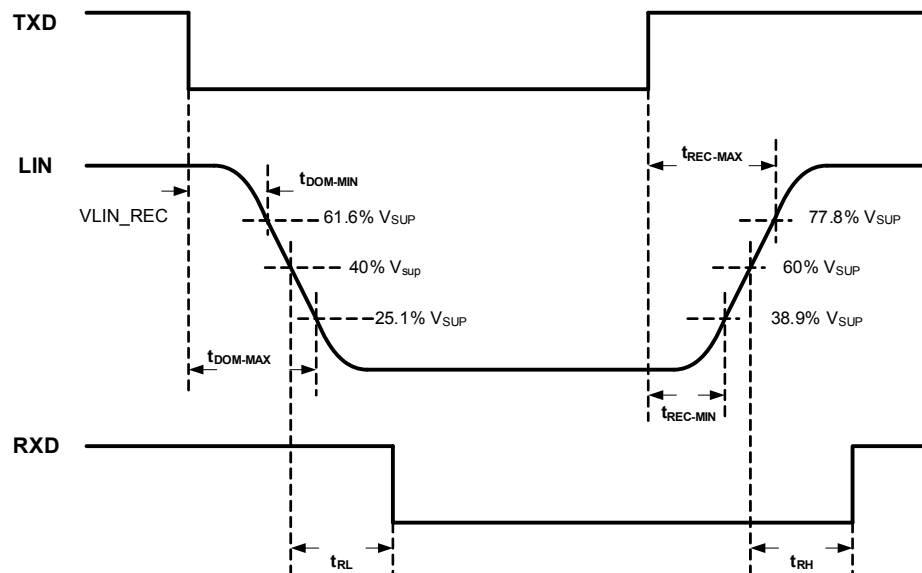


Figure 7. LIN Timing Measurements for Slow Slew Rate

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	RST_A Output	Watchdog Function	HS1, HS2, and HS3	LIN Interface	Sense Amplifier
Reset	V _{DD} ON	N/A	LOW	Disabled	Disabled	Recessive only	Not active
Normal Request	V _{DD} ON	N/A	HIGH	150 ms time out if WD enabled	Enabled	Transmit and receive	Not active
Normal (Run)	V _{DD} ON	N/A	HIGH	Window WD if enabled	Enabled	Transmit and receive	Active
Stop	V _{DD} ON with limited current capability	LIN wake-up, L1, L2 state change, SS rising edge	HIGH	Disabled	Disabled	Recessive state with wake-up capability	Not active
Sleep	V _{DD} OFF	LIN wake-up L1, L2 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability	Not active

INTERRUPTS

In Normal (Run) mode the 908E624 has four different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ_A}}$ pin is generated to report a fault to the MCU. All interrupts are not maskable and cannot be disabled.

After an Interrupt the INTSRC bit in the SPI Status register is set, indicating the source of the event. This interrupt source information is only transferred once, and the INTSRC bit is cleared automatically.

Low-Voltage Interrupt

Low-voltage interrupt (LVI) is related to external supply voltage VSUP1. If this voltage falls below the LVI threshold, it will set the LVF bit in the SPI Status register and an interrupt will be initiated. The LVF bit remains set as long as the Low-voltage condition is present.

During Sleep and Stop mode the low-voltage interrupt circuitry is disabled.

High-voltage Interrupt

High-voltage interrupt (HVI) is related to external supply voltage VSUP1. If this voltage rises above the HVI threshold, it will set the HVF bit in the SPI Status register and an interrupt will be initiated. The HVF bit remains set as long as the high-voltage condition is present.

During Sleep and Stop mode the high-voltage interrupt circuitry is disabled.

Wake-up Interrupts

In Stop mode the $\overline{\text{IRQ_A}}$ pin reports wake-up events on the L1, L2, or the LIN bus to the MCU. All wake-up interrupts are not maskable and cannot be disabled.

After a wake-up interrupt, the INTSRC bit in the Serial Peripheral Interface (SPI) Status register is set, indicating the source of the event. This wake-up source information is only transferred once, and the INTSRC bit is cleared automatically.

[Figure 12](#), page 21, describes the Stop/Wake-up procedure.

Voltage Regulator Temperature Prewarning (VDDT)

Voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Status register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop mode the voltage regulator temperature prewarning circuitry is disabled.

High Side Switch Thermal Shutdown (HSST)

The high side switch thermal shutdown HSST is generated if one of the high side switches HS1:HS3 is above the HSST threshold, it will shutdown all high side switches, set the HSST flag in the SPI Status register and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present.

During Sleep and Stop mode the high side switch thermal shutdown circuitry is disabled.

Sleep and Stop Mode

In Sleep and Stop modes the high sides are disabled.

High Side Output HS3

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done using the SPI Control register. No direct PWM control is possible on this pin (refer to [Figure 14](#), page 22).

Current Limit (Over-current) Protection

This high side feature switch feature current limit to protect it against over-current and short-circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop mode the high side is disabled.

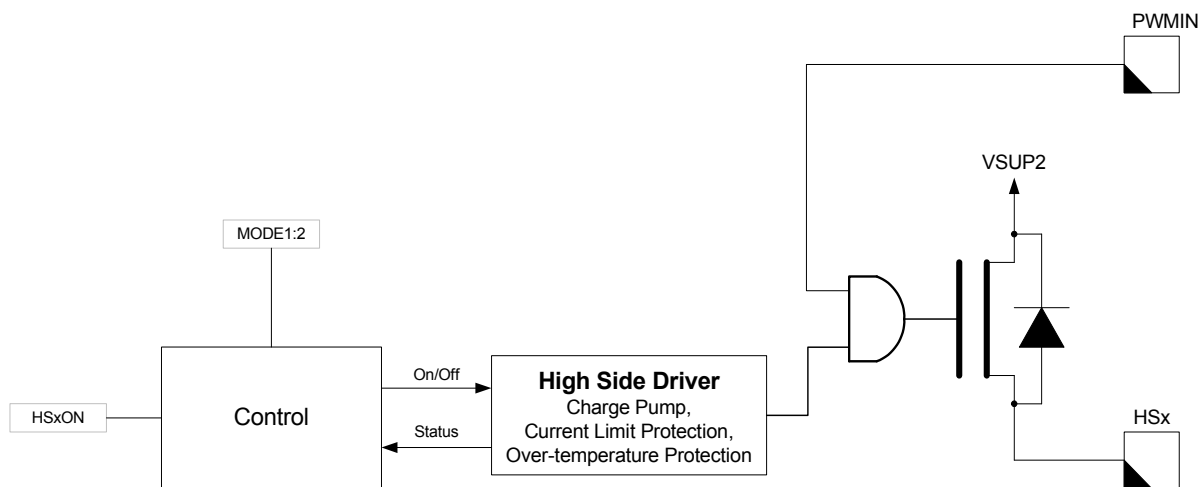


Figure 13. High Side HS1 and HS2 Circuitry

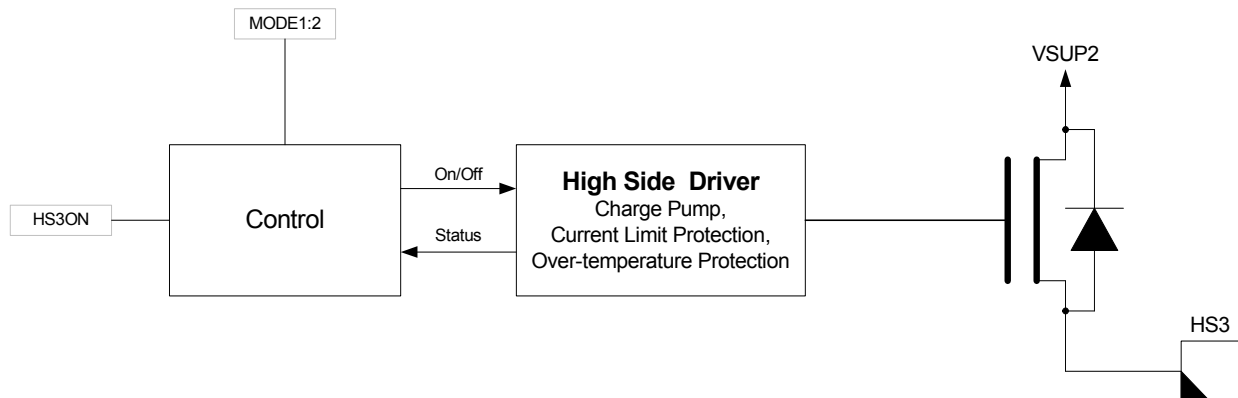


Figure 14. High Side HS3 Circuitry

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with over-current protection and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave

node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LINS2:1 in the SPI Control Register. The initial slew rate is optimized for 20 kBit/s.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled in Normal and Normal Request mode.

An over-current condition (e.g. LIN bus short to V_{BAT}) or a over-temperature in the output low side FET will shutdown

the transmitter and set the LINFAIL flag in the SPI Status Register.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN pin can be disconnected, with the LIN-PU bit in the SPI Control Register, and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

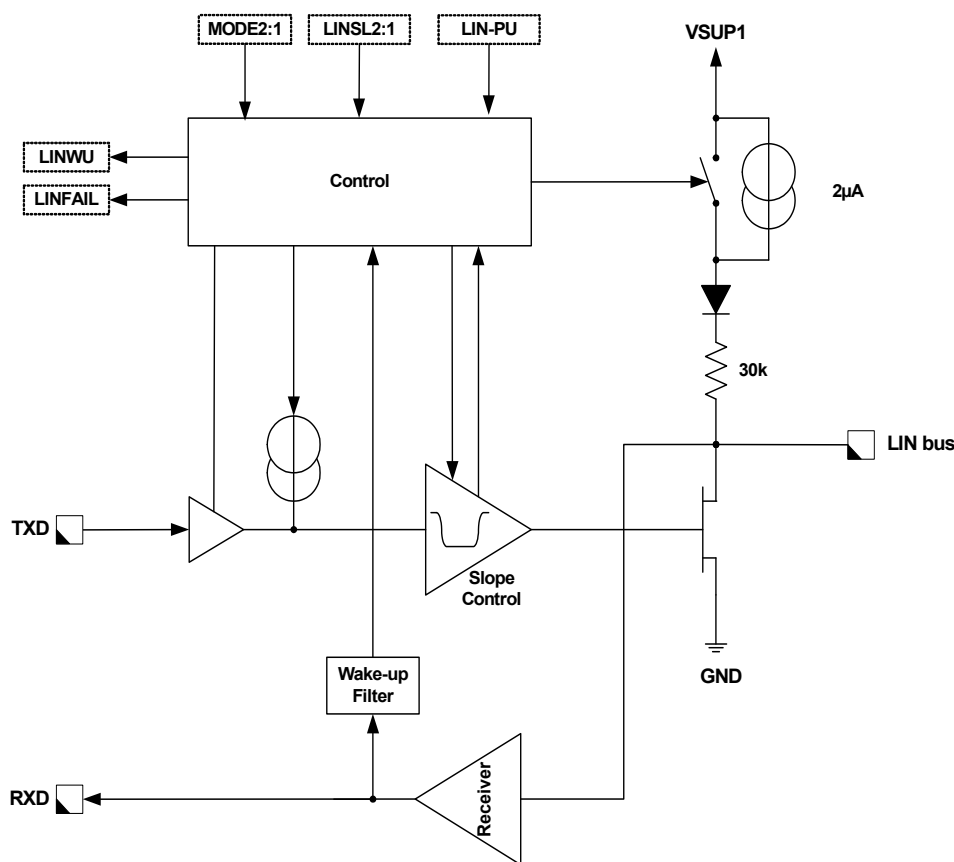


Figure 15. LIN Interface

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see [Figure 2](#), page 2). When TXD is LOW, the LIN pin is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD pin has an internal pull-up current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a wake-up interrupt and set the LINWF flag in the SPI Status Register. Also see [Figure 9](#), page 15.

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is

disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register. Also see [Figure 8](#), page [15](#).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF pin. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to [Table 8](#), page [26](#)).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST_A}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

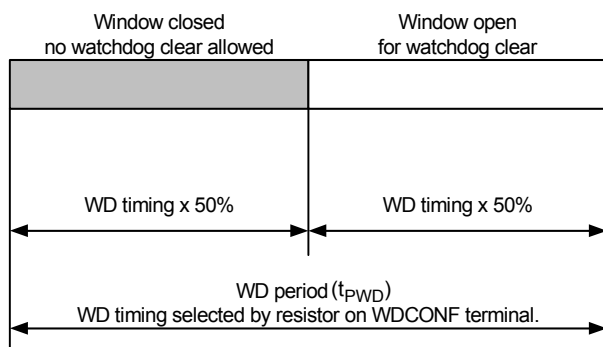


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF pin must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD} [\text{ms}] = 0.991 * R_{EXT} [\text{k}\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Over-current) Protection

The voltage regulator has current limit to protect the device against over-current and short-circuit conditions.

Over-temperature Protection

The voltage regulator also features an over-temperature protection having an over-temperature warning (Interrupt - VDDT) and an over-temperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease of use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the "empty" (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as $\pm 25\%$, due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at the address \$FDC2. After trimming the ICG, a range of typ. $\pm 2\%$ ($\pm 3\%$ max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 μF) $V_{DD} = 5.0 \text{ V}$, $T_{\text{Ambient}} \sim 23^\circ\text{C}$) and will vary over-temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values must be copied to the ICG Trim Register ICGTR at address \$38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

Table 7. SPI Register Overview

Read/Write Information	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
Write	LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
Read	INTSRC ⁽³⁰⁾	LINWU or LINFAIL	HVF	LVF or BATFAIL ⁽³¹⁾	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes

30. D7 signals interrupts and wake-up interrupts, D6:D0 indicated the source.
31. The first SPI read after reset returns the BATFAIL flag state on bit D4.

SPI Control Register (Write)

[Table 8](#) shows the SPI Control register bits by name.

Table 8. Control Bits Function (Write Operation)

D7	D6	D5	D4	D3	D2	D1	D0
LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1

LINSL2:1—LIN Baud Rate and Low-power Mode Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with [Table 9](#). Reset clears the LINSL2:1 bits.

Table 9. LIN Baud Rate and Low-power Mode Selection Bits

LINSL2	LINSL1	Description
0	0	Baud Rate up to 20 kbps (normal)
0	1	Baud Rate up to 10 kbps (slow)
1	0	Fast Program Download Baud Rate up to 100 kbps
1	1	Low-power Mode (Sleep or Stop) Request

LIN-PU—LIN Pull-up Enable Bit

This bit controls the LIN pull-up resistor during Sleep and Stop modes.

- 1 = Pull-up disconnected in Sleep and Stop modes.
- 0 = Pull-up connected in Sleep and Stop modes.

If the Pull-up is disconnected, a small current source is used to pull the LIN pin in recessive state. In case of an erroneous short of the LIN bus to ground, this will significantly

reduce the power consumption, e.g. in combination with STOP/SLEEP mode.

HS3ON:HS1ON—High Side H3:HS1 Enable Bits

These bits enable the HSx. Reset clears the HSxON bit.

- 1 = HSx switched on (refer to Note below).
- 0 = HSx switched off.

Note If no PWM on HS1 and HS2 is required, the PWMIN pin must be connected to the VDD pin.

MODE2:1—Mode Selection Bits

The MODE2:1 bits control the operating modes and the watchdog in accordance with [Table 10](#).

Table 10. Mode Selection Bits

MODE2	MODE1	Description
0	0	Sleep Mode ⁽³²⁾
0	1	Stop Mode ⁽³²⁾
1	0	Watchdog Clear ⁽³³⁾
1	1	Run (Normal) Mode

Notes

32. To enter Sleep and Stop mode, a special sequence of SPI commands is implemented.
33. The device stays in Run (Normal) mode.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence

The Sleep command, as shown in [Table 11](#), must be sent twice.

Table 11. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	0

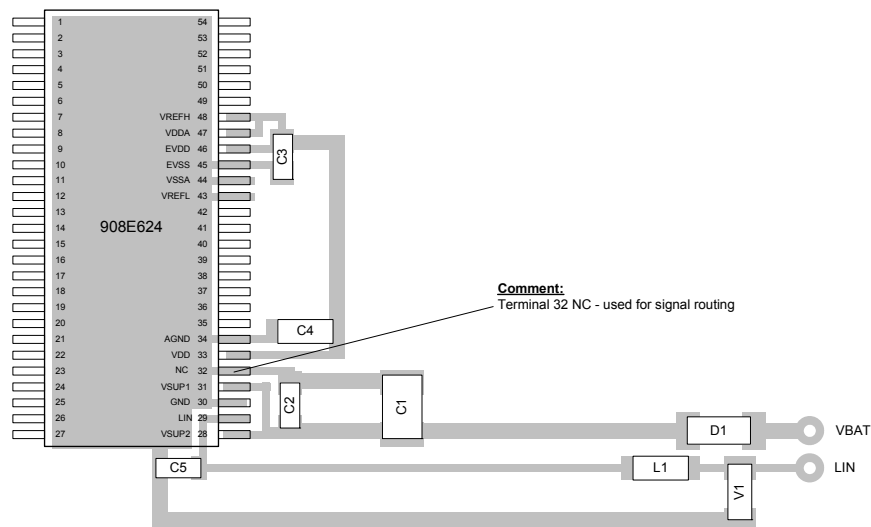


Figure 21. PCB Layout Recommendations

Table 15. Component Value Recommendation

Component	Recommended Value ⁽³⁹⁾	Comments / Signal routing
D1		Reverse battery protection
C1	Bulk Capacitor	
C2	100 nF, SMD Ceramic	Close (<5.0 mm) to VSUP1, VSUP2 pins with good ground return
C3	100 nF, SMD Ceramic	Close (<3.0 mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4.7 μF, SMD Ceramic or Low ESR	Bulk Capacitor
C5	180 pF, SMD Ceramic	Close (<5.0 mm) to LIN pin. Total Capacitance per LIN node has to be below 220 pF. ($C_{TOTAL} = C_{LIN-PIN} + C5 + C_{VARISTOR} \sim 10 \text{ pF} + 180 \text{ pF} + 15 \text{ pF}$)
V1 ⁽⁴⁰⁾	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1 ⁽⁴⁰⁾	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

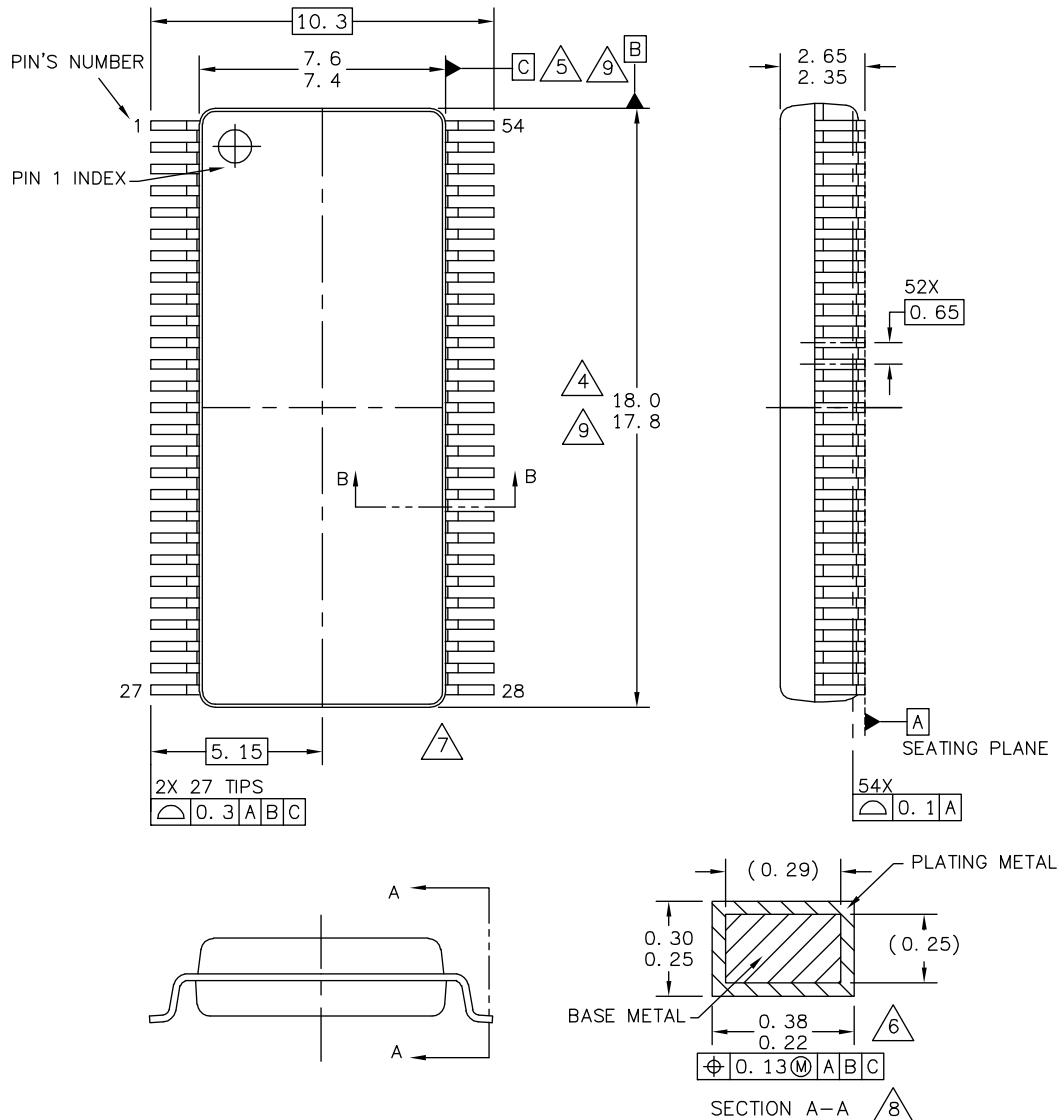
Notes

39. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
40. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ASA99294D drawing number below. Dimensions shown are provided for reference ONLY.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 54LD SOIC W/B, 0.65 PITCH CASE-OUTLINE		DOCUMENT NO: 98ASA99294D		REV: B	
		CASE NUMBER: 1365-01		12 APR 2005	
		STANDARD: NON-JEDEC			

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 3.0)

INTRODUCTION

This thermal addendum is provided as a supplement to the MM908E624 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MM908E624 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2 . This results in two junction temperatures, T_{J1} and T_{J2} , and a thermal resistance matrix with $R_{\theta JA mn}$.

For $m, n = 1$, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1 .

For $m = 1, n = 2$, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2 . This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below

Standards

Table 16. Thermal Performance Comparison

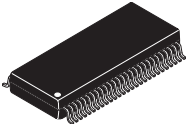
Thermal Resistance	1 = Power Chip, 2 = Logic Chip [$^{\circ}\text{C}/\text{W}$]		
	$m = 1, n = 1$	$m = 1, n = 2$ $m = 2, n = 1$	$m = 2, n = 2$
$R_{\theta JA mn}$ ⁽¹⁾⁽²⁾	40	31	36
$R_{\theta JB mn}$ ⁽²⁾⁽³⁾	25	16	21
$R_{\theta JA mn}$ ⁽¹⁾⁽⁴⁾	57	47	52
$R_{\theta JC mn}$ ⁽⁵⁾	21	12	16

Notes:

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, "infinite" heat sink attached to exposed pad.

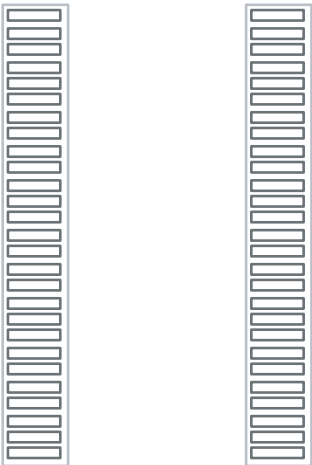
908E624

**54-Pin
SOICW**



**EW (Pb-FREE) SUFFIX
98ASA99294D
54-Pin SOICW**

Note For package dimensions, refer to 98ASA99294D.



54 Terminal SOIC
0.65 mm Pitch
17.9 mm x 7.5 mm Body

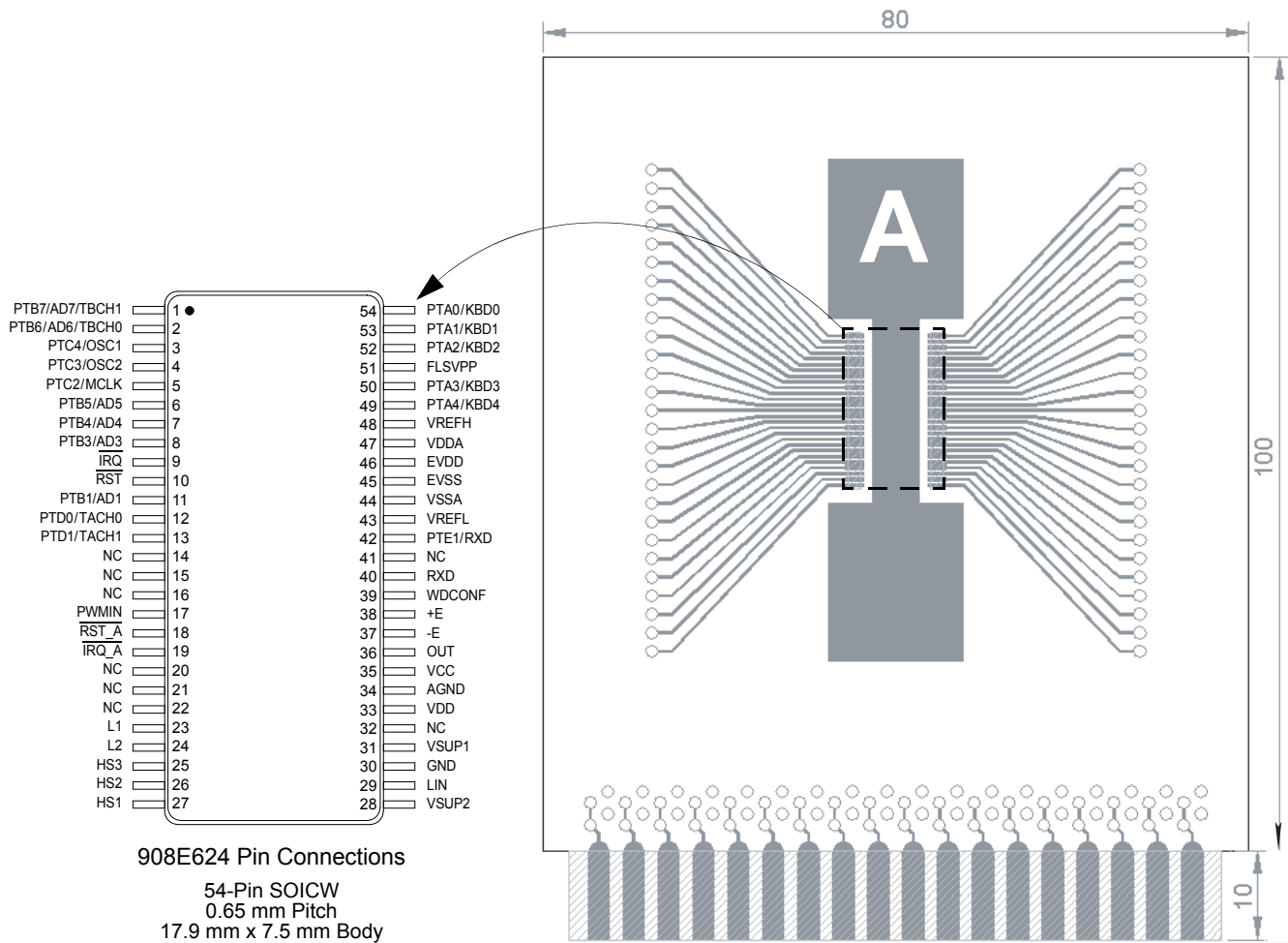


Figure 22. Surface Mount for SOIC Wide Body
Non-exposed Pad

Device on Thermal Test Board

Material: Single layer printed circuit board
FR4, 1.6 mm thickness
Cu traces, 0.07 mm thickness

Outline: 80 mm x 100 mm board area,
including edge connector for thermal
testing

Area A: Cu heat-spreading areas on board
surface

Ambient Conditions: Natural convection, still air

Table 17. Thermal Resistance Performance

Pin Resistance	Area A (mm ²)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		$m = 1, n = 1$	$m = 1, n = 2$ $m = 2, n = 1$	$m = 2, n = 2$
$R_{\theta JA mn}$	0	58	48	53
	300	56	46	51
	600	54	45	50

$R_{\theta JA mn}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index m indicates the die that is heated. Index n refers to the number of the die where the junction temperature is sensed.

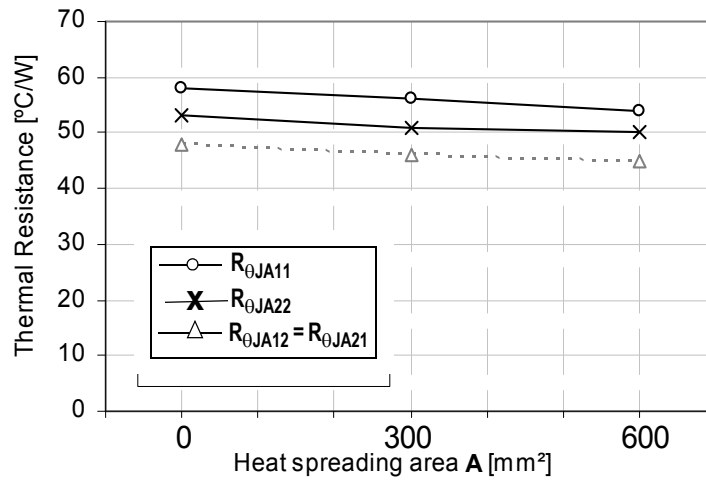


Figure 23. Device on Thermal Test Board

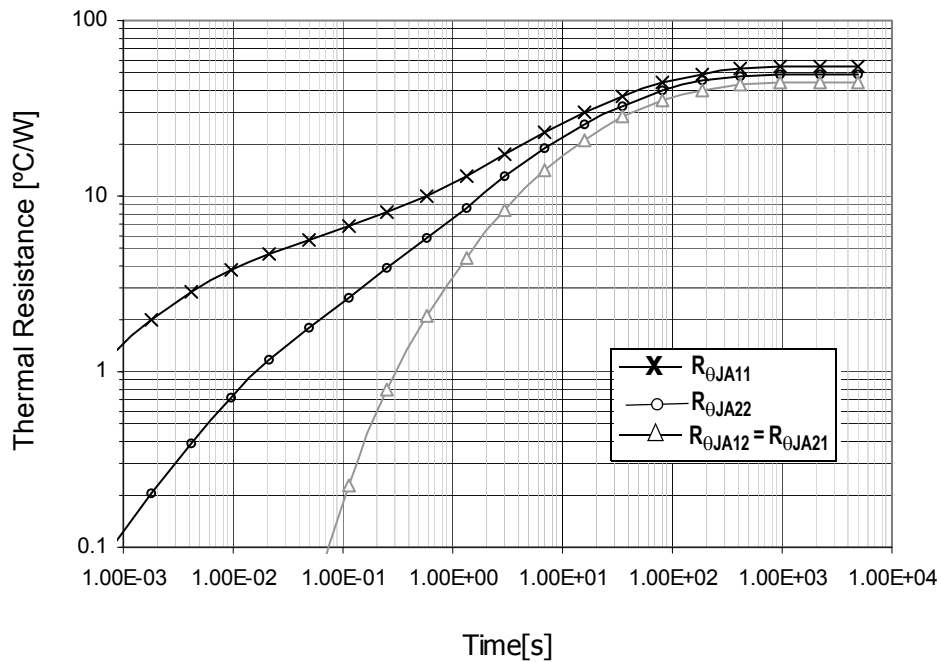


Figure 24. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm²)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	5/2006	<ul style="list-style-type: none"> Implemented Revision History page Added Pb-Free package option (Suffix EW) and higher Soldering temperature Added "Y" temperature (T_J -40°C to 125°C) code option (MM908E624AYEW) and updated condition statement for Static and Dynamic Electrical Characteristics Corrected Figure 11, Operating Modes and Transitions ("STOP command" for transition from Normal to Stop state) Updated Figure 21, PCB Layout Recommendations, comment NC Pin used for signal routing Updated Table 15, Component Value Recommendation Corrected Figure 23, Device on Thermal Test Board Removed reference to Note 11, Voltage Regulator - Dropout Voltage Added comment "LIN in recessive state" to Supply Current Range in Stop Mode and Sleep Mode Updated format to match current data sheet standard. Added Figure 10, Power On Reset and Normal Request Timeout Timing Added LIN P/L details Made clarifications on Max Ratings Table for T_A and T_J Thermal Ratings and the accompanying Note
8.0	3/2007	<ul style="list-style-type: none"> Removed "Advance Information" watermark from first page.
9.0	9/2010	<ul style="list-style-type: none"> Changed Peak Package Reflow Temperature During Reflow⁽³⁾⁽⁵⁾ description. Added note ⁽⁵⁾
10.0	8/2011	<ul style="list-style-type: none"> Deleted MM908E624ACDWB/R2 Added MM908E624ACPEW/R2 and MM908E624AYPEW/R2 Update Freescale form and style. Updated package drawing
11.0	4/2012	<ul style="list-style-type: none"> Removed part number MM908E624ACEW/ R2 and MM908E624AYEW/ R2. Update Freescale form and style.

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