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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	16
Voltage - Supply	5.5V ~ 18V
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	54-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	54-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e624aypewr2

PIN CONNECTIONS

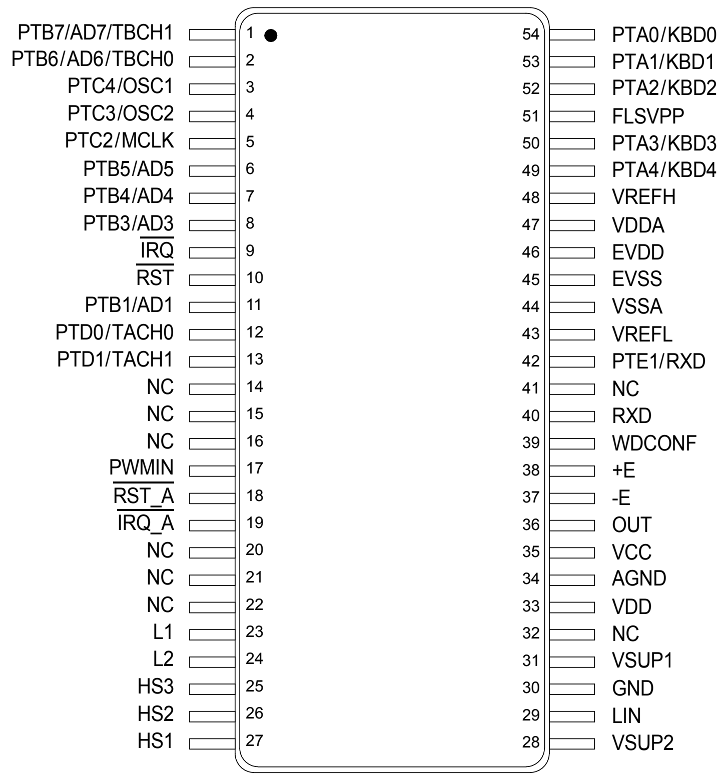


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 16.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0 PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
—	14, 15, 16, 20, 21, 22, 32, 41	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin, that can is shared with other functional modules in the MCU.

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Package Operating Ambient Temperature [(4)] MM908E624ACPEW MM908E624AYPEW	T_A	 -40 to 85 -40 to 125	°C
Operating Junction Temperature [(2)(4)] MM908E624ACPEW MM908E624AYPEW	T_J	 -40 to 125 -40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[(3)(5)]	T_{PPRT}	Note 5	°C

Notes

2. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation of the analog die. The analog die junction temperature must not exceed 150°C under these conditions.
3. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Independent of $T_{A,}$ device parametrics are only guaranteed for -40 < T_J < 125 °C. Please see note 2. T_J is a factor of power dissipation, package thermal resistance, and available heat sinking.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\leq V_{SUP} \leq$ 16 V, -40 °C $\leq T_J \leq$ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low-voltage Reset (LVR) Threshold	V_{LVRON}	3.6	4.0	4.4	V
Low-voltage Interrupt (LVI) Threshold Hysteresis	V_{LVI} V_{LVI_HYS}	5.7 —	6.0 1.0	6.6 —	V
High-voltage Interrupt (HVI) Threshold Hysteresis	V_{HVI} V_{HVI_HYS}	18 —	19.25 220	20.5 —	V mV
VOLTAGE REGULATOR (10)					
Normal Mode Output Voltage 2.0 mA < I_{DD} < 50 mA, 5.5 V < V_{SUP} < 27 V	V_{DDRUN}	4.75	5.0	5.25	V
Normal Mode Output Current Limitation (11)	I_{DDRUN}	50	110	200	mA
Dropout Voltage V_{SUP} = 4.9 V, I_{DD} = 50 mA	V_{DDDROP}	—	0.1	0.2	V
Stop Mode Output Voltage (12)	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Regulator Current Limitation	I_{DDSTOP}	4.0	8.0	14	mA
Line Regulation Normal Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA Stop Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	V_{LRRUN} V_{LRSTOP}	— —	20 10	150 100	mV
Load Regulation Normal Mode, 1.0 mA < I_{DD} < 50 mA, V_{SUP} = 18 V Stop Mode, 1.0 mA < I_{DD} < 5.0 mA, V_{SUP} = 18 V	V_{LRRUN} V_{LDSTOP}	— —	40 40	150 150	mV
Over-temperature Prewarning (Junction) (13)	T_{PRE}	120	135	160	°C
Thermal Shutdown Temperature (Junction) (13)	T_{SD}	155	170	—	°C
Temperature Threshold Difference T_{SD}-T_{PRE}	ΔT_{SD}-T_{PRE}	20	30	45	°C

Notes

10. Specification with external capacitor 2.0 μF< C < 10 μF and 200 mΩ ≤ ESR ≤ 10 Ω. Capacitor value up to 47 μF can be used.
11. Total V_{DD} regulator current. A 5.0 mA current for current sense operational amplifier is included. Digital output supplied from VDD.
12. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.
13. This parameter is guaranteed by process monitoring but not production tested

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\leq V_{SUP} \leq$ 16 V, -40 °C $\leq T_J \leq$ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
External Resistor Range	R_{EXT}	10	—	100	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) (14)	WD_{CACC}	-15	—	15	%
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage Recessive State, TXD HIGH, I_{OUT} = 1.0 µA Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	 V_{LIN_REC} V_{LIN_DOM}	 V_{SUP}-1 —	 — —	 — 1.4	V
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	2.0	—	µA
Output Current Shutdown Threshold	$I_{OV\text{-}CUR}$	50	75	150	mA
Leakage Current to GND VSUP Disconnected, V_{BUS} at 18 V Recessive State, 8.0 V $\leq V_{SUP} \leq$ 18 V, 8.0 V$\leq V_{BUS} \leq$ 18 V, $V_{BUS} \geq V_{SUP}$ GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V	I_{BUS}	 — 0.0 -1.0	 1.0 3.0 —	 10 20 1.0	µA
LIN Receiver Receiver Threshold Dominant Receiver Threshold Recessive Receiver Threshold Center Receiver Threshold Hysteresis	 V_{BUS_DOM} V_{BUS_REC} V_{BUS_CNT} V_{BUS_HYS}	 — 0.6 0.475 —	 — — 0.5 —	 0.4 — 0.525 0.175	V_{SUP}
HIGH SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} > 9.0 V	$R_{DS(ON)}$	 — — —	 2.0 — 3.0	 2.5 4.5 —	Ω
Output Current Limit	I_{LIM}	300	—	600	mA
Over-temperature Shutdown (15), (16)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	µA
Output Clamp Voltage I_{OUT} = -100 mA	V_{CL}	 -6.0	 —	 —	V

Notes

14. Watchdog timing period calculation formula: P_{WD} = 0.991 * R_{EXT}+0.648 (R_{EXT} in kΩ and P_{WD} in ms).
15. This parameter is guaranteed by process monitoring but it is not production tested
16. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate [19], [20]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1	-10.44	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2	—	—	11	µs
Driver Characteristics for Slow Slew Rate [19], [21]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	DT1S	-22	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	DT2S	—	—	23	µs
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	15	—	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay [22]	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay [22]	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	$t_{PROP}WL$	35	—	150	µs
Bus Wake-up Event Reported [23]	t_{WAKE}	—	20	—	µs

Notes

19. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
20. See Figure 6, page 14.
21. See Figure 7, page 14.
22. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
23. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 8 and Figure 9, page 15. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD pin.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER (CONTINUED)					
Output Current Shutdown Delay	$t_{OV\text{-}DELAY}$	—	10	—	µs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	f_{SPIOP}	0.25	—	4.0	MHz
L1 AND L2 INPUTS					
Wake-up Filter Time [24]	t_{WUF}	8.0	20	38	µs
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
Watchdog Period	t_{PWD}				ms
External Resistor R_{EXT} = 10 kΩ (1%)		—	10.558	—	
External Resistor R_{EXT} = 100 kΩ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Pin Open)		97	150	205	
STATE MACHINE TIMING					
Reset Low Level Duration after V_{DD} High [28]	$t_{\overline{RST}}$	0.65	1.0	1.35	ms
Interrupt Low Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Normal Request Mode Timeout [28]	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On [25], [26]	$t_{S\text{-}HSON}$	—	3.0	10	µs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off [25], [26]	$t_{S\text{-}HSOFF}$	—	3.0	10	µs
Delay Between Normal Request and Normal Mode After W/D Trigger Command [27]	$t_{S\text{-}NR2N}$	6.0	35	70	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and Normal Request Mode (VDD On and Reset High)	$t_{W\text{-}\overline{SS}}$	15	40	80	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and First Accepted SPI Command	$t_{W\text{-}SPI}$	90	—	N/A	µs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{S\text{-}1STSPI}$	30	—	N/A	µs
Minimum Time Between Two Rising Edges on $\overline{SS}$	$t_{2\overline{SS}}$	15	—	—	µs

Notes
24. This parameter is guaranteed by process monitoring but is not production tested.
25. Delay between turn-on or turn-off command and high side on or high side off, excluding rise or fall time due to external load.
26. Delay between the end of the SPI command (rising edge of the $\overline{SS}$) and start of device activation/deactivation.
27. This parameter is guaranteed by process monitoring but it is not production tested.
28. Also see Figure 10 on page 15

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\le V_{SUP} \le$ 16 V, -40 °C $\le T_J \le$ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Supply Voltage Rejection Ratio [(29)]	SVR	60	—	—	dB
Common Mode Rejection Ratio [(29)]	CMR	70	—	—	dB
Gain Bandwidth [(29)]	GBP	1.0	—	—	MHz
Slew Rate	SR	0.5	—	—	V/μs
Phase Margin (for Gain = 1, Load 100 pF / 5.0 kΩ [(29)]	PHMO	40	—	—	°
Open Loop Gain	OLG	—	85	—	dB

Notes
29. This parameter is guaranteed by process monitoring but it is not production tested.

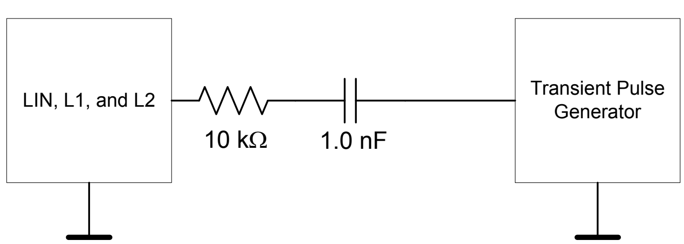
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 data sheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note Waveform in accordance with ISO7637 Part 1, Test Pulses 1, 2, 3a, and 3b.

Figure 4. Test Circuit for Transient Test Pulses

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details, refer to the 68HC908EY16 data sheet.

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSSA via separate traces.

For details, refer to the 68HC908EY16 data sheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. Do not connect in the application or connect to GND.

PWMIN PIN (PWMIN)

This pin is the direct PWM input for high side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD to enable the HS1 and HS2 outputs.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

RESET PIN ($\overline{RST\_A}$)

$\overline{RST\_A}$ is the reset output pin of the analog die and must be connected to the $\overline{RST}$ pin of the MCU.

Important To ensure proper operation, do not add any external pull-up resistor.

INTERRUPT PIN ($\overline{IRQ\_A}$)

$\overline{IRQ\_A}$ is the interrupt output pin of the analog die indicating errors or wake-up events. This pin must be connected to the $\overline{IRQ}$ pin of the MCU.

WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

This pin is the configuration pin for the internal watchdog. A resistor is connected to this pin. The resistor value defines the watchdog period. If the pin is open, the watchdog period is fixed to its default value.

The watchdog can be disabled (e.g., for flash programming or software debugging) by connecting this pin to GND.

POWER SUPPLY PINS (VSUP1 AND VSUP2)

This VSUP1 power supply pin supplies the voltage regulator, the internal logic, and LIN transceiver.

This VSUP2 power supply pin is the positive supply for the high side switches.

POWER GROUND PIN (GND)

This pin is the device ground connection.

HIGH SIDE OUTPUT PINS (HS1 AND HS2)

These pins are high side switch outputs to drive loads such as relays or lamps. Each switch is protected with over-temperature and current limit (over-current). The output has an internal clamp circuitry for inductive load. The HS1 and HS2 outputs are controlled by the SPI and have a direct enabled input (PWMIN) for PWM capability.

HIGH SIDE OUTPUT PIN (HS3)

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. The switch is protected with over-temperature and current limit (over-current). The output is controlled only by the SPI.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

WAKE-UP PINS (L1 AND L2)

These pins are high-voltage capable inputs used to sense external switches and to wake-up the device from Sleep or Stop mode. During Normal mode the state of these pins can be read through the SPI.

Important If unused, these pins should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode, this could lead to random wake-up events.

CURRENT SENSE OPERATIONAL AMPLIFIER PINS (E+, E-, OUT, VCC)

These are the pins of the single supply current sense operational amplifier.

- The E+ and E- input pins are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT pin is the output pin of the current sense operational amplifier.
- The VCC pin is the +5.0 V single supply connection.

Note If the operational amplifier is not used, it is possible to connect all pins (E+, E-, OUT and VCC) to GND. In this case, all of the four pins must be grounded.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller. The pin is protected against shorts to GND with an integrated current limit (temperature shutdown could occur).

Important The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR AND CURRENT SENSE AMPLIFIER GROUND PIN (AGND)

The AGND pin is the ground pin of the voltage regulator and the current sense operational amplifier.

Important GND, AGND, VSS, EVSS, VSSA, and VREFL pins must be connected together.

NO CONNECT PINS (NC)

The NC pins are not connected internally.

Note Each of the NC pins can be left open or connected to ground (recommended).

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E624 ANALOG DIE MODES OF OPERATION

The 908E624 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode the device is active and is operating under normal application conditions. The Stop and Sleep modes are low-power modes with wake-up capabilities.

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), and in Sleep mode the voltage regulator is turned off (V_{DD} = 0 V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MODE1:2 bits in the SPI Control register.

Figure 11 describes how transitions are done between the different operating modes and Table 6, page 20, gives an overview of the operating mode.

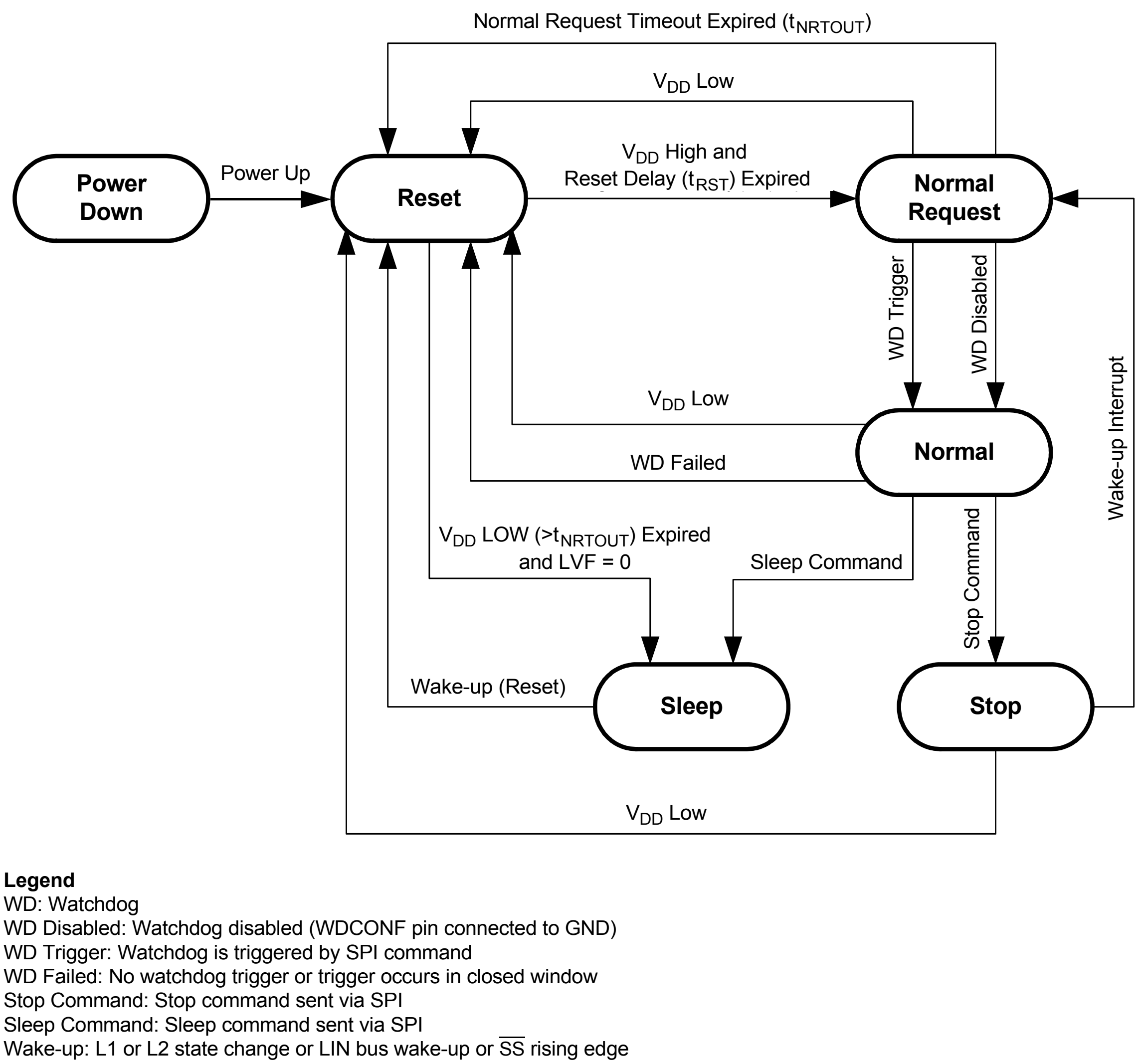


Figure 11. Operating Modes and Transitions

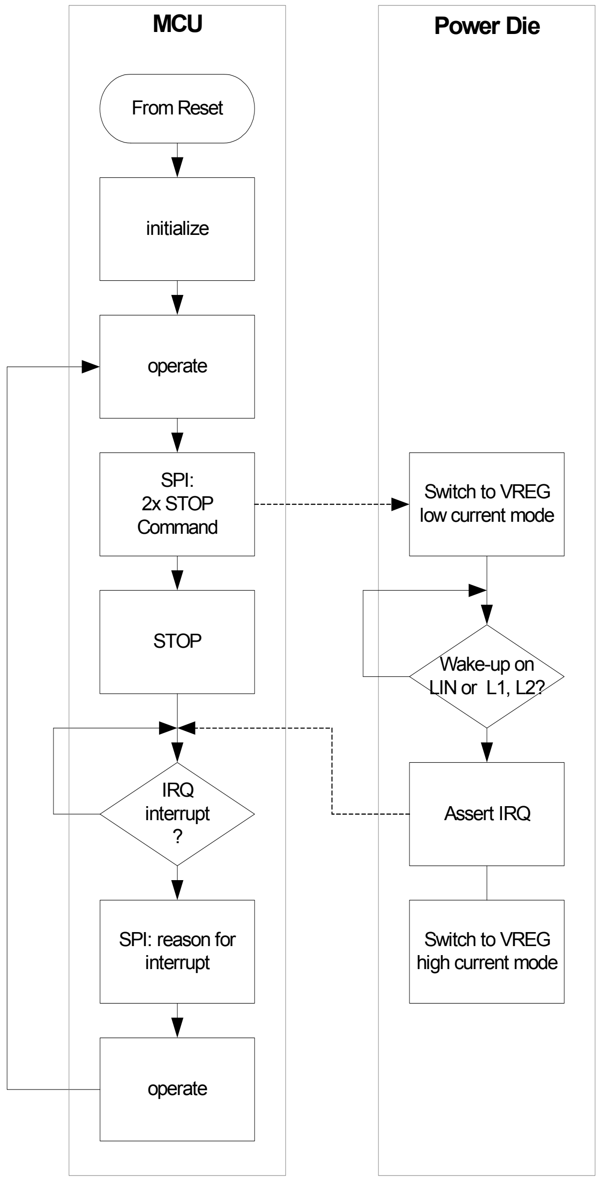


Figure 12. Stop Mode/Wake-up Procedure

ANALOG DIE INPUTS/OUTPUTS

High Side Output Pins HS1 and HS2

These are two high side switches used to drive loads such as relays or lamps. They are protected with over-temperature and current limit (over-current) and include an active internal clamp circuitry for inductive load drive. Control is done using the SPI Control register. PWM capability is offered through the PWMIN input pin.

The high side switch is turned on if both the HSxON bit in the SPI Control register is set and the PWMIN input is HIGH (refer to Figure 13, page 22). In order to have HS1 on, the PWMIN must be HIGH and bit HS1ON must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD pin.

Current Limit (Over-current) Protection

These high side switches feature current limit to protect them against over-current and short circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop modes the high sides are disabled.

High Side Output HS3

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done using the SPI Control register. No direct PWM control is possible on this pin (refer to Figure 14, page 22).

Current Limit (Over-current) Protection

This high side feature switch feature current limit to protect it against over-current and short-circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop mode the high side is disabled.

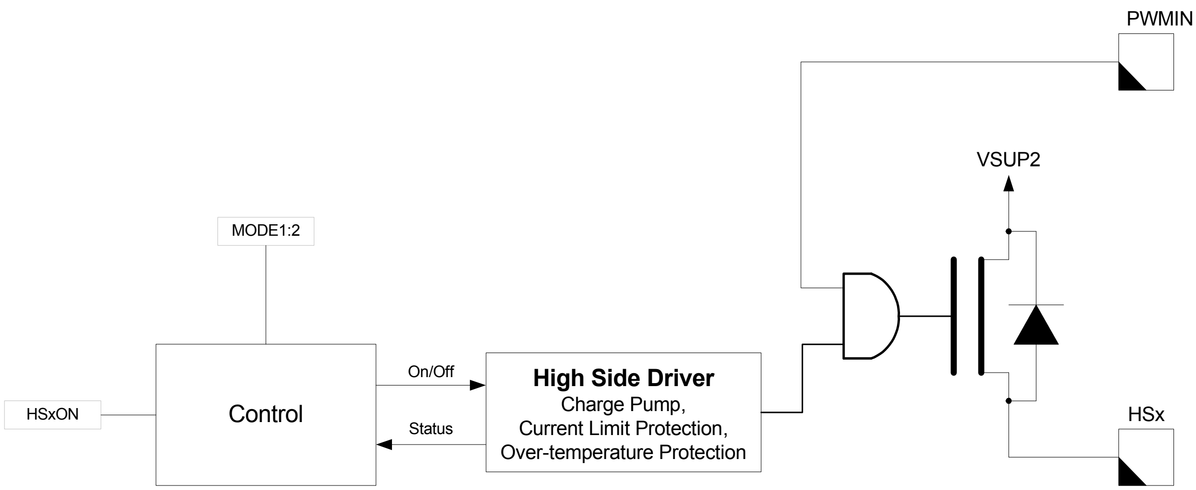


Figure 13. High Side HS1 and HS2 Circuitry

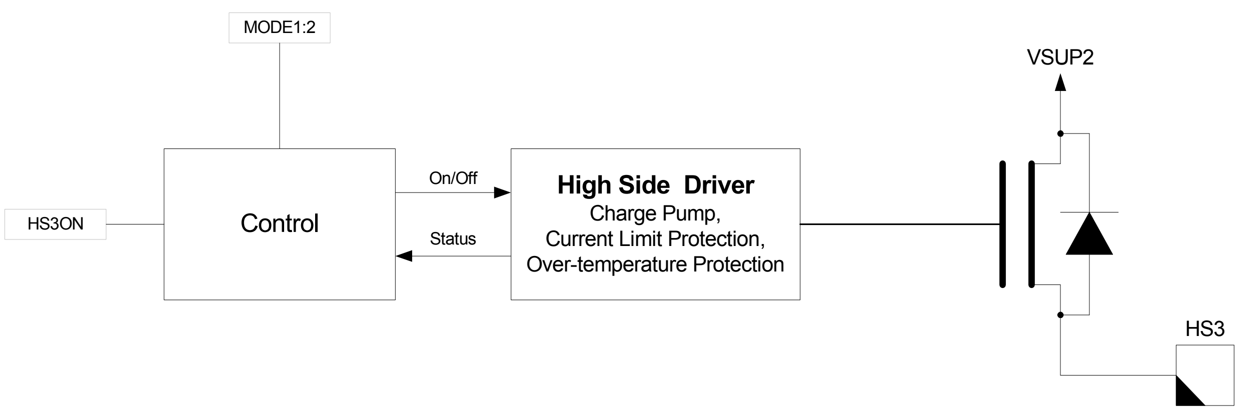


Figure 14. High Side HS3 Circuitry

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with over-current protection and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LINSL2:1 in the SPI Control Register. The initial slew rate is optimized for 20 kBit/s.

disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register. Also see Figure 8, page 15).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF pin. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to Table 8, page 26).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST\_A}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

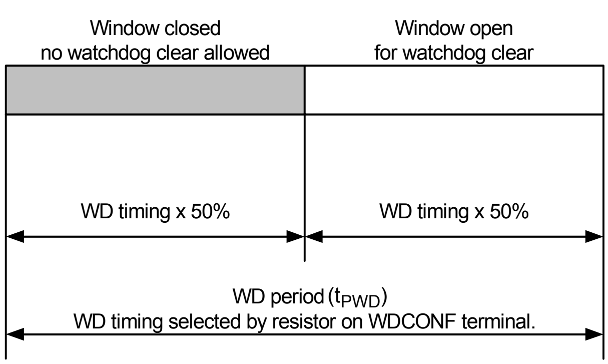


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF pin must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD}\ [\text{ms}] = 0.991 * R_{EXT}\ [\text{k}\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Over-current) Protection

The voltage regulator has current limit to protect the device against over-current and short-circuit conditions.

Over-temperature Protection

The voltage regulator also features an over-temperature protection having an over-temperature warning (Interrupt - VDDT) and an over-temperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease of use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25%, due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at the address $FDC2. After trimming the ICG, a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 µF) V_{DD} = 5.0 V, $T_{Ambient}$~23 °C) and will vary over-temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values must be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

LOGIC COMMANDS AND REGISTERS

908E624 SPI INTERFACE AND CONFIGURATION

The serial peripheral interface creates the communication link between the microcontroller and the analog die of the 908E624.

The interface consists of four pins (see Figure 17):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 8 bits of control information and the slave replies with 8 bits of status data.

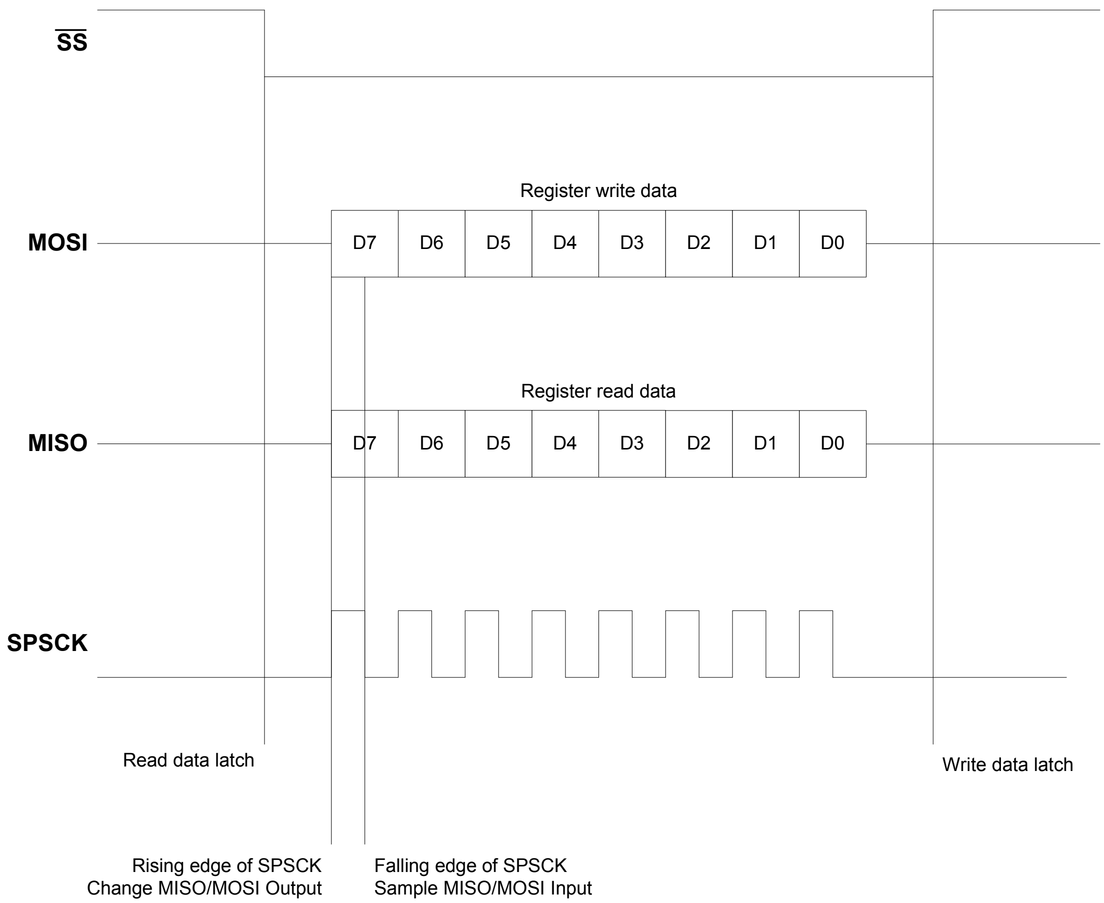


Figure 17. SPI Protocol

During the inactive phase of the $\overline{SS}$ (HIGH), the new data transfer is prepared.

The falling edge of the $\overline{SS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock, SPSCK the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock SPSCK the data is sampled by the Receiver.

The data transfer is only valid if exactly 8 sample clock edges are present in the active (low) phase of $\overline{SS}$.

The rising edge of the slave select $\overline{SS}$ indicates the end of the transfer and latches the write data (MOSI) into the register The $\overline{SS}$ high forces MISO to the high-impedance state.

SPI REGISTER OVERVIEW

Table 7 summarizes the SPI Register bit meaning, reset value, and bit reset condition.

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale website: www.freescale.com.

VSUP Pins (VSUP1 and VSUP2)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN Pin

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) it is recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU Digital Supply Pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU Analog Supply Pins (VREFH, VDDA, VREFL, and VSSA)

To avoid noise on the analog supply pins it is important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 20 and Figure 21 show the recommendations on schematics and layout level and Table 15 indicates recommended external components and layout considerations.

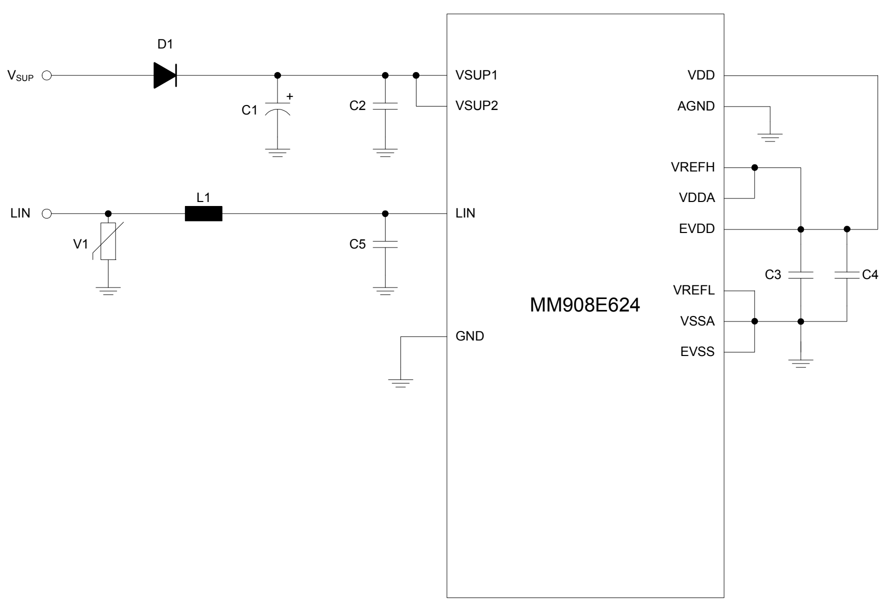
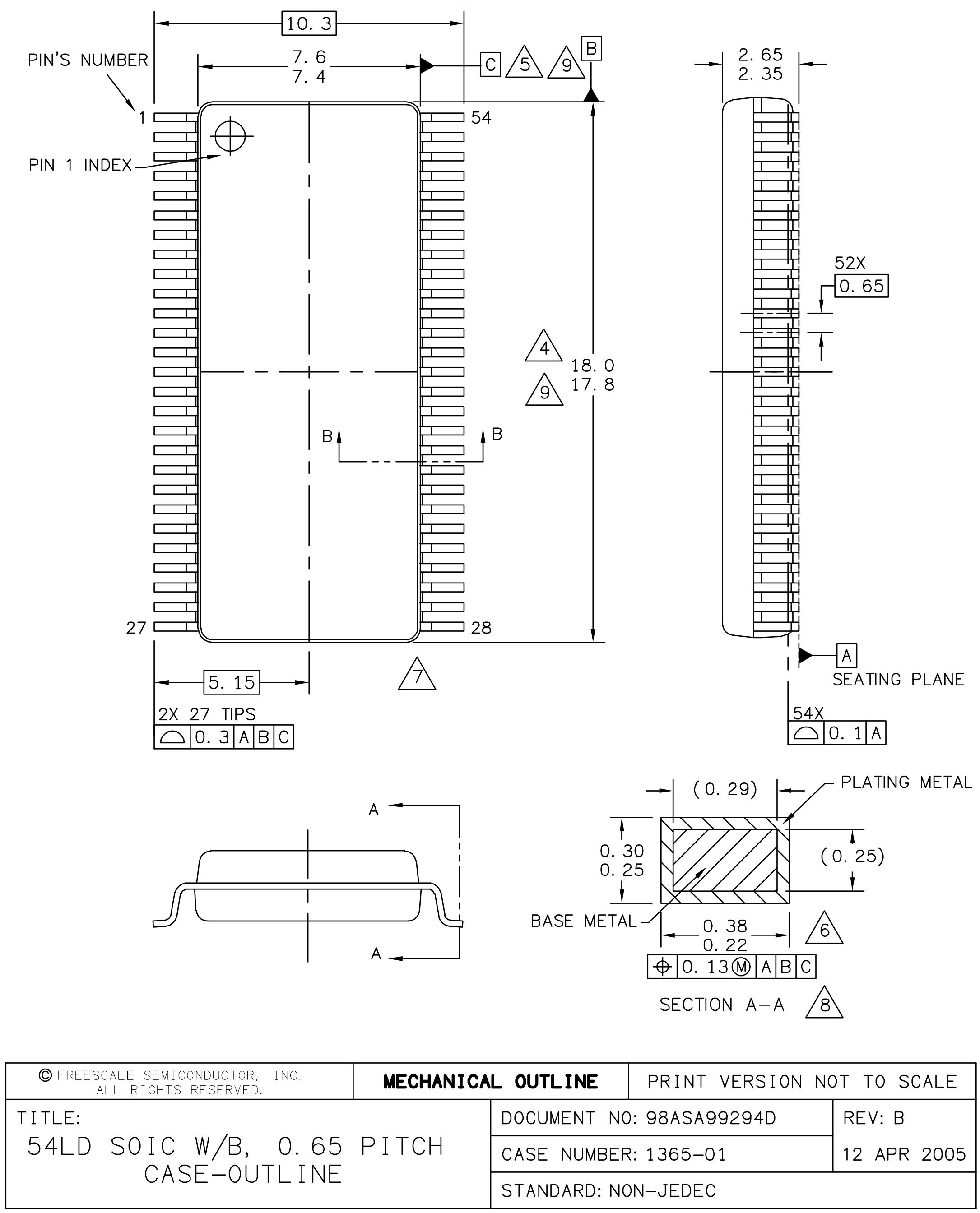


Figure 20. EMC/EMI Recommendations

PACKAGING

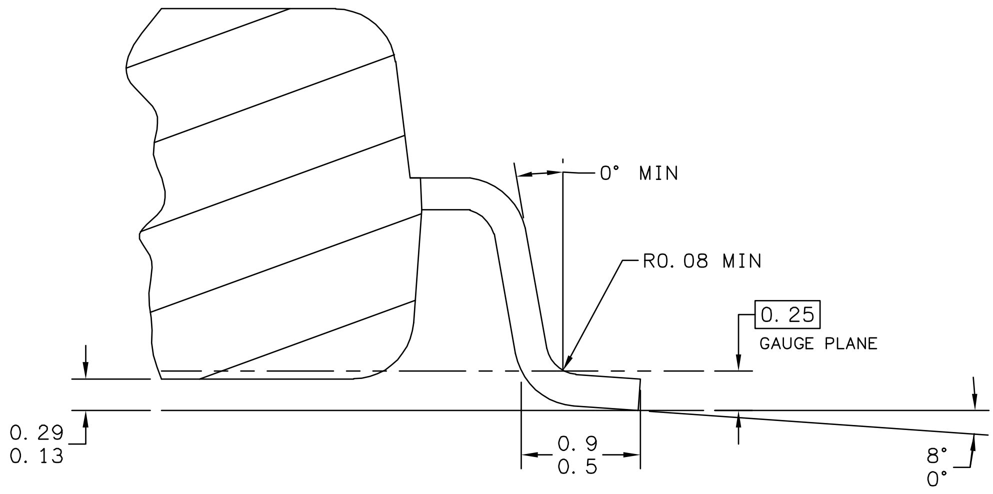
PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ASA99294D drawing number below. Dimensions shown are provided for reference ONLY.



EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

908E624



SECTION B–B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH CASE–OUTLINE	DOCUMENT NO: 98ASA99294D	REV: B
	CASE NUMBER: 1365–01	12 APR 2005
	STANDARD: NON–JEDEC	

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

908E624

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.

9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 54LD SOIC W/B, 0.65 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASA99294D		REV: B
	CASE NUMBER: 1365-01		12 APR 2005
	STANDARD: NON-JEDEC		

EW SUFFIX (Pb-FREE)
54-Pin SOIC WIDE BODY
98ASA99294D
ISSUE B

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	5/2006	• Implemented Revision History page • Added Pb-Free package option (Suffix EW) and higher Soldering temperature • Added “Y” temperature (T_J -40°C to 125°C) code option (MM908E624AYEW) and updated condition statement for Static and Dynamic Electrical Characteristics • Corrected Figure 11, Operating Modes and Transitions (“STOP command” for transition from Normal to Stop state) • Updated Figure 21, PCB Layout Recommendations, comment NC Pin used for signal routing • Updated Table 15, Component Value Recommendation • Corrected Figure 23, Device on Thermal Test Board • Removed reference to Note 11, Voltage Regulator - Dropout Voltage • Added comment “LIN in recessive state” to Supply Current Range in Stop Mode and Sleep Mode • Updated format to match current data sheet standard. • Added Figure 10, Power On Reset and Normal Request Timeout Timing • Added LIN P/L details • Made clarifications on Max Ratings Table for T_A and T_J Thermal Ratings and the accompanying Note
8.0	3/2007	• Removed “Advance Information” watermark from first page.
9.0	9/2010	• Changed Peak Package Reflow Temperature During Reflow(3)(5) description. • Added note (5)
10.0	8/2011	• Deleted MM908E624ACDWB/R2 • Added MM908E624ACPEW/R2 and MM908E624AYPEW/R2 • Update Freescale form and style. • Updated package drawing
11.0	4/2012	• Removed part number MM908E624ACEW/ R2 and MM908E624AYEW/ R2. • Update Freescale form and style.

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Document Number: MM908E624
Rev. 11.0
4/2012