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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	8MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny43u-sur

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Features

- High Performance, Low Power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
 - 123 Powerful Instructions Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- Non-volatile Program and Data Memories
 - 4K Bytes of In-System Programmable Program Memory Flash
 - 64 Bytes of In-System Programmable EEPROM
 - 256 Bytes of Internal SRAM
 - Write/Erase Cycles: 10,000 Flash/ 100,000 EEPROM
 - Data Retention: 20 years at 85°C/ 100 years at 25°C
 - Programming Lock for Software Security
- Peripheral Features
 - QTouch[®] Library Support for Capacitive Touch Sensing (8 Channels)
 - Two 8-bit Timer/Counters with two PWM Channels, Each
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-chip Analog Comparator
 - 10-bit ADC
 - 4 Single-ended Channels
 - Universal Serial Interface
 - Boost Converter
- Special Microcontroller Features
 - debugWIRE On-chip Debug System
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Pin Change Interrupt on 16 Pins
 - Low Power Idle, ADC Noise Reduction and Power-down Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
 - Temperature Sensor On-chip
- I/O and Packages
 - Available in 20-pin SOIC and 20-pin QFN/MLF
 - 16 Programmable I/O Lines
- Operating Voltage:
 - 0.7 1.8V (via On-chip Boost Converter)
 - 1.8 5.5V (Boost Converter Bypassed)
- Speed Grade
 - Using On-chip Boost Converter
 - 0 4 MHz
 - External Power Supply
 - 0 4 MHz @ 1.8 5.5V
 - 0 8 MHz @ 2.7 5.5V
- Low Power Consumption
 - Active Mode, 1 MHz System Clock
 - 400 µA @ 3V (Without Boost Converter)
 - Power-down Mode
 - 150 nA @ 3V (Without Boost Converter)





8-bit **AVR**[®] Microcontroller with 4K Bytes In-System Programmable Flash and Boost Converter

ATtiny43U

Summary

Rev. 8048CS-AVR-02/12



1. Pin Configurations

Figure 1-1. Pinout of ATtiny43U



1.1 Pin Descriptions

1.1.1 V_{cc}

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port A (PA7:PA0)

Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source

² ATtiny43U

capability except PA7 which has the RESET capability. To use pin PA7 as an I/O pin, instead of RESET pin, program ('0') RSTDISBL fuse. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has an alternate functions as analog inputs for the ADC, analog comparator, timer/counter, SPI and pin change interrupt as described in "Alternate Port Functions" on page 69.

1.1.4 **RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 20-4 on page 161. Shorter pulses are not guaranteed to generate a reset.

1.1.5 Port B (PB7:PB0)

Port B is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features as listed in Section 11.3 "Alternate Port Functions" on page 69.

1.1.6 LSW

Boost converter external inductor connection. Connect to ground when boost converter is disabled permanently.

1.1.7 V_{BAT}

Battery supply voltage. Connect to ground when boost converter is disabled permanently.





2. Overview

The ATtiny43U is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny43U achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.



Figure 2-1. Block Diagram

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting

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architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny43U provides the following features: 4K byte of In-System Programmable Flash, 64 bytes EEPROM, 256 bytes SRAM, 16 general purpose I/O lines, 32 general purpose working registers, two 8-bit Timer/Counters with two PWM channels, Internal and External Interrupts, a 4-channel 10-bit ADC, Universal Serial Interface, a programmable Watchdog Timer with internal Oscillator, internal calibrated oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

A special feature of ATtiny43U is the built-in boost voltage converter, which provides 3V supply voltage from an external, low voltage.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny43U AVR is supported by a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.





3. General Information

3.1 Resources

A comprehensive set of development tools, drivers and application notes, and datasheets are available for download on http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

3.3 Capacitive Touch Sensing

Atmel QTouch Library provides a simple to use solution for touch sensitive interfaces on Atmel AVR microcontrollers. The QTouch Library includes support for QTouch[®] and QMatrix[®] acquisition methods.

Touch sensing is easily added to any application by linking the QTouch Library and using the Application Programming Interface (API) of the library to define the touch channels and sensors. The application then calls the API to retrieve channel information and determine the state of the touch sensor.

The QTouch Library is free and can be downloaded from the Atmel website. For more information and details of implementation, refer to the QTouch Library User Guide – also available from the Atmel website.

3.4 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
0x3F (0x5F)	SREG	I	Т	Н	S	V	N	Z	С	Page 9	
0x3E (0x5E)	SPH	-	-	-	-	-	-	-	SP8	Page 12	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Page 12	
0x3C (0x5C)	OCR0B			Timer/	Counter0 – Outp	out Compare Re	gister B			Page 97	
0x3B (0x5B)	GIMSK	-	INT0	PCIE1	PCIE0	-	-	-	-	Page 61	
0x3A (0x5A)	GIFR	-	INTF0	PCIF1	PCIFU	-	-	-	-	Page 61	
0x39 (0x59)	TIMSKU	-	_	_	_	_	OCIEOB	OCIEUA	TOIE0	Page 97	
0x38 (0x58)	SDMCSD	_	_	_	-	PELB	DCF0B BCWPT	DCFUA	SPMEN	Page 98	
0x36 (0x56)	OCR0A		_	 Timer/	Counter0 – Outr	ut Compare Re	aister A	FOLKS	SEMEN	Page 139	
0x35 (0x55)	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	Pages 33, 60, 79	
0x34 (0x54)	MCUSR	-	_	-	-	WDRF	BORF	EXTRF	PORF	Page 55	
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	Page 95	
0x32 (0x52)	TCNT0				Timer/C	Counter0				Page 96	
0x31 (0x51)	OSCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	Page 28	
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-		WGM01	WGM00	Page 92	
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-		WGM11	WGM10	Page 92	
0x2E (0x4E)	TCCR1B	FOC1A	FOC1B	-	-	WGM12	CS12	CS11	CS10	Page 95	
0x2D (0x4D)					Limer/C	Counter1				Page 97	
0x2C (0x4C)	OCR1A			Timer/	Counter1 – Outp	out Compare Reg	gister A			Page 97	
0x26 (0x46)	Reserved			Timer/	Countern – Outp	–	JISTEL P			Page 97	
0x29 (0x49)	Reserved										
0x28 (0x48)	Reserved					_					
0x27 (0x47)	DWDR				DWD	R[7:0]				Page 134	
0x26 (0x46)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	Page 28	
0x25 (0x45)	Reserved				-	_					
0x24 (0x44)	Reserved				-	_					
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	-	PSR10	Page 101	
0x22 (0x42)	Reserved		•	•	-	-			•		
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	Page 55	
0x20 (0x40)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	Page 62	
0x1F (0x3F)	EEAD			EEAD5	EEAD4	EEAD2	EEAP2	EEAD1	EEADO	Page 20	
0x1D (0x3D)	EEDR			LEARS	EEPROMIC	lata Register	LEANZ	LEART	LEARO	Page 21	
0x1C (0x3C)	EECR	_	_	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	Page 21	
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	Page 79	
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	Page 79	
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	Page 79	
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	Page 79	
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	Page 79	
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	Page 79	
0x15 (0x35)	GPIOR2	General Purpose I/O Register 2					Page 22				
0x14 (0x34)	GPIOR1				General Purpos	se I/O Register 1				Page 22	
0x13 (0x33)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINTO	Page 22	
0x11 (0x31)	Reserved	101111	1 01110	1 GINTO		-	1 01112	10111	1 GINTO	1 490 02	
0x10 (0x30)	USIBR				USI Buffe	r Register				Page 113	
0x0F (0x2F)	USIDR				USI Data	Register				Page 112	
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	Page 111	
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	Page 109	
0x0C (0x2C)	TIMSK1	-	-	-	-	-	OCIE1B	OCIE1A	TOIE1	Page 98	
0x0B (0x2B)	TIFR1	-	-	-	-	-	OCF1B	OCF1A	TOV1	Page 98	
0x0A (0x2A)	Reserved					-					
UXU9 (0x29)	Reserved	405	4000	400	A.C.			40104	40100	Dear 115	
	ACSK	ACD	REES	ACO	ACI	ACIE	- MUX2	AUIST MUV1	MUXO	Page 129	
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIE	ADIE	ADPS2	ADPS1	ADPS0	Page 129	
0x05 (0x25)	ADCH				ADC Data Rec	ister High Byte				Page 130	
0x04 (0x24)	ADCL				ADC Data Red	gister Low Byte				Page 130	
0x03 (0x23)	ADCSRB	BS	ACME	-	ADLAR	-	ADTS2	ADTS1	ADTS0	Pages 48, 115, 131	
0x02 (0x22)	Reserved		·	·			·	·	·		
0x01 (0x21)	DIDR0			AIN1D	AIN0D	ADC3D	ADC2D	ADC1D	ADC0D	Pages 116, 132	
0x00 (0x20)	PRR	PRE2	PRE1	PRE0	_	PRTIM1	PRTIM0	PRUSI	PRADC	Page 34	





- Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 - 2. I/O Registers within the address range 0x00 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 - Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

ATtiny43U

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTION	S			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd v Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 - Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (UXFF - K)$	Z,N,V	1
INC	Rd	Increment		Z,N,V	1
DEC	Ra	Decrement		Z,N,V	1
	Ru				1
SER	Ru	Clear Register		Z,IN,V	1
		Set Register		NUTIE	
RIMP	k	Relative lump	$PC \leftarrow PC + k + 1$	None	2
LIMP	ĸ	Indirect lump to (7)	$PC \leftarrow 7$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	1	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC \leftarrow PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC+k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC+k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC \leftarrow PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRMI	K	Branch if Minus	If $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	ĸ	Dranch if Creater or Friel, Circo d	II (IN = U) then PC \leftarrow PC + K + 1	None	1/2
BRGE	ĸ	Dranch il Greater of Equal, Signed	II (IN \oplus V= U) THEN PC \leftarrow PC + K + 1 if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carny Flag Set	if (H = 1) then PC \leftarrow PC + k + 1 if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then PC \leftarrow PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then PC \leftarrow PC $\pm k \pm 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then PC \leftarrow PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then PC \leftarrow PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if $(1 = 0)$ then PC \leftarrow PC + k + 1	None	1/2
BIT AND BIT-TEST	INSTRUCTIONS				
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Bd(0) \leftarrow C Bd(n+1) \leftarrow Bd(n) C \leftarrow Bd(7)$	Z.C.N.V	1





Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=06	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag		N 7	1
SEZ		Set Zero Flag		7	1
SEI		Clobal Interrupt Epoble		2	1
CLI		Global Interrupt Disable		1	1
SES		Set Signed Test Flag	S ← 1	s	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	Т	1
CLT		Clear T in SREG	$T \leftarrow 0$	Т	1
SEH		Set Half Carry Flag in SREG	H ← 1	Н	1
CLH		Clear Half Carry Flag in SREG	H ← 0	Н	1
DATA TRANSFER IN	STRUCTIONS		1		
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD		Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, I+	Load Indirect and Post-Inc.	$Rd \leftarrow (f), f \leftarrow f + f$	None	2
	Rd Y+a	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1$, $Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
SI	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
SID	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	∠, KI 7⊥ Rr	Store Indirect and Post-Inc	$(\mathcal{L}) \leftarrow R I$	None	2
ST	-7 Rr	Store Indirect and Pre-Dec	$7 \leftarrow 7 - 1$ (7) $\leftarrow Rr$	None	2
STD	7+a Rr	Store Indirect with Displacement	$(7+q) \leftarrow \text{Rr}$	None	2
STS	k Rr	Store Direct to SRAM	$(k) \leftarrow Br$	None	2
LPM	ių iu	Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd. Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	(z) ← R1:R0	None	
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INS	TRUCTIONS				
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny43U

Speed	Supply Voltage	Temperature Range	Package ⁽¹⁾	Ordering Code ⁽²⁾
	1.8 - 5.5V ⁽³⁾		20M1	ATtiny43U-MU
8 MHz		Industrial (-40°C to 85°C)		ATtiny43U-MUR
			20S2	ATtiny43U-SU
				ATtiny43U-SUR

Notes: 1. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).

2. Code indicators:

- U, N or F: matte tin

- R: tape & reel

Supply voltage on V_{CC} pin, boost converter disregarded. When boost converter is active the device can be operated from voltages sources lower than indicated here. See table "Characteristics of Boost Converter. T = -20°C to +85°C, unless otherwise noted" on page 162 for more information.

Package Type				
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)			
20S2	20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)			





7. Packaging Information

7.1 20M1



7.2 20S2







8. Errata

The revision letter in this section refers to the revision of the ATtiny43U device.

8.1 ATtiny43U

8.1.1 Rev. D – F

No known errata.

8.1.2 Rev. C

• Increased Probability of Boost Converter Entering Active Low Current Mode

1. Increased Probability Of Boost Converter Entering Active Low Current Mode

The boost converter may enter and stay in Active Low Current Mode at supply voltages and load currents higher than those specified. This is due to high switching currents in bonding wires of the SOIC package. Devices packaged in MLF are not affected.

Problem Fix / Workaround

Add a 1.5nF capacitor between pins LSW and GND of the SOIC package. Also, increase the value of the by-pass capacitor between pins V_{CC} and GND to at least 30µF.

Alternatively, use the device in MLF, without modifications.

8.1.3 Rev. B – A

Not sampled.

9. Datasheet Revision History

9.1 Rev. 8048C - 02/12

- 1. Removed preliminary status of device.
- 2. Updated boost converter descriptions:
 - Last chapter of Section 8.1 "Overview" on page 35
 - Second chapter of Section 8.6.4 "RC Filter" on page 44
 - Boost Converter Component values in Table 8-1 on page 45
 - Last chapter of Section 9.2.3 "Brown-out Detection" on page 51
 - DC Current from Boost Converter Output in Section 20.1 "Absolute Maximum Ratings*" on page 158
 - Section 20.7 "Boost Converter Characteristics" on page 162
 - Section 20.8 "ADC Characteristics" on page 164
 - Section 21.1 "Boost Converter" on page 168
- 3. Updated:
 - Section "Features" on page 1
 - Section 16.8 "Analog Input Circuitry" on page 124
 - Table 16-4 on page 129
 - Section 19.7.1 "Serial Programming Algorithm" on page 154
 - Section 20.2 "DC Characteristics" on page 158
 - Section 21. "Typical Characteristics" on page 168
 - Bit syntax throughout the datasheet, e.g. from CSn2:0 to CSn[2:0]
- 4. Added:
 - Section 3.3 "Capacitive Touch Sensing" on page 6
 - Description on reset in Section 8.5.1 "Stopping the Boost Converter" on page 41
 - Section 8.10 "Firmware Example" on page 46
 - Characteristic plots in Section 21. "Typical Characteristics", starting on page 170
 - Tape & reel in Section 6. "Ordering Information" on page 11

9.2 Rev. 8048B - 05/09

- 1. Updated bullet on data retention in "Features" on page 1.
- 2. Removed section "Typical Applications" on page 46. This data can now be found in application note AVR188.

9.3 Rev. 8048A - 02/09

Initial revision.





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