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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc100ve3dn

6.3.5	Power-down Mode Clock	64
6.3.6	Frequency Divider Output	64
6.4	FLASH MEMORY CONTROLLER (FMC)	66
6.4.1	Overview	66
6.4.2	Features	66
6.5	External Bus Interface (EBI)	67
6.5.1	Overview	67
6.5.2	Features	67
6.6	General Purpose I/O (GPIO)	68
6.6.1	Overview	68
6.6.2	Features	68
6.7	PDMA Controller (PDMA)	69
6.7.1	Overview	69
6.7.2	Features	69
6.8	Timer Controller (TMR)	70
6.8.1	Overview	70
6.8.2	Features	70
6.9	PWM Generator and Capture Timer (PWM)	71
6.9.1	Overview	71
6.9.2	Features	72
6.10	Watchdog Timer (WDT).....	73
6.10.1	Overview	73
6.10.2	Features	73
6.11	Window Watchdog Timer (WWDT)	74
6.11.1	Overview	74
6.11.2	Features	74
6.13	Real Time Clock (RTC)	75
6.13.1	Overview	75
6.13.2	Features	75
6.14	UART Interface Controller (UART).....	76
6.14.1	Overview	76
6.14.2	Features	78
6.15	Smart Card Host Interface (SC)	80
6.15.1	Overview	80
6.15.2	Features	80

- Up to two analog comparators
- External input or internal Band-gap voltage selectable at negative node
- Interrupt when compare results change
- Supports Power-down wake-up
- Smart Card Host (SC)
 - Compliant to ISO-7816-3 T=0, T=1
 - Supports up to three ISO-7816-3 ports
 - Separate receive / transmit 4 bytes entry FIFO for data payloads
 - Programmable transmission clock frequency
 - Programmable receiver buffer trigger level
 - Programmable guard time selection (11 ETU ~ 266 ETU)
 - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
 - Supports auto inverse convention function
 - Supports transmitter and receiver error retry and error limit function
 - Supports hardware activation sequence process
 - Supports hardware warm reset sequence process
 - Supports hardware deactivation sequence process
 - Supports hardware auto deactivation sequence when detecting the card removal
- 96-bit unique ID (UID)
- One built-in temperature sensor with 1°C resolution
- Brown-out Detector
 - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
 - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ 85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin
 - LQFP 64-pin
 - LQFP48-pin

4.2 Pin Configuration

4.2.1 NuMicro® NUC100 Pin Diagram

4.2.1.1 NuMicro® NUC100VxxDN LQFP 100 pin

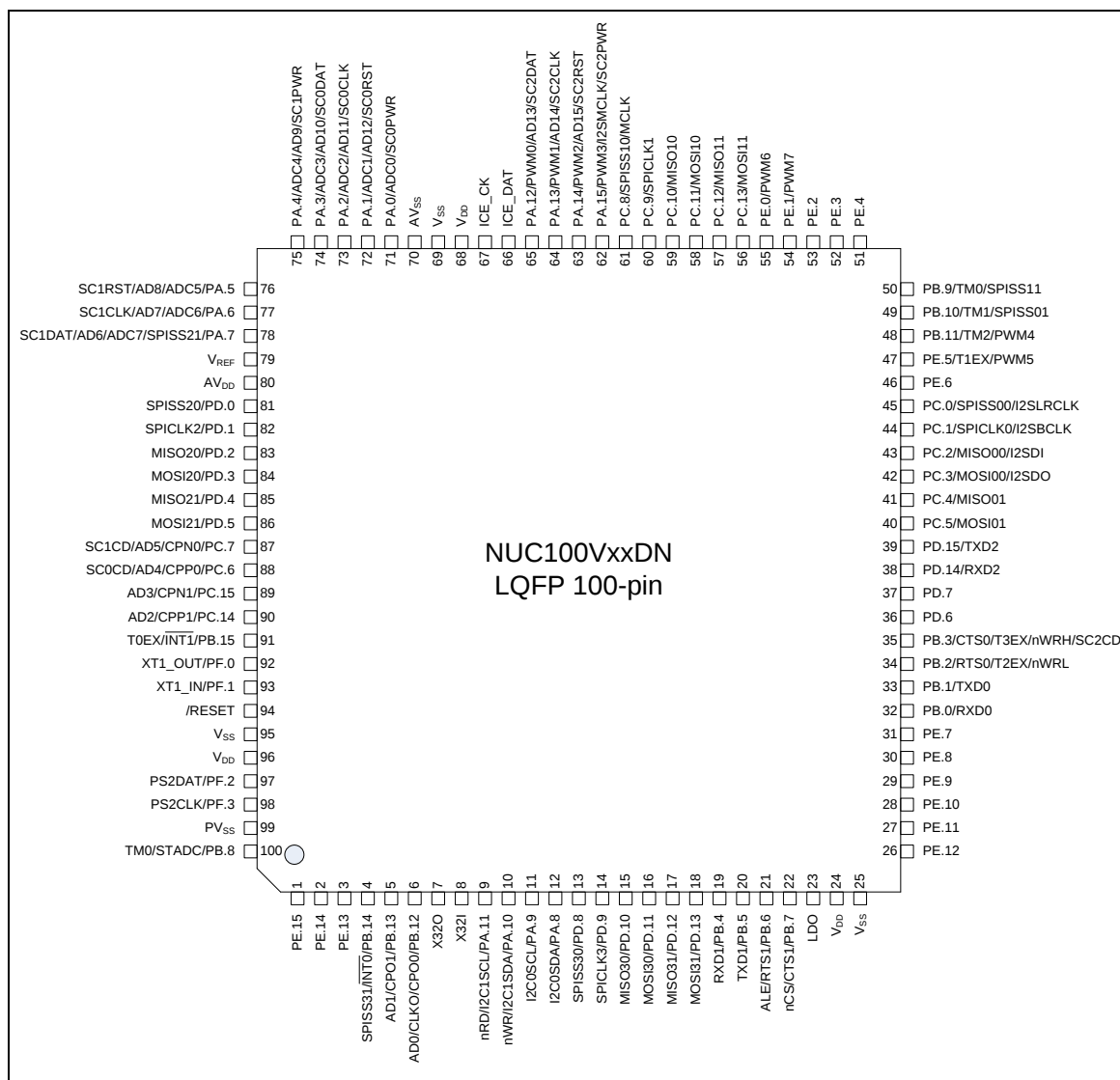


Figure 4-2 NuMicro® NUC100VxxDN LQFP 100-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC100 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			/INT0	I	External interrupt0 input pin.
			SPISS31	I/O	2 nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			CPO1	O	Comparator1 output pin.
			AD1	I/O	EBI Address/Data bus bit1
6	3	1	PB.12	I/O	General purpose digital I/O pin.
			CPO0	O	Comparator0 output pin
			CLKO	O	Frequency Divider output pin
			AD0	I/O	EBI Address/Data bus bit0
7	4	2	X32O	O	External 32.768 kHz low speed crystal output pin
8	5	3	X32I	I	External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1SCL	I/O	I ² C1 clock pin.
			nRD	O	EBI read enable output pin
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1SDA	I/O	I ² C1 data input/output pin.
			nWR	O	EBI write enable output pin
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0SCL	I/O	I ² C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0SDA	I/O	I ² C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPISS30	I/O	1 st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPICLK3	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			MISO30	I/O	1 st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	I/O	General purpose digital I/O pin.
			MOSI30	I/O	1 st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	I/O	General purpose digital I/O pin.
			MISO31	I/O	2 nd SPI3 MISO (Master In, Slave Out) pin.
18			PD.13	I/O	General purpose digital I/O pin.
			MOSI31	I/O	2 nd SPI3 MOSI (Master Out, Slave In) pin.
19	10	8	PB.4	I/O	General purpose digital I/O pin.
			RXD1	I	Data receiver input pin for UART1.
20	11	9	PB.5	I/O	General purpose digital I/O pin.
			TXD1	O	Data transmitter output pin for UART1.
21	12		PB.6	I/O	General purpose digital I/O pin.
			RTS1	O	Request to Send output pin for UART1.
			ALE	O	EBI address latch enable output pin
22	13		PB.7	I/O	General purpose digital I/O pin.
			CTS1	I	Clear to Send input pin for UART1.
			nCS	O	EBI chip select enable output pin
23	14	10	LDO	P	LDO output pin
24	15	11	V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
25	16	12	V _{SS}	P	Ground pin for digital circuit.
26			PE.12	I/O	General purpose digital I/O pin.
27			PE.11	I/O	General purpose digital I/O pin.
28			PE.10	I/O	General purpose digital I/O pin.
29			PE.9	I/O	General purpose digital I/O pin.
30			PE.8	I/O	General purpose digital I/O pin.
31			PE.7	I/O	General purpose digital I/O pin.
32	17	13	PB.0	I/O	General purpose digital I/O pin.
			RXD0	I	Data receiver input pin for UART0.
33	18	14	PB.1	I/O	General purpose digital I/O pin.
			TXD0	O	Data transmitter output pin for UART0.
34	19	15	PB.2	I/O	General purpose digital I/O pin.
			RTS0	O	Request to Send output pin for UART0.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC0DAT	O	SmartCard0 data pin.
			AD10	I/O	EBI Address/Data bus bit10
75	48	36	PA.4	I/O	General purpose digital I/O pin.
			ADC4	AI	ADC4 analog input.
			SC1PWR	O	SmartCard1 power pin.
			AD9	I/O	EBI Address/Data bus bit9
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			SC1RST	O	SmartCard1 reset pin.
			AD8	I/O	EBI Address/Data bus bit8
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			SC1CLK	I/O	SmartCard1 clock pin.
			AD7	I/O	EBI Address/Data bus bit7
78	51	39	PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			SC1DAT	O	SmartCard1 data pin.
			SPISS21	I/O	2 nd SPI2 slave select pin.
			AD6	I/O	EBI Address/Data bus bit6
79			V _{REF}	AP	Voltage reference input for ADC.
80	52	40	AV _{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPISS20	I/O	1 st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPICLK2	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			MISO20	I/O	1 st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			MOSI20	I/O	1 st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			MISO21	I/O	2 nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	I/O	General purpose digital I/O pin.
			MOSI21	I/O	2 nd SPI2 MOSI (Master Out, Slave In) pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
87	53	41	PC.7	I/O	General purpose digital I/O pin.
			CPN0	AI	Comparator0 negative input pin.
			SC1CD	I	SmartCard1 card detect pin.
			AD5	I/O	EBI Address/Data bus bit5
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			CPP0	AI	Comparator0 positive input pin.
			SC0CD	I	SmartCard0 card detect pin.
			AD4	I/O	EBI Address/Data bus bit4
89	55		PC.15	I/O	General purpose digital I/O pin.
			CPN1	AI	Comparator1 negative input pin.
			AD3	I/O	EBI Address/Data bus bit3
90	56		PC.14	I/O	General purpose digital I/O pin.
			CPP1	AI	Comparator1 positive input pin.
			AD2	I/O	EBI Address/Data bus bit2
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			/INT1	I	External interrupt1 input pin.
			T0EX	I	Timer0 external capture input pin.
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	/RESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V _{SS}	P	Ground pin for digital circuit.
96	62		V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2DAT	I/O	PS/2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2CLK	I/O	PS/2 clock pin.
99	63	47	PV _{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			SC2RST	O	SmartCard2 reset pin.
			AD15	I/O	EBI Address/Data bus bit15
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			SC2CLK	O	SmartCard2 clock pin.
			AD14	I/O	EBI Address/Data bus bit14
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			SC2DAT	O	SmartCard2 data pin.
			AD13	I/O	EBI Address/Data bus bit13
66	41	29	ICE_DAT	I/O	Serial Wire Debugger Data pin
67	42	30	ICE_CLK	I	Serial Wire Debugger Clock pin
68			V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V _{SS}	P	Ground pin for digital circuit.
70	43	31	AV _{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.
			ADC1	AI	ADC1 analog input.
			SC0RST	O	SmartCard0 reset pin.
			AD12	I/O	EBI Address/Data bus bit12
73	46	34	PA.2	I/O	General purpose digital I/O pin.
			ADC2	AI	ADC2 analog input.
			SC0CLK	O	SmartCard0 clock pin.
			AD11	I/O	EBI Address/Data bus bit11
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0DAT	O	SmartCard0 data pin.
			AD10	I/O	EBI Address/Data bus bit10

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
 - Four hardware breakpoints
 - Two watchpoints
 - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
 - Single step and vector catch capabilities
- Bus interfaces:
 - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
 - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from RSTSRC register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
 - Power-on Reset (POR)
 - Low level on the nRESET pin
 - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
 - Low Voltage Reset (LVR)
 - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
 - CHIP Reset will reset whole chip by writing 1 to CHIP_RST (IPRSTC1[0])
 - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
 - CPU Reset for Cortex[®]-M0 core Only by writing 1 to CPU_RST (IPRSTC1[1])

Power-on Reset or CHIP_RST (IPRSTC1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

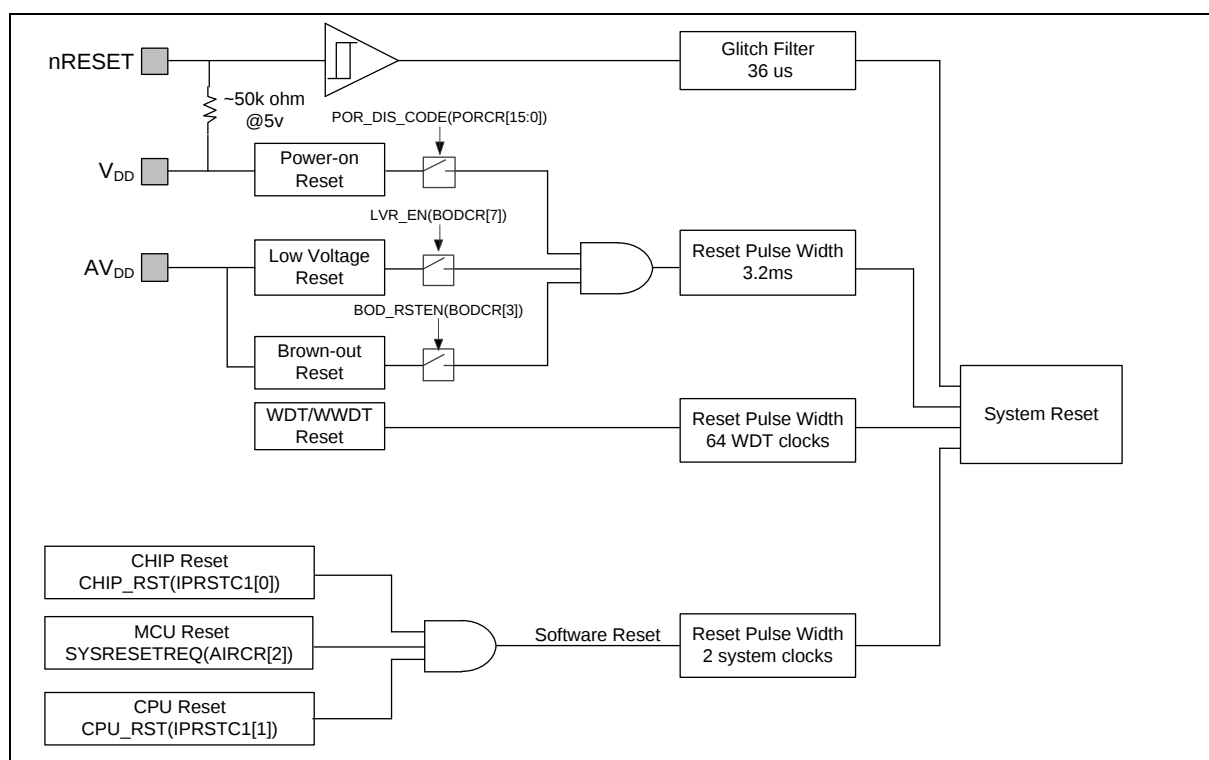


Figure 6-2 System Reset Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
RSTSRC	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIP_RST (IPRSTC1[0])	0x0	-	-	-	-	-	-	-
BOD_EN (BODCR[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BOD_VL (BODCR[2:1])								
BOD_RSTEN (BODCR[3])								
XTL12M_EN (PWRCON[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_EN (APBCLK[0])	0x1	-	0x1	-	-	0x1	-	-
HCLK_S (CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_S	0x3	0x3	-	-	-	-	-	-

6.4 FLASH MEMORY CONTROLLER (FMC)

6.4.1 Overview

The NuMicro® NUC100 series has 128/64/32 Kbytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro® NUC100 series also provides additional DATA Flash for user to store some application dependent data. For 128 Kbytes APROM device, the Data Flash is shared with original 128K program memory and its start address is configurable in Config1. For 64/32 Kbytes APROM device, the Data Flash is fixed at 4K.

6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 128/64/32 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB Data Flash for 64/32 KB APROM device
- Configurable Data Flash size for 128KB APROM device
- Configurable or fixed 4 KB Data Flash with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.14 UART Interface Controller (UART)

The NuMicro® NUC100 series provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART. Besides, only UART0 and UART1 support the flow control function.

6.14.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR, LIN master/slave mode and RS-485 mode functions. Each UART channel supports seven types of interrupts including:

- Transmitter FIFO empty interrupt (INT_THRE)
- Receiver threshold level reached interrupt (INT_RDA),
- Line status interrupt (parity error or frame error or break interrupt) (INT_RLS),
- Receiver buffer time-out interrupt (INT_TOUT),
- MODEM/Wake-up status interrupt (INT_MODEM),
- Buffer error interrupt (INT_BUF_ERR)
- LIN interrupt (INT_LIN)

Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to the Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The UART1~2 are equipped with 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, frame error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is $\text{Baud Rate} = \text{UART_CLK} / M * [\text{BRD} + 2]$, where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 6-6 lists the equations in the various conditions and Table 6-7 lists the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	Don't care	A	$\text{UART_CLK} / [16 * (A+2)]$
1	1	0	B	A	$\text{UART_CLK} / [(B+1) * (A+2)]$, B must ≥ 8
2	1	1	Don't care	A	$\text{UART_CLK} / (A+2)$, A must ≥ 3

Table 6-6 UART Baud Rate Equation

System Clock = Internal 22.1184 MHz High Speed Oscillator						
Baud Rate	Mode 0		Mode 1		Mode 2	
	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016

SIR Protocol encoder/decoder. The IrDA SIR Protocol encoder/decoder is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception, and this delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the UA_FUN_SEL[1:0] to '01'. In LIN mode, 1 start bit and 8 data bits format with 1 stop bit are required in accordance with the LIN standard.

For NuMicro® NUC100 series, another alternate function of UART controllers is RS-485 9-bit mode, and direction control provided by /RTS pin or can program GPIO (PB.2 for UART0_nRTS and PB.6 for UART1_nRTS) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 transceiver control is implemented using the /RTS control signal from an asynchronous serial port to enable the RS-485 transceiver. In RS-485 mode, many characteristics of the receiving and transmitting are same as UART.

6.14.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0 and UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- UART0/UART1 can through DMA channels to receive/transmit data
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
 - Programmable data bit length, 5-, 6-, 7-, 8-bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
 - Supports 3-/16-bit duration for normal mode
- LIN function mode
 - Supports LIN master/slave mode
 - Supports programmable break generation function for transmitter
 - Supports break detect function for receiver
- RS-485 function mode.

6.19 I²S Controller (I²S)

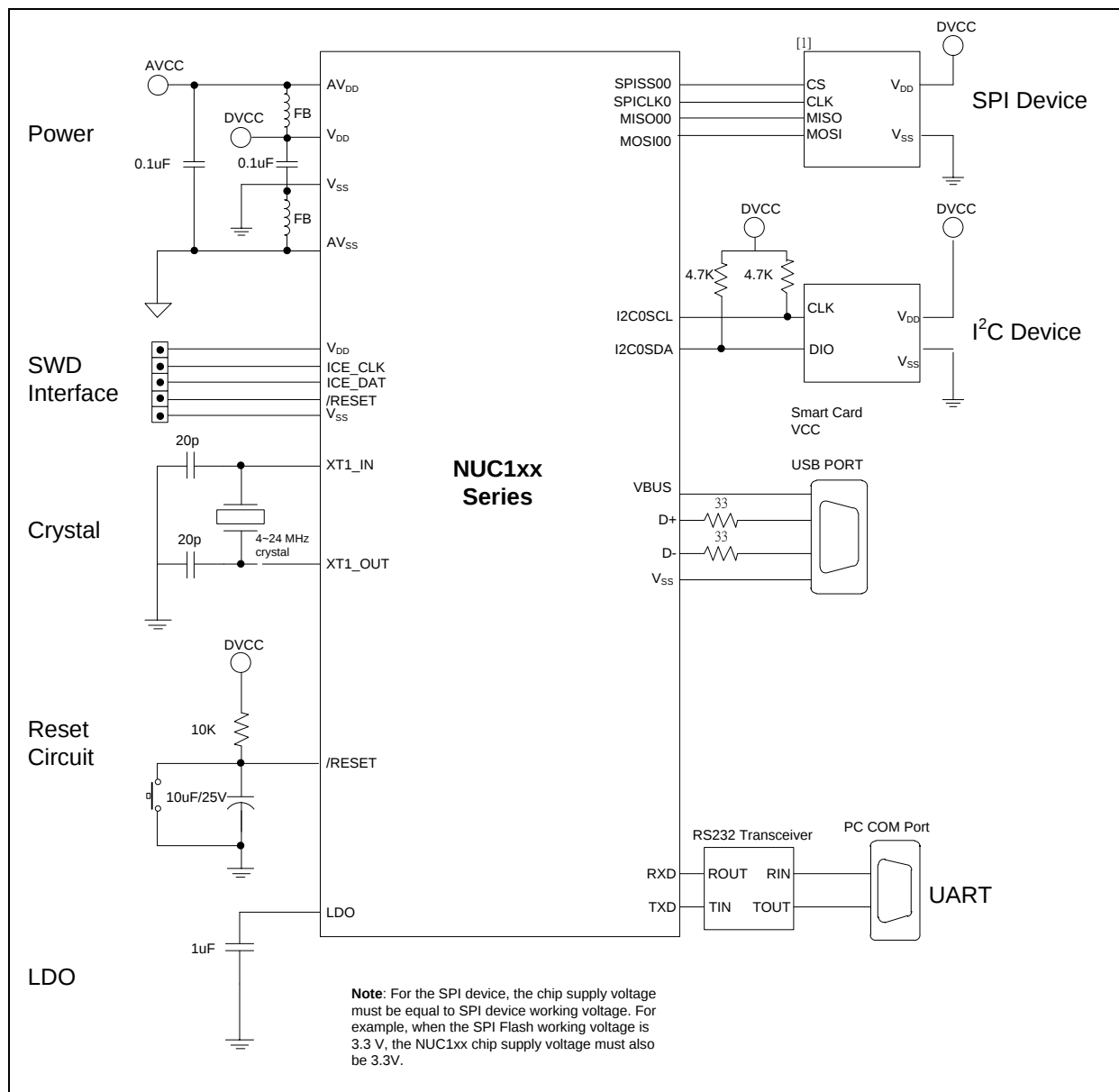
6.19.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 8-word deep FIFO for read path and write path respectively and is capable of handling 8-, 16-, 24- and 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

6.19.2 Features

- Operated as either Master or Slave
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports Mono and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two PDMA requests, one for transmitting and the other for receiving

7 APPLICATION CIRCUIT



8 ELECTRICAL CHARACTERISTICS

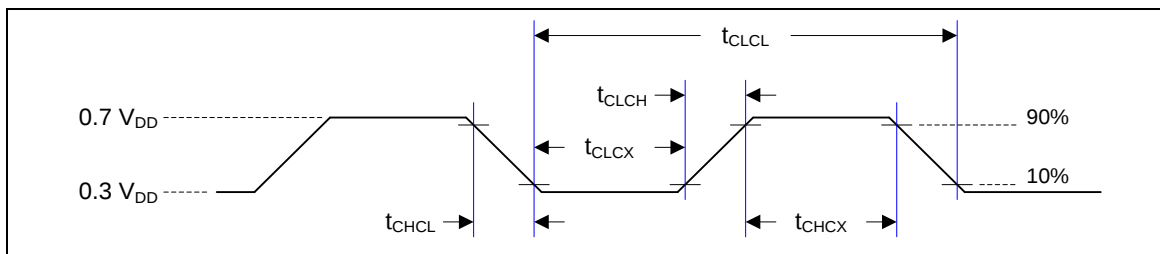
8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	°C
Operating Current	12 MHz at $V_{DD} = 5V$	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High (driven)		2.0			V
V _{IL}	Input Low				0.8	V
V _{DI}	Differential Input Sensitivity	PADP-PADM	0.2			V
V _{CM}	Differential Common-mode Range	Includes V _{DI} range	0.8		2.5	V
V _{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V _{OL}	Output Low (driven)		0		0.3	V
V _{OH}	Output High (driven)		2.8		3.6	V
V _{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R _{PU}	Pull-up Resistor		1.425		1.575	kΩ
V _{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z _{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C _{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T _{FR}	Rise Time	C _L =50p	4		20	ns
T _{FF}	Fall Time	C _L =50p	4		20	ns
T _{FRFF}	Rise and Fall Time Matching	T _{FRFF} =T _{FR} /T _{FF}	90		111.11	%

8.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{VBUS}	VBUS Current (Steady State)	Standby		50		μA

8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V _{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C _{bp}	External Bypass Capacitor			1.0	-	uF