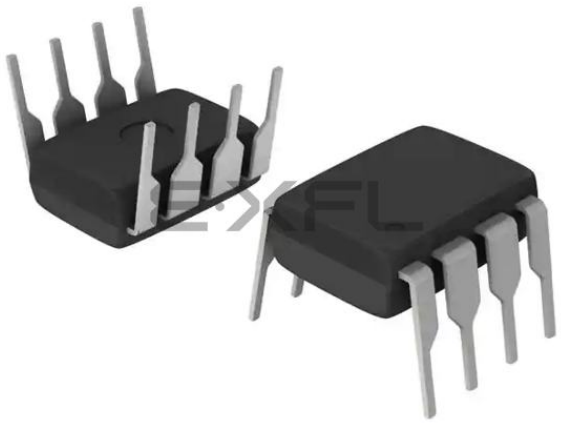


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	4
Program Memory Size	384B (256 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f220-e-p

PIC10F220/222

6-Pin, 8-Bit Flash Microcontrollers

Device Included In This Data Sheet:

- PIC10F220
- PIC10F222

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions Except for Program Branches which are Two-Cycle
- 12-bit Wide Instructions
- 2-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-bit Wide Data Path
- 8 Special Function Hardware Registers
- Operating Speed:
  - 500 ns instruction cycle with 8 MHz internal clock
  - 1 μs instruction cycle with 4 MHz internal clock

Special Microcontroller Features:

- 4 or 8 MHz Precision Internal Oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Short Device Reset Timer, DRT (1.125 ms typical)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{MCLR}$ Input Pin
- Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change

Low-Power Features/CMOS Technology:

- Operating Current:
  - < 175 μA @ 2V, 4 MHz
- Standby Current:
  - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
  - 100,000 Flash endurance
  - > 40-year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Peripheral Features:

- 4 I/O Pins:
  - 3 I/O pins with individual direction control
  - 1 input only pin
  - High current sink/source for direct LED drive
  - Wake-on-change
  - Weak pull-ups
- 8-bit Real-Time Clock/Counter (TMR0) with 8-bit Programmable Prescaler
- Analog-to-Digital (A/D) Converter:
  - 8-bit resolution
  - 2 external input channels
  - 1 internal input channel dedicated

Device	Program Memory	Data Memory	I/O	Timers 8-bit	8-Bit A/D (ch)
	Flash (words)	SRAM (bytes)			
PIC10F220	256	16	4	1	2
PIC10F222	512	23	4	1	2

1.0 GENERAL DESCRIPTION

The PIC10F220/222 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/single-cycle instructions. All instructions are single-cycle (1 μs) except for program branches, which take two cycles. The PIC10F220/222 devices deliver performance in an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC10F220/222 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminates the need for the external Reset circuitry. INTOSC Internal Oscillator mode is provided, thereby, preserving the limited number of I/O available. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC10F220/222 devices are available in cost-effective Flash, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers while benefiting from the Flash programmable flexibility.

The PIC10F220/222 products are supported by a full-featured macro assembler, a software simulator, an in-circuit debugger, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC10F220/222 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers well suited for applications with space limitations. Low-cost, low-power, high-performance, ease-of-use and I/O flexibility make the PIC10F220/222 devices very versatile, even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC10F220/222 DEVICES(1), (2)

		PIC10F220	PIC10F222
Clock	Maximum Frequency of Operation (MHz)	8	8
Memory	Flash Program Memory	256	512
	Data Memory (bytes)	16	23
Peripherals	Timer Module(s)	TMR0	TMR0
	Wake-up from Sleep on pin change	Yes	Yes
	Analog inputs	2	2
Features	I/O Pins	3	3
	Input Only Pins	1	1
	Internal Pull-ups	Yes	Yes
	In-Circuit Serial Programming™	Yes	Yes
	Number of instructions	33	33
	Packages	6-pin SOT-23, 8-pin DIP, DFN	6-pin SOT-23, 8-pin DIP, DFN

Note 1: The PIC10F220/222 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.

2: The PIC10F220/222 devices use serial programming with data pin GP0 and clock pin GP1.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC10F220/222 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC10F220/222 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1 μs @ 4 MHz or 500 ns @ 8 MHz) except for program branches.

The table below lists program memory (Flash) and data memory (RAM) for the PIC10F220/222 devices.

Device	Memory	
	Program	Data
PIC10F220	256 x 12	16 x 8
PIC10F222	512 x 12	23 x 8

The PIC10F220/222 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC10F220/222 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC10F220/222 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC10F220/222 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1 with the corresponding device pins described in Table 3-1.

FIGURE 3-1: BLOCK DIAGRAM

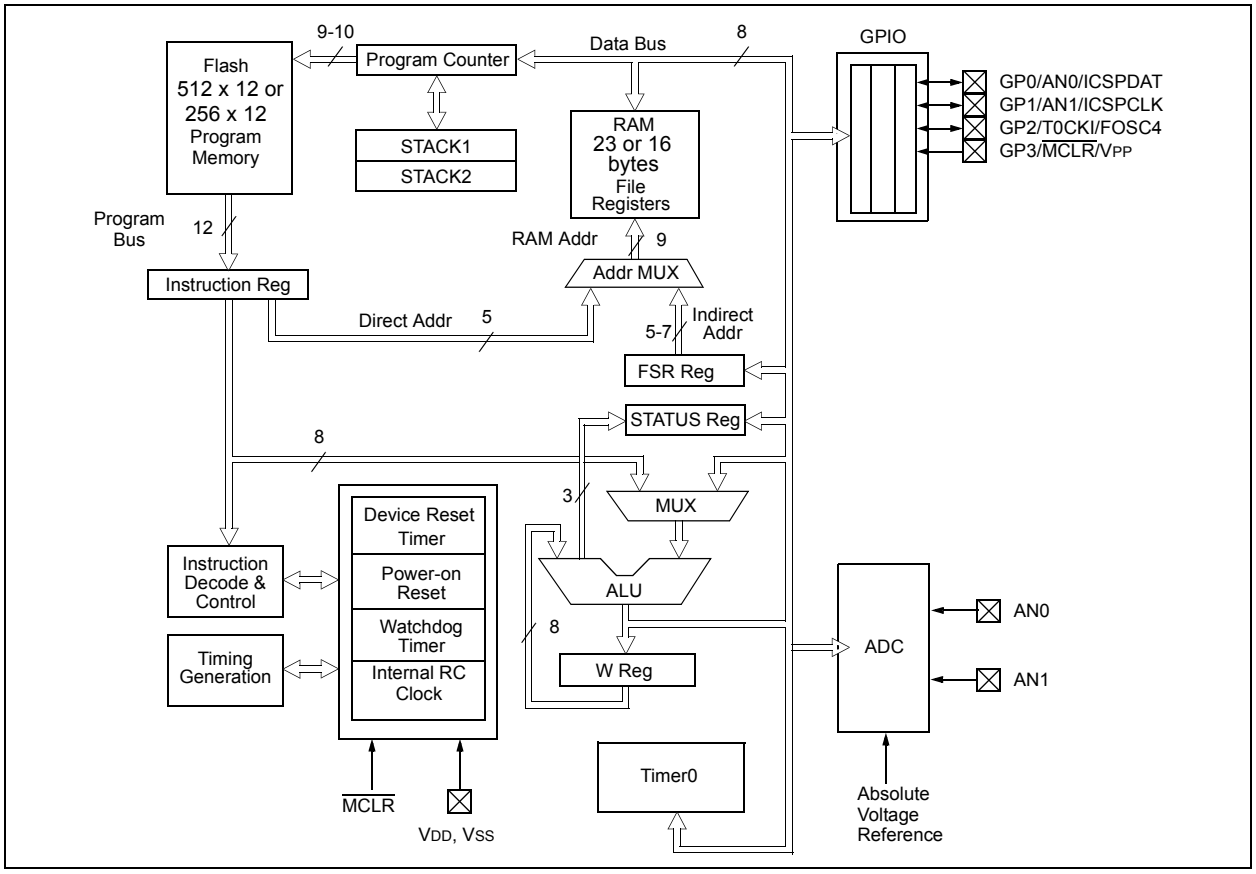


TABLE 3-1: PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/AN0/ICSPDAT	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN0	AN	—	Analog Input
	ICSPDAT	ST	CMOS	In-Circuit programming data
GP1/AN1/ICSPCLK	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN1	AN	—	Analog Input
	ICSPCLK	ST	—	In-Circuit programming clock
GP2/T0CKI/FOSC4	GP2	TTL	CMOS	Bidirectional I/O pin
	T0CKI	ST	—	Clock input to TMR0
	FOSC4	—	CMOS	Oscillator/4 output
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/VPP must not exceed VDD during normal device operation or the device will enter Programming mode.
	VPP	HV	—	Programming voltage input
VDD	VDD	P	—	Positive supply for logic and I/O pins
VSS	VSS	P	—	Ground reference for logic and I/O pins

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Input

4.0 MEMORY ORGANIZATION

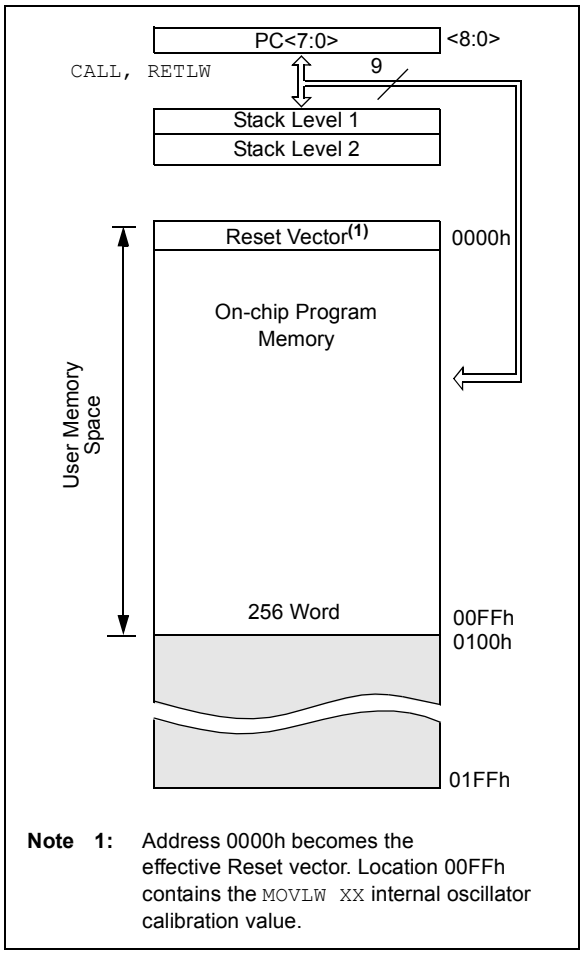
The PIC10F220/222 memories are organized into program memory and data memory. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization for the PIC10F220

The PIC10F220 devices have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space.

Only the first 256 x 12 (0000h-00FFh) for the PIC10F220 are physically implemented (see Figure 4-1). Accessing a location above these boundaries will cause a wrap-around within the first 256 x 12 space (PIC10F220). The effective Reset vector is at 0000h, (see Figure 4-1). Location 00FFh (PIC10F220) contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC10F220



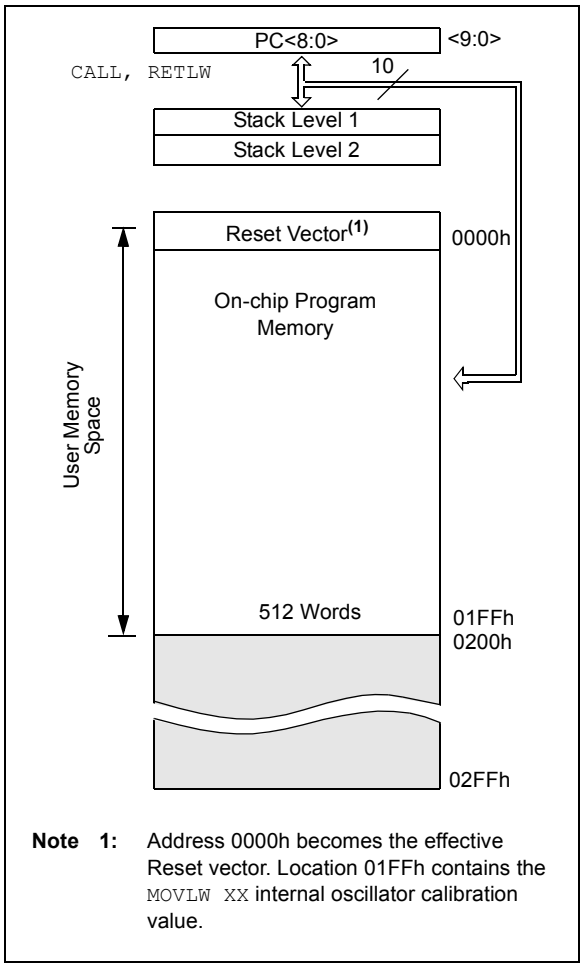
Note 1: Address 0000h becomes the effective Reset vector. Location 00FFh contains the `MOVLW XX` internal oscillator calibration value.

4.2 Program Memory Organization for the PIC10F222

The PIC10F222 devices have a 10-bit Program Counter (PC) capable of addressing a 1024 x 12 program memory space.

Only the first 512 x 12 (0000h-01FFh) for the Mem-High are physically implemented (see Figure 4-2). Accessing a location above these boundaries will cause a wrap-around within the first 512 x 12 space (PIC10F222). The effective Reset vector is at 0000h, (see Figure 4-2). Location 01FFh (PIC10F222) contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC10F222



Note 1: Address 0000h becomes the effective Reset vector. Location 01FFh contains the `MOVLW XX` internal oscillator calibration value.

REGISTER 4-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GPWUF:** GPIO Reset bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **Reserved:** Do not use. Use of this bit may affect upward compatibility with future products.

bit 5 **Reserved:** Do not use. Use of this bit may affect upward compatibility with future products.

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{borrow}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry to the 4th low-order bit of the result occurred
0 = A carry to the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C:** Carry/$\overline{borrow}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

ADDWF:	SUBWF:	RRF or RLF:
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

4.7 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

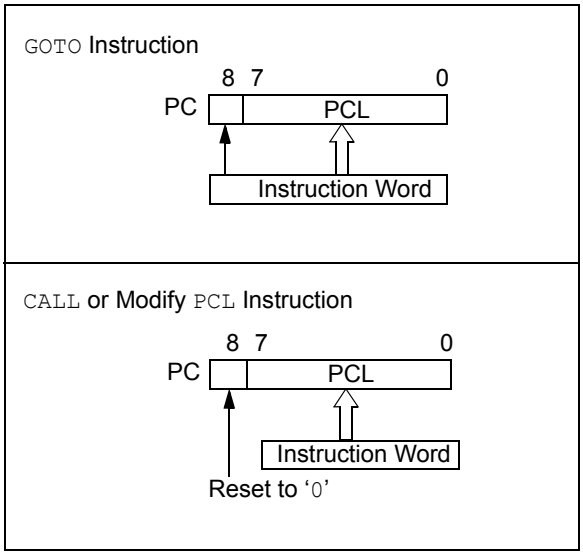
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>.

For a CALL instruction or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-5).

Instructions where the PCL is the destination or Modify PCL instructions, include MOVWF PC, ADDWF PC and BSF PC, 5.

Note:	Because PC<8> is cleared in the CALL instruction or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-5: LOADING OF PC BRANCH INSTRUCTIONS



4.7.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in program memory (i.e., the oscillator calibration instruction). After executing MOVLW XX, the PC will roll over to location 0000h and begin executing user code.

4.8 Stack

The PIC10F220 device has a 2-deep, 8-bit wide hardware PUSH/POP stack.

The PIC10F222 device has a 2-deep, 9-bit wide hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of stack 1 into stack 2 and then PUSH the current PC value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of stack level 1 into the PC and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2.

Note 1:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.
2:	There are no Status bits to indicate stack overflows or stack underflow conditions.
3:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

5.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF GPIO, W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

5.1 GPIO

GPIO is an 8-bit I/O register. Only the low-order 4 bits are used (GP<3:0>). Bits 7 through 4 are unimplemented and read as '0's. Please note that GP3 is an input only pin. Pins GP0, GP1 and GP3 can be configured with weak pull-ups and also for wake-up on change. The wake-up on change and weak pull-up functions are not individually pin selectable. If GP3/$\overline{\text{MCLR}}$ is configured as $\overline{\text{MCLR}}$, a weak pull-up can be enabled via the Configuration Word. Configuring GP3 as $\overline{\text{MCLR}}$ disables the wake-up on change function for this pin.

5.2 TRIS Registers

The Output Driver Control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a High-Impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3, which is input only, and the GP2/T0CKI/FOSC4 pin, which may be controlled by various registers. See Table 5-1.

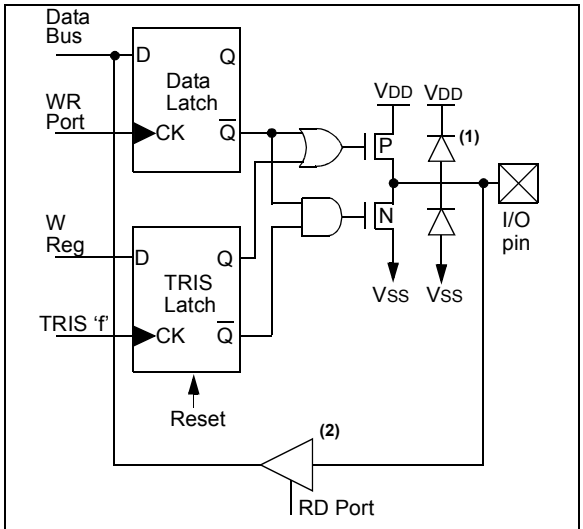
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon Reset.

5.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except GP3, which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to V_{DD} and V_{SS}.

2: See Table 3-1 for buffer type.

TABLE 5-1: ORDER OF PRECEDENCE FOR PIN FUNCTIONS

Priority	GP0	GP1	GP2	GP3
1	AN0	AN1	FOSC4	$\overline{\text{MCLR}}$
2	TRIS GPIO	TRIS GPIO	T0CKI	—
3	—	—	TRIS GPIO	—

TABLE 5-2: REQUIREMENTS TO MAKE PINS AVAILABLE IN DIGITAL MODE

Bit	GP0	GP1	GP2	GP3
FOSC4	—	—	0	—
T0CS	—	—	0	—
ANS1	—	0	—	—
ANS0	0	—	—	—
MCLRE	—	—	—	0

Legend: — = Condition of bit will have no effect on the setting of the pin to Digital mode.

7.7 Analog Conversion Result Register

The ADRES register contains the results of the last conversion. These results are present during the sampling period of the next analog conversion process. After the sampling period is over, ADRES is cleared (= 0). A 'leading one' is then right shifted into the ADRES to serve as an internal conversion complete bit. As each bit weight, starting with the MSb, is converted, the leading one is shifted right and the converted bit is stuffed into ADRES. After a total of 9 right shifts of the 'leading one' have taken place, the conversion is complete; the 'leading one' has been shifted out and the GO/$\overline{\text{DONE}}$ bit is cleared.

If the GO/$\overline{\text{DONE}}$ bit is cleared in software during a conversion, the conversion stops. The data in ADRES is the partial conversion result. This data is valid for the bit weights that have been converted. The position of the 'leading one' determines the number of bits that have been converted. The bits that were not converted before the GO/$\overline{\text{DONE}}$ was cleared are unrecoverable.

7.8 Internal Absolute Voltage Reference

The function of the Internal Absolute Voltage Reference is to provide a constant voltage for conversion across the devices V_{DD} supply range. The A/D Converter is ratiometric with the conversion reference voltage being V_{DD}. Converting a constant voltage of 0.6V (typical) will result in a result based on the voltage applied to V_{DD} of the device. The result of conversion of this reference across the V_{DD} range can be approximated by: Conversion Result = 0.6V/(V_{DD}/256)

Note:	The actual value of the Absolute Voltage Reference varies with temperature and part-to-part variation. The conversion is also susceptible to analog noise on the V_{DD} pin and noise generated by the sinking or sourcing of current on the I/O pins.

REGISTER 7-1: ADCON0: A/D CONVERTER 0 REGISTER

R/W-1	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-0
ANS1	ANS0	—	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ANS1:** ADC Analog Input Pin Select bit
1 = GP1/AN1 configured for analog input
0 = GP1/AN1 configured as digital I/O

bit 6 **ANS0:** ADC Analog Input Pin Select bit(1), (2)
1 = GP0/AN0 configured as an analog input
0 = GP0/AN0 configured as digital I/O

bit 5-4 **Unimplemented:** Read as '0'

bit 3-2 **CHS<1:0>:** ADC Channel Select bits(3)
00 = Channel 00 (GP0/AN0)
01 = Channel 01 (GP1/AN1)
1X = 0.6V absolute Voltage reference

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit(4)
1 = ADC conversion in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC is done converting.
0 = ADC conversion completed/not in progress. Manually clearing this bit while a conversion is in process terminates the current conversion.

bit 0 **ADON:** ADC Enable bit
1 = ADC module is operating
0 = ADC module is shut-off and consumes no power

Note 1: When the ANS bits are set, the channel(s) selected are automatically forced into analog mode regardless of the pin function previously defined.
2: The ANS<1:0> bits are active regardless of the condition of ADON
3: CHS<1:0> bits default to 11 after any Reset.
4: If the ADON bit is clear, the GO/$\overline{\text{DONE}}$ bit cannot be set.

REGISTER 7-2: ADRES: ANALOG CONVERSION RESULT REGISTER

R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**

8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC10F220/222 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Reset:
  - Power-on Reset (POR)
  - Device Reset Timer (DRT)
  - Watchdog Timer (WDT)
  - Wake-up from Sleep on pin change
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™
- Clock Out

The PIC10F220/222 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. When using DRT, there is an 1.125 ms (typical) delay only on VDD power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low current Power-Down mode. The user can wake-up from Sleep through a change on input pins or through a Watchdog Timer time-out.

8.1 Configuration Bits

The PIC10F220/222 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. One bit is the Watchdog Timer enable bit, one bit is the $\overline{\text{MCLR}}$ enable bit and one bit is for code protection (see Register 8-1).

REGISTER 8-1: CONFIG: CONFIGURATION WORD(1)

—	—	—	—	—	—	—	MCLRE	$\overline{\text{CP}}$	WDTE	$\overline{\text{MCPU}}$	IOSCFS
bit 11											bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 11-5 **Unimplemented:** Read as '0'

bit 4 **MCLRE:** GP3/$\overline{\text{MCLR}}$ Pin Function Select bit
1 = GP3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = GP3/$\overline{\text{MCLR}}$ pin function is digital I/O, $\overline{\text{MCLR}}$ internally tied to VDD

bit 3 **$\overline{\text{CP}}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1 **$\overline{\text{MCPU}}$:** Master Clear Pull-up Enable bit(2)
1 = Pull-up disabled
0 = Pull-up enabled

bit 0 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz
0 = 4 MHz

Note 1: Refer to the "*PIC10F220/222 Memory Programming Specification*" (DS41266), to determine how to access the Configuration Word. The Configuration Word is not user addressable during device operation.
2: MCLRE must be a '1' to enable this selection.

9.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 9-1, while the various opcode fields are summarized in Table 9-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 9-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top-of-Stack
PC	Program Counter
WDT	Watchdog Timer counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

'0xhhh'

where 'h' signifies a hexadecimal digit.

FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS

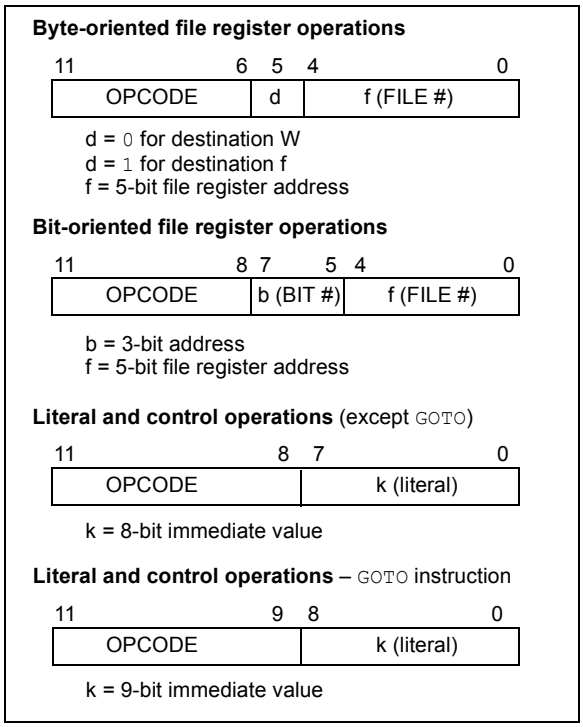


FIGURE 11-2: IDD vs. VDD OVER FOSC (8 MHz)

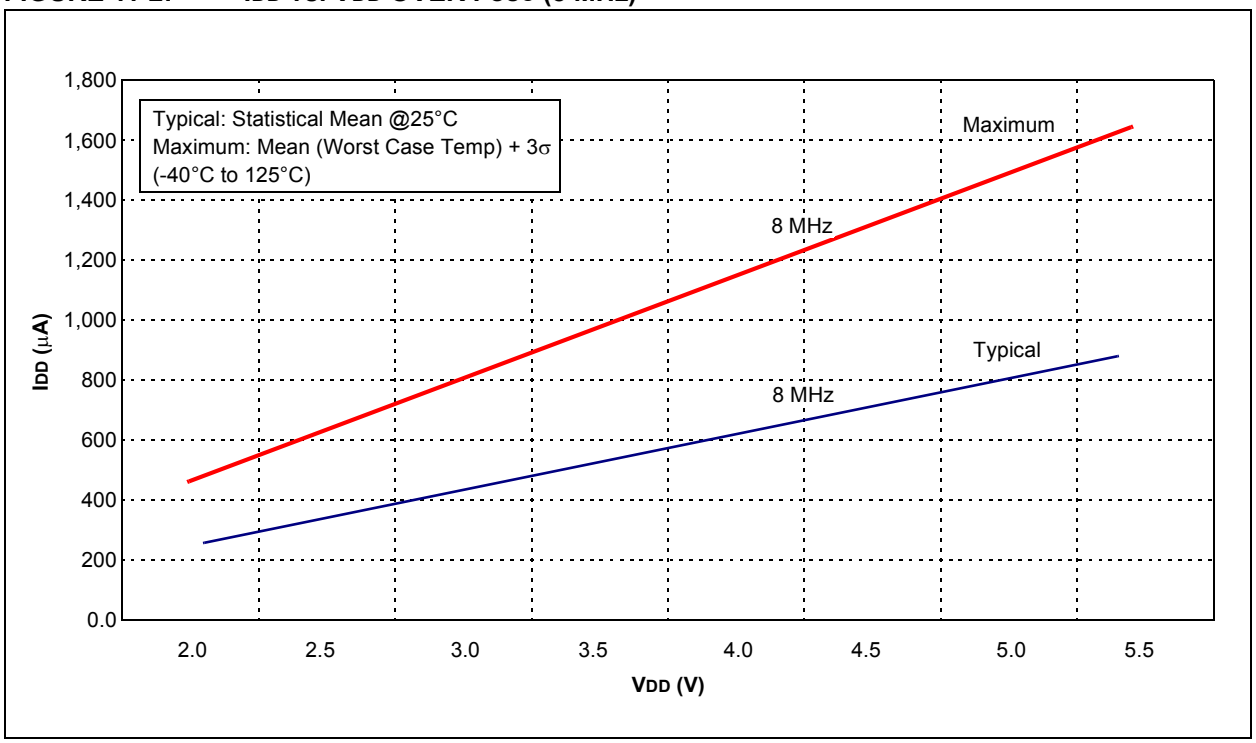


FIGURE 11-3: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

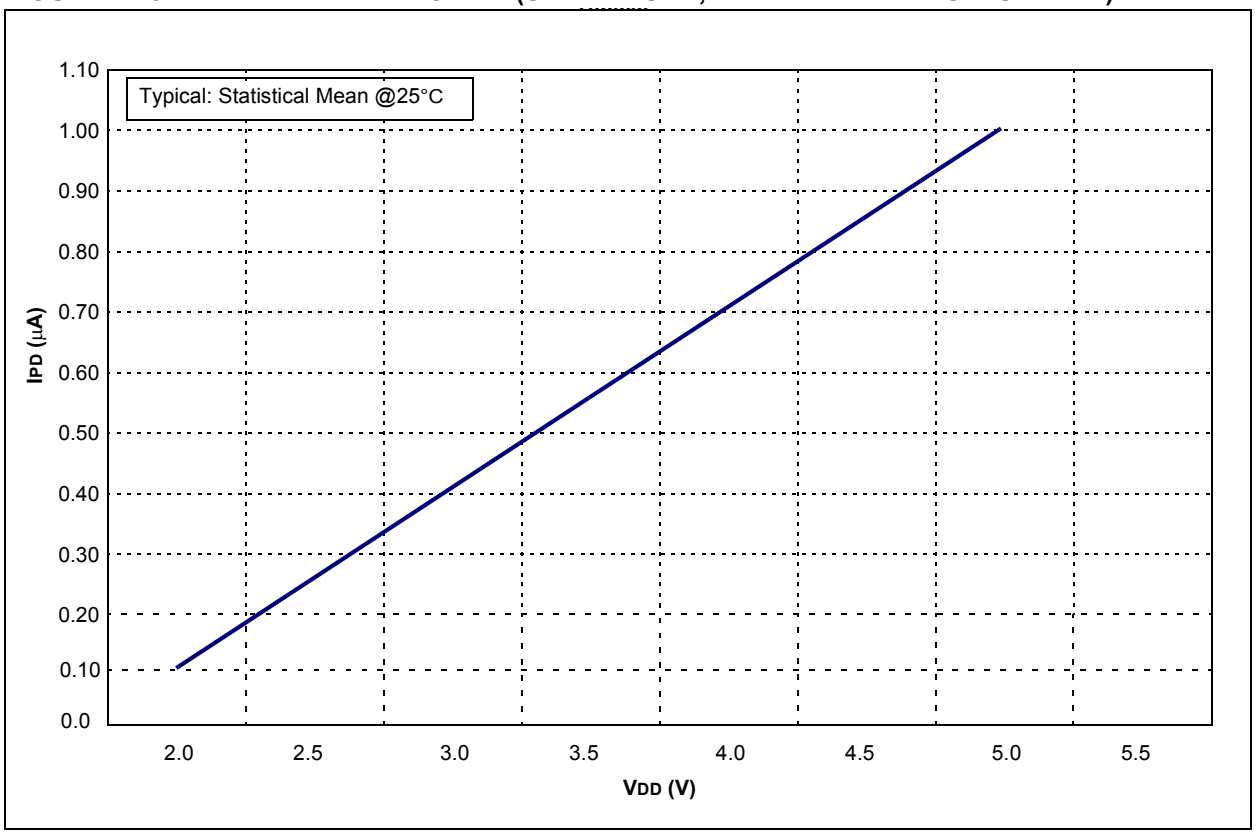


FIGURE 11-6: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

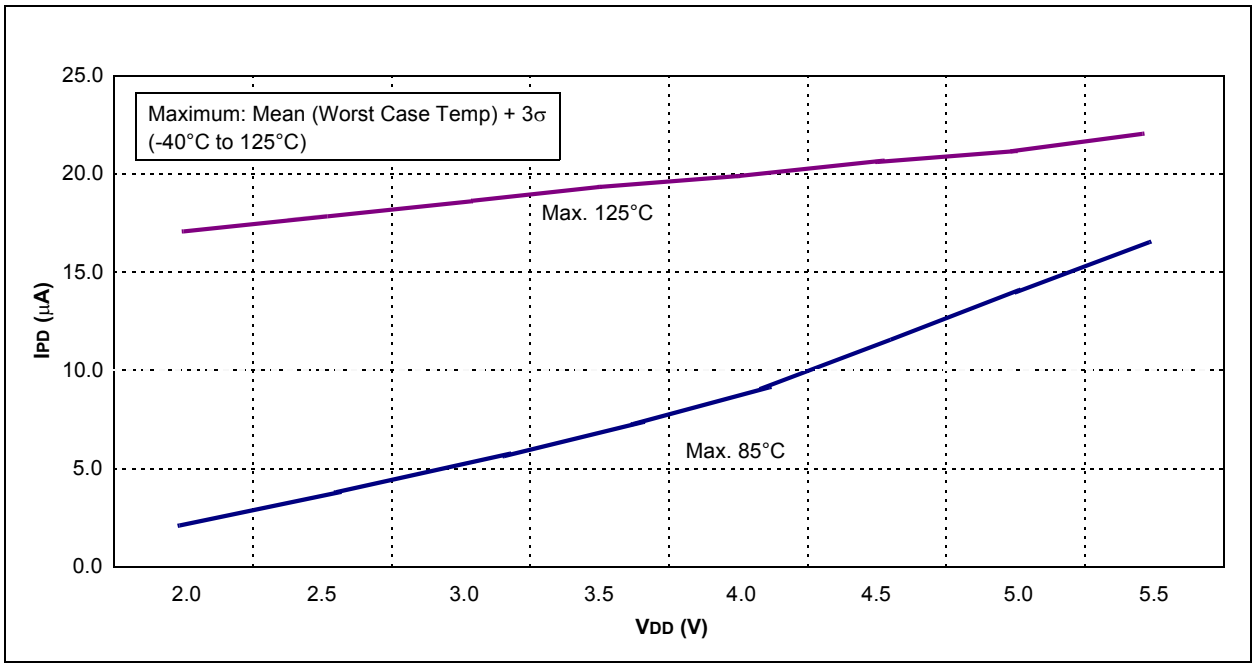


FIGURE 11-7: WDT TIME-OUT vs. VDD OVER TEMPERATURE (NO PRESCALER)

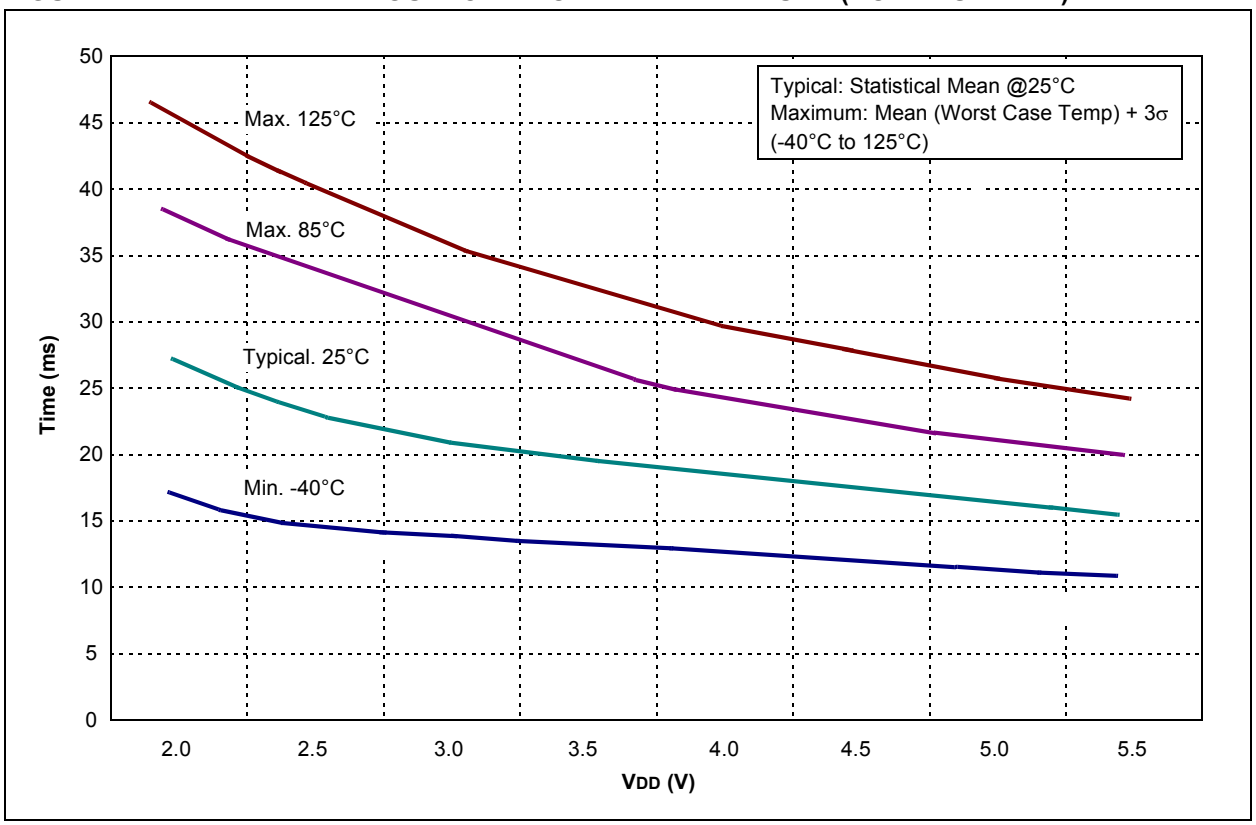


FIGURE 11-10: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

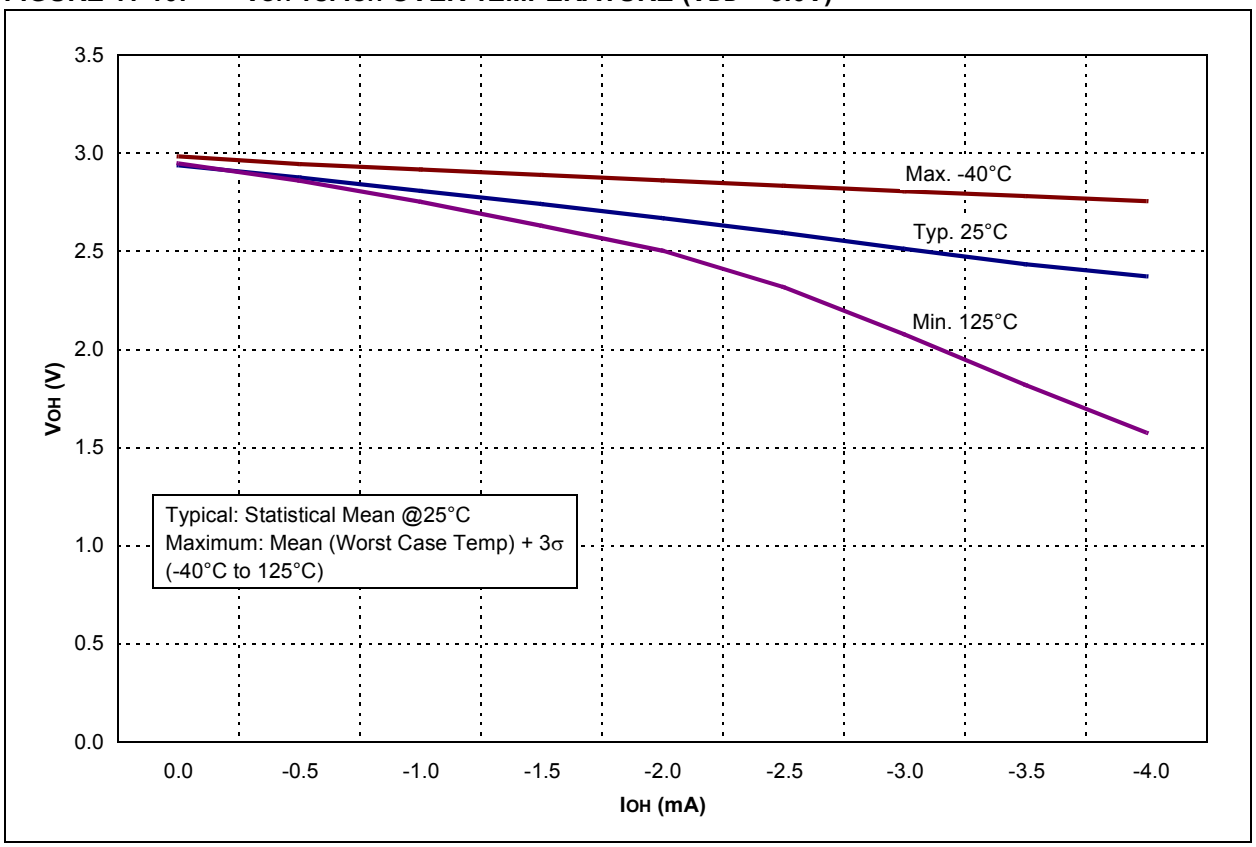
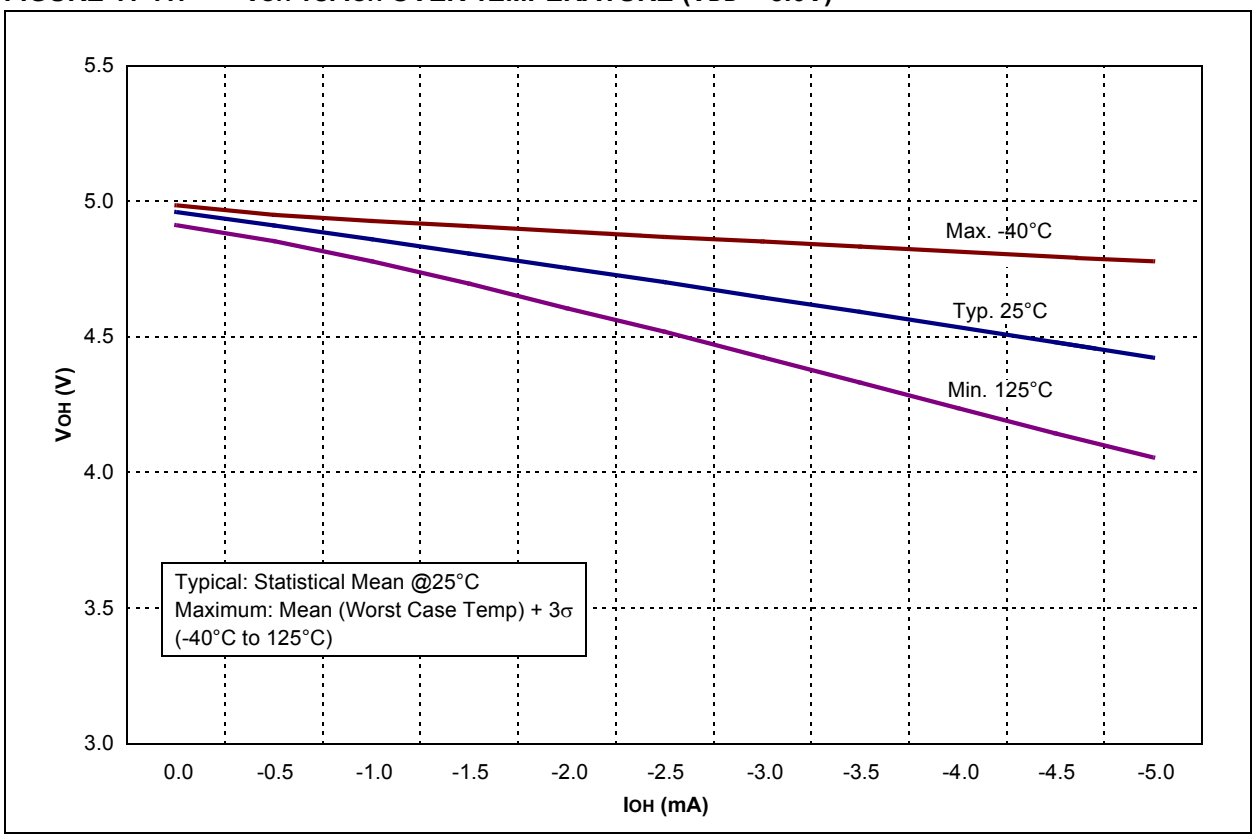
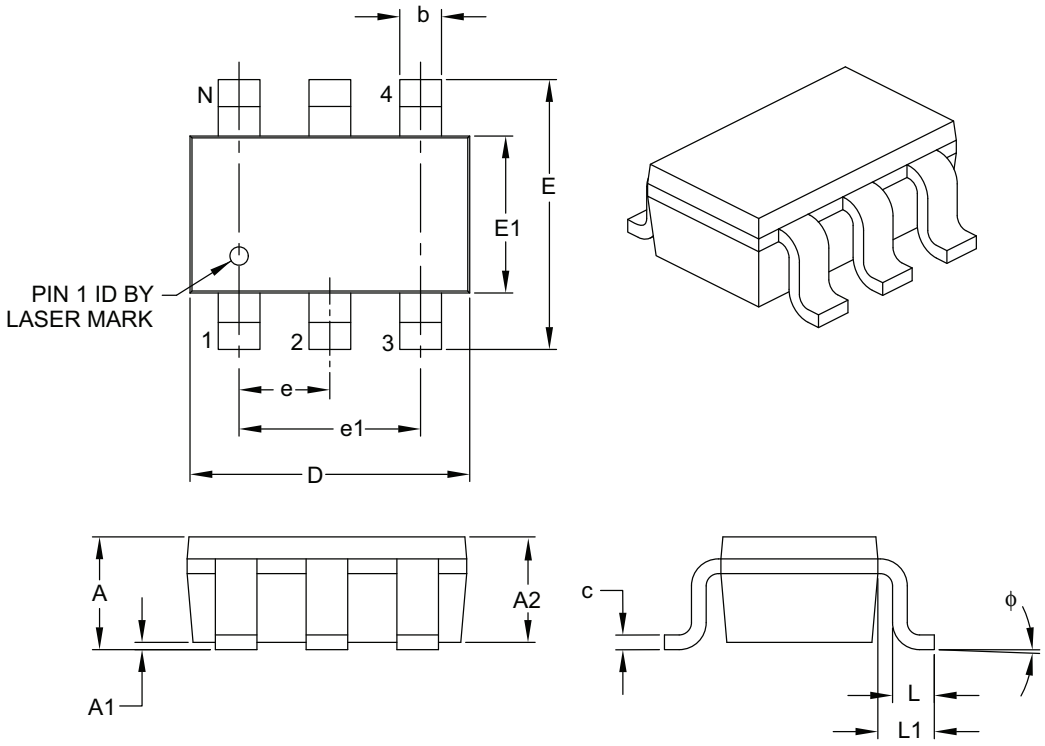


FIGURE 11-11: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)



6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

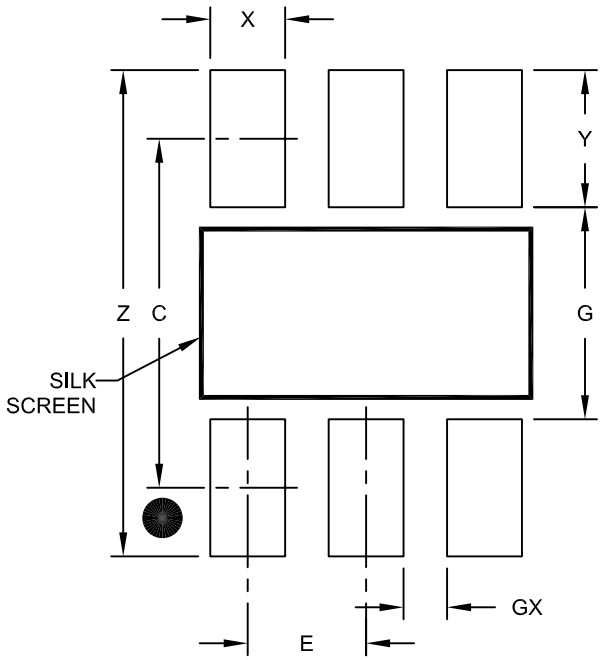
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

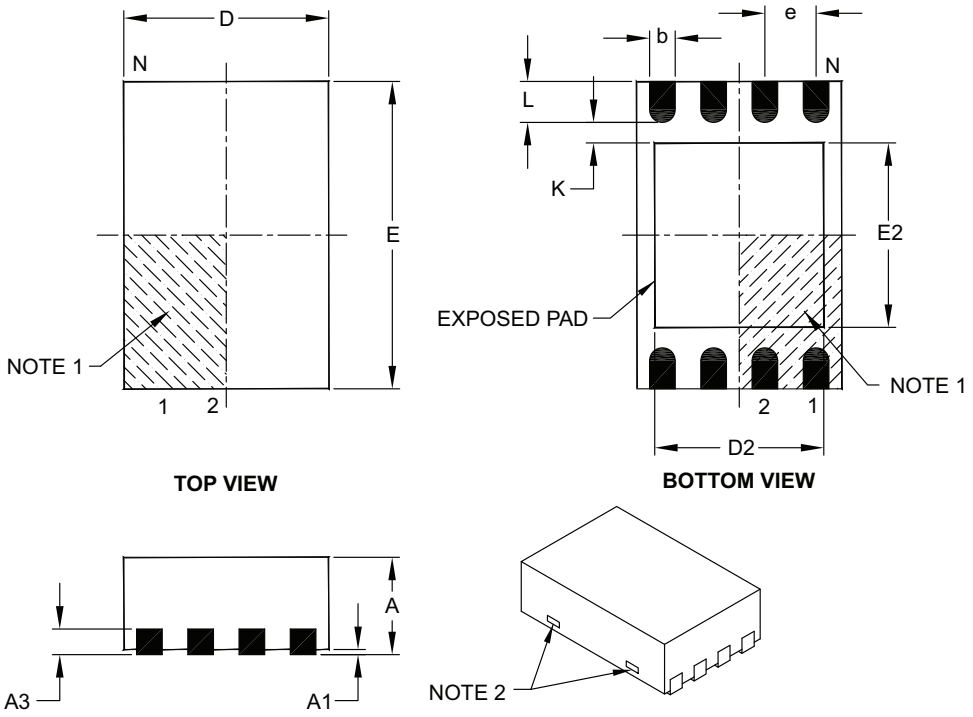
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

NOTES:

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/20/13