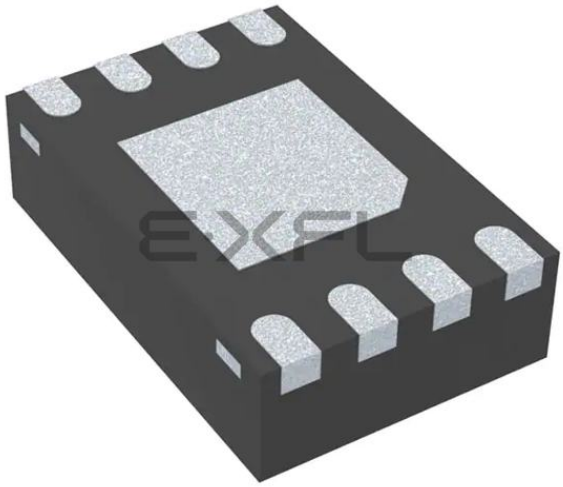


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	4
Program Memory Size	384B (256 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VFDFN Exposed Pad
Supplier Device Package	8-DFN (2x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f220t-i-mc

NOTES:

© 2005-2013 Microchip Technology Inc.

NOTES:

© 2005-2013 Microchip Technology Inc.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)	Page #
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	20
01h	TMR0	8-Bit Real-Time Clock/Counter								xxxx xxxx	25
02h	PCL(1)	Low Order 8 Bits of PC								1111 1111	19
03h	STATUS	GPWUF	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0--1 1xxx(3)	15
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx	20
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	FOSC4	1111 1110	18
06h	GPIO	—	—	—	—	GP3	GP2	GP1	GP0	---- xxxx	21
07h	ADCON0	ANS1	ANS0	—	—	CHS1	CHS0	GO/$\overline{DONE}$	ADON	11-- 1100	30
08h	ADRES	Result of Analog-to-Digital Conversion								xxxx xxxx	31
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111	23
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	17

Legend: – = unimplemented, read as '0', x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.7 "Program Counter"** for an explanation of how to access these bits.

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$, Watchdog Timer and wake-up on pin change Reset.

3: See Table 8-1 for other Reset specific values.

4.4 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

Therefore, it is recommended that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect Status bits, see Instruction Set Summary.

6.0 TMR0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

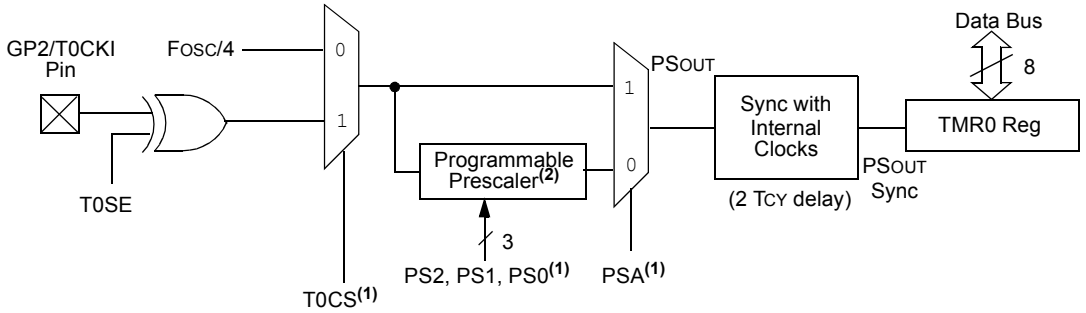
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 With An External Clock"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

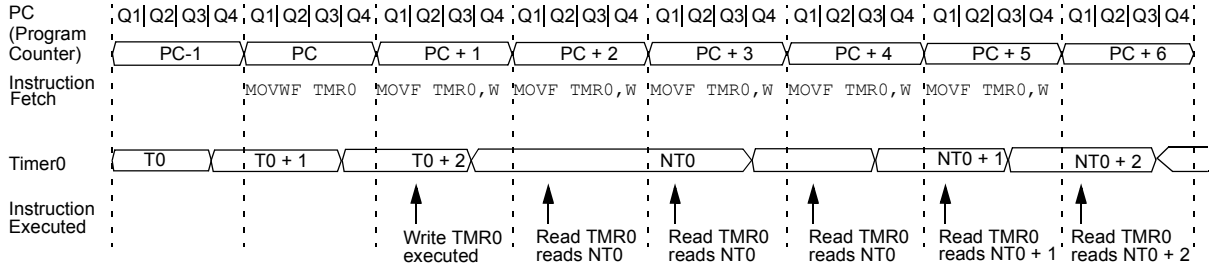
FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.

2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE



7.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D converter allows conversion of an analog signal into an 8-bit digital signal.

7.1 Clock Divisors

The A/D Converter has a single clock source setting, INTOSC/4. The A/D Converter requires 13 TAD periods to complete a conversion. The divisor values do not affect the number of TAD periods required to perform a conversion. The divisor values determine the length of the TAD period.

Note:	Due to the fixed clock divisor, a conversion will complete in 13 CPU instruction cycles.

7.2 Voltage Reference

Due to the nature of the design, there is no external voltage reference allowed for the A/D Converter. The A/D Converter reference voltage will always be VDD.

7.3 Analog Mode Selection

The ANS<1:0> bits are used to configure pins for analog input. Upon any Reset ANS<1:0> defaults to 11. This configures pins AN0 and AN1 as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

7.4 A/D Converter Channel Selection

The CHS bits are used to select the analog channel to be sampled by the A/D Converter. The CHS bits should not be changed during a conversion. To acquire an analog signal, the CHS selection must match one of the pin(s) selected by the ANS bits. The Internal Absolute Voltage Reference can be selected regardless of the condition of the ANS bits. All channel selection information will be lost when the device enters Sleep.

Note:	The A/D Converter module consumes power when the ADON bit is set even when no channels are selected as analog inputs. For low-power applications, it is recommended that the ADON bit be cleared when the A/D Converter is not in use.

7.5 The GO/$\overline{\text{DONE}}$ bit

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the A/D Converter module clears the GO/$\overline{\text{DONE}}$ bit. A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The A/D Converter does not have a dedicated oscillator, it runs off of the system clock.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

7.6 Sleep

This A/D Converter does not have a dedicated A/D Converter clock and therefore no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/$\overline{\text{DONE}}$ and ADON bit will be cleared. This will stop any conversion in process and power-down the A/D Converter module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The CHS bits are reset to their default condition and CHS<1:0> = 11.

For accurate conversions, TAD must meet the following:

- 500 ns < TAD < 50 μs
- TAD = 1/(FOSC/divisor)

TABLE 7-1: EFFECTS OF SLEEP AND WAKE ON ADCON0

	ANS1	ANS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
Prior to Sleep	x	x	x	x	0	0
Prior to Sleep	x	x	x	x	1	1
Entering Sleep	Unchanged	Unchanged	1	1	0	0
Wake	1	1	1	1	0	0

7.9 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 7-1. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 7-1. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 7-1 may be used. This equation assumes that 1/2 LSb error is used (256 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 7-1: ACQUISITION TIME EXAMPLE

Assumptions:

Temperature = 50°C and external impedance of 10 kΩ 5.0V VDD

Tacq = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient

= TAMP + TC + TCOFF

= 2 μs + TC + [(Temperature - 25°C)(0.05 μs/°C)]

Solving for Tc:

Tc = CHOLD (RIC + RSS + RS) In(1/512)

= -25pF (l kΩ + 7 kΩ + 10 kΩ) In(0.00196)

= 2.81 μs

Therefore:

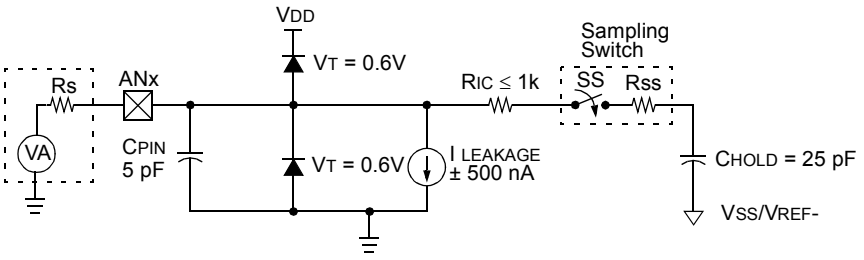
Tacq = 2 μs + 2.81 μs + [(50°C-25°C)(0.0 5μs/°C)]

= 6.06 μs

Note 1: The charge holding capacitor (CHOLD) is not discharged after each conversion.

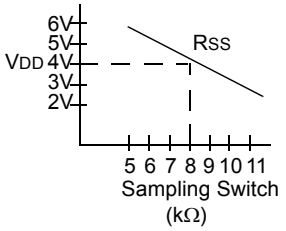
2: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 7-1: ANALOG INPUT MODULE



Legend:

CPIN	=	Input Capacitance
VT	=	Threshold Voltage
ILEAKAGE	=	Leakage current at the pin due to various junctions
RIC	=	Interconnect Resistance
SS	=	Sampling Switch
CHOLD	=	Sample/Hold Capacitance



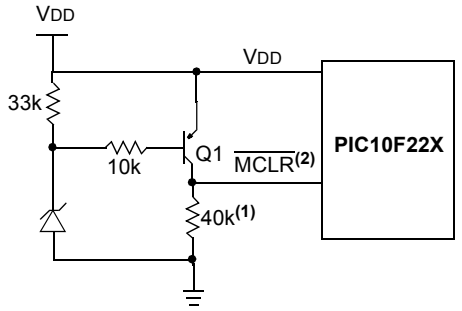
© 2005-2013 Microchip Technology Inc.

8.8 Reset on Brown-out

A Brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a Brown-out.

To reset PIC10F220/222 devices when a Brown-out occurs, external Brown-out protection circuits may be built, as shown in Figure 8-7 and Figure 8-8.

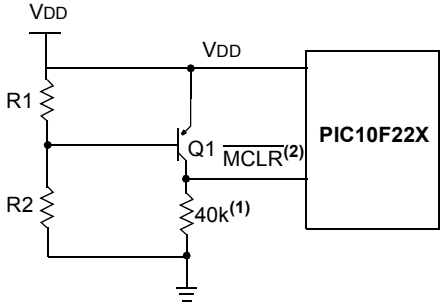
FIGURE 8-7: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

2: Pin must be configured as $\overline{MCLR}$.

FIGURE 8-8: BROWN-OUT PROTECTION CIRCUIT 2

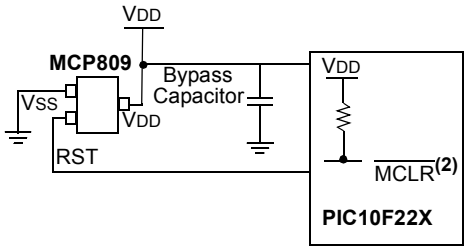


Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be configured as $\overline{MCLR}$.

FIGURE 8-9: BROWN-OUT PROTECTION CIRCUIT 3



Note 1: This Brown-out Protection circuit employs Microchip Technology's MCP809 micro-controller supervisor. There are 7 different trip point selections to accommodate 5V to 3V systems.

2: Pin must be configured as $\overline{MCLR}$.

8.9 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

8.9.1 SLEEP

The Power-Down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low or high-impedance).

Note: A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the GP3/$\overline{MCLR}$/VPP pin must be at a logic high level if $\overline{MCLR}$ is enabled.

© 2005-2013 Microchip Technology Inc.

10.1 DC Characteristics: PIC10F220/222 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40×C ≤ TA ≤ +85°C (industrial)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See **Figure 10-1**
D002	VDR	**RAM Data Retention Voltage(2)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	
D010	IDD	**Supply Current(3)**					
			— — — —	175 0.625 250 0.800	275 1.1 400 1.5	μA mA μA mA	VDD = 2.0V, Fosc = 4 MHz VDD = 5.0V, Fosc = 4 MHz VDD = 2.0V, Fosc = 8 MHz VDD = 5.0V, Fosc = 8 MHz
D020	IPD	**Power-down Current(4)**					
			— —	0.1 1	1.2 2.4	μA μA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(4)**					
			— —	1.0 7	3 16	μA μA	VDD = 2.0V VDD = 5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS. The peripheral current is the sum of the base IPD and the additional current consumed when the peripheral is enabled.

10.3 DC Characteristics: PIC10F220/222 (Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC specification				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	Vss	—	0.8	V	For all 4.5 ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	
D032		$\overline{MCLR}$, T0CKI	Vss	—	0.2 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$, T0CKI	0.8VDD	—	VDD	V	
D070	IPUR	**GPIO weak pull-up current**	50	250	400	µA	VDD = 5V, VPIN = VSS
	IIL	**Input Leakage Current(1)**					
D060		I/O ports	—	±0.1	± 1	µA	Vss ≤ VPIN ≤ VDD, Pin at high-impedance
D061		GP3/$\overline{MCLR}$(2)	—	±0.7	± 5	µA	Vss ≤ VPIN ≤ VDD
		Output Low Voltage					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
		Output High Voltage					
D090		I/O ports(2)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD – 0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
		Capacitive Loading Specs on Output Pins					
D101		All I/O pins	—	—	50*	pF	

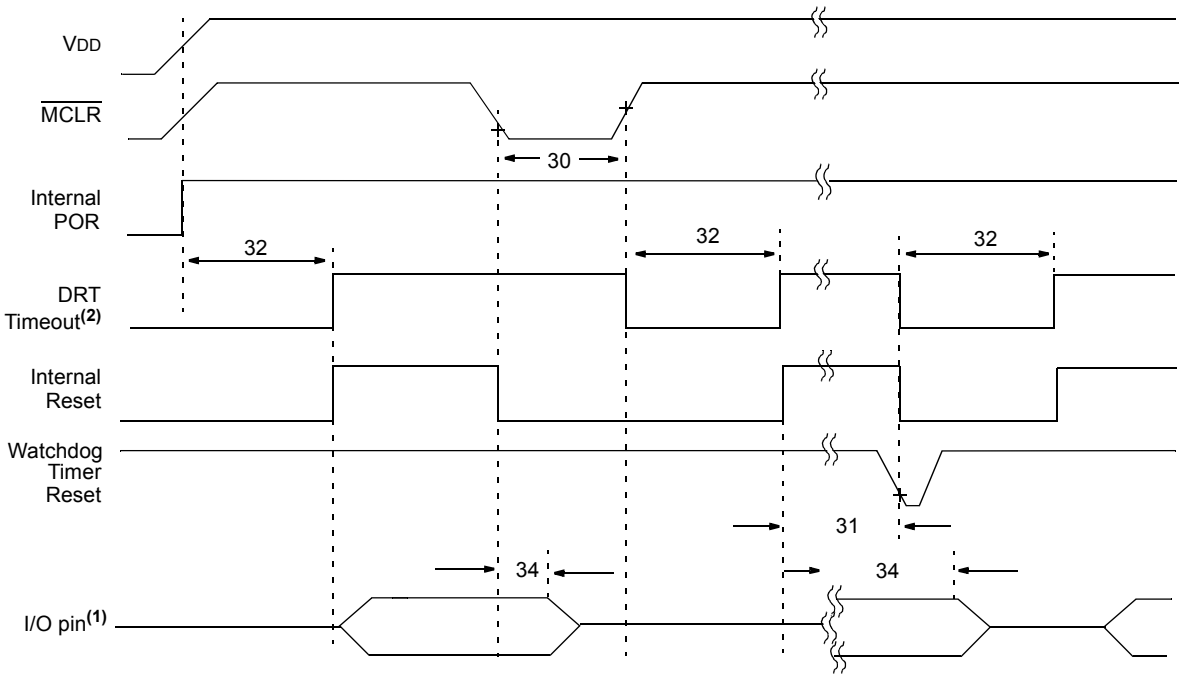
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as coming out of the pin.

2: This specification applies when GP3/$\overline{MCLR}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

FIGURE 10-3: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING



Note 1: I/O pins must be taken out of High-impedance mode by enabling the output drivers in software.
2: Runs on POR Reset only.

TABLE 10-3: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER – PIC10F220/222

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in **Section 10.1 "DC Characteristics: PIC10F220/222 (Industrial)"**				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	T_{MCL}	$\overline{MCLR}$ Pulse Width (low)	2* 5*	— —	— —	µs µs	VDD = 5V, -40°C to +85°C VDD = 5.0V
31	TWDT	Watchdog Timer Time-out Period (no prescaler)	10 10	18 18	29 31	ms ms	VDD = 5.0V (Industrial) VDD = 5.0V (Extended)
32	TDRT*	Device Reset Timer Period (standard)	0.600 0.600	1.125 1.125	1.85 1.95	ms ms	VDD = 5.0V (Industrial) VDD = 5.0V (Extended)
34	TIOZ	I/O High-impedance from $\overline{MCLR}$ low	—	—	2*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

© 2005-2013 Microchip Technology Inc.

TABLE 10-5: A/D CONVERTER CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
A01	NR	Resolution	—	—	8 bits	bit	
A03	EIL	Integral Error	—	—	±1.5	LSb	
A04	EDL	Differential Error	—	—	-1 < EDL ≤ + 1.5	LSb	
A05	EFS	Full-scale Range	2.0*	—	5.5*	V	
A06	EOFF	Offset Error	—	—	±1.5	LSb	
A07	EGN	Gain Error	—	—	±1.5	LSb	
A10	—	Monotonicity	—	guaranteed(1)	—	—	VSS ≤ VAIN ≤ VDD
A25	VAIN	Analog Input Voltage	VSS	—	VDD	V	
A30	ZAIN	Recommended Impedence of Analog Voltage Source	—	—	10	kΩ	
A31*	ΔIAD	A/D Conversion Current(2)	—	120	150	μA	2.0V
			—	200	250	μA	5.0V

* These parameters are characterized but not tested.

† Data in the "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only are not tested.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: This is the additional current consumed by the A/D module when it is enabled; this current adds to base IDD.

TABLE 10-6: A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD131	TCNV	Conversion Time (not including Acquisition Time)	—	13	—	TCY	Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register
AD132*	TACQ	Acquisition Time(1)	—	3.5 5	—	μs μs	VDD = 5V VDD = 2.5V

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The **Section 7.9 "A/D Acquisition Requirements"** for information on how to compute minimum acquisition times based on operating conditions.

© 2005-2013 Microchip Technology Inc.

FIGURE 11-6: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

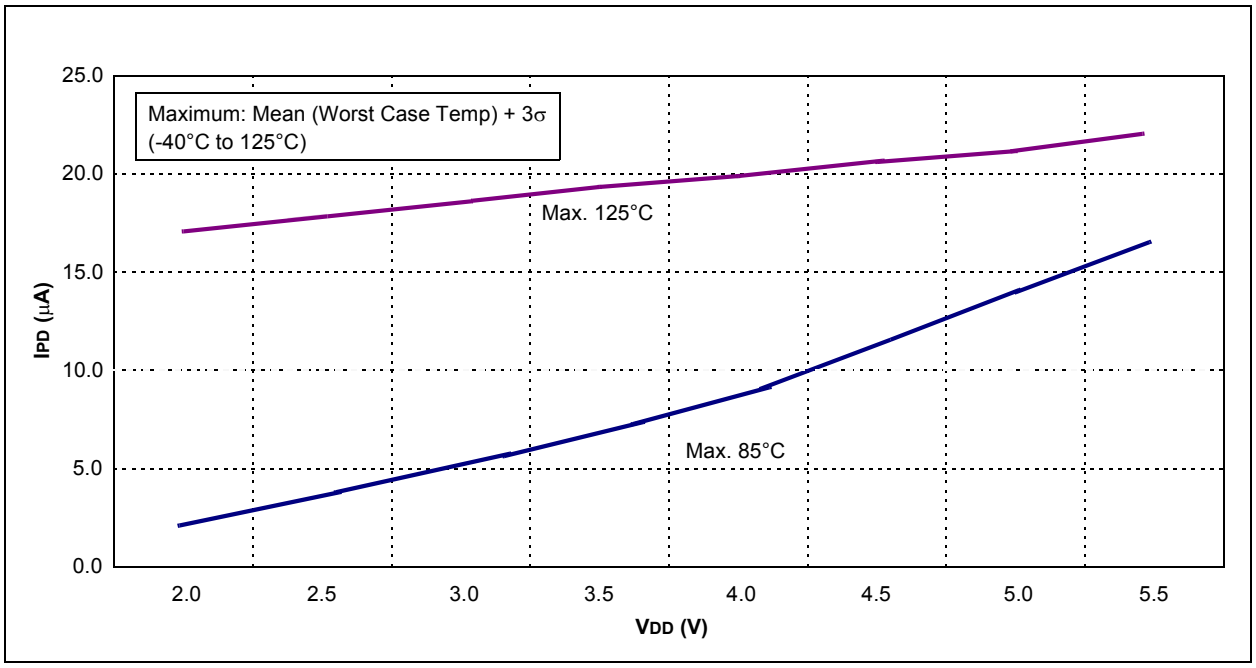
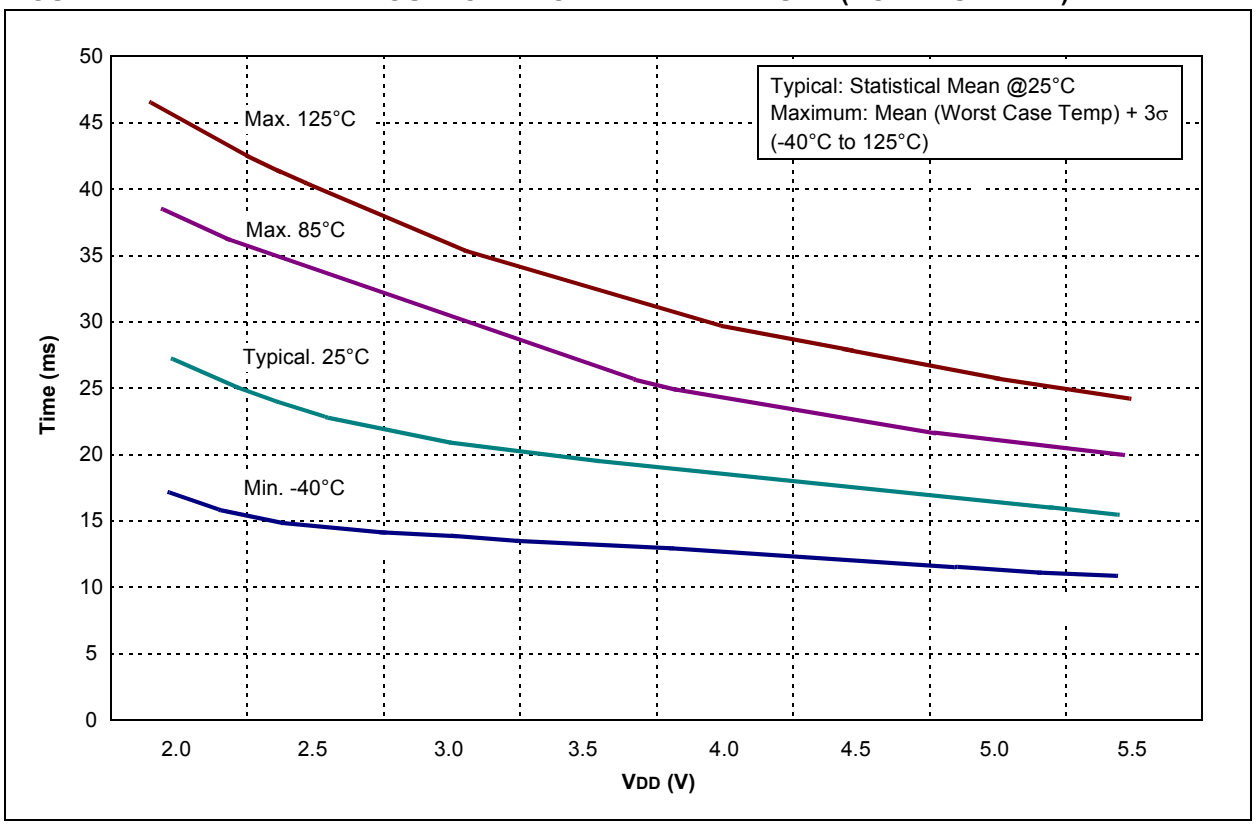


FIGURE 11-7: WDT TIME-OUT vs. VDD OVER TEMPERATURE (NO PRESCALER)



© 2005-2013 Microchip Technology Inc.

FIGURE 11-12: TTL INPUT THRESHOLD VIN vs. VDD

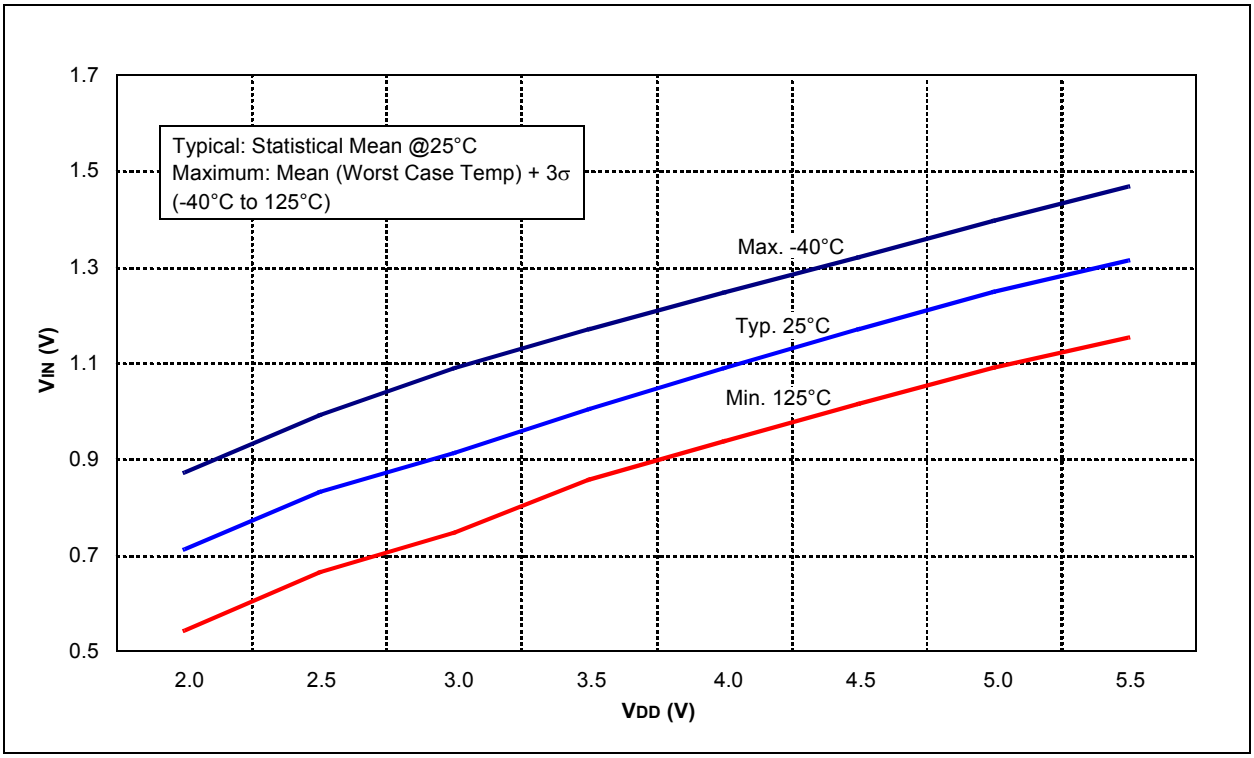
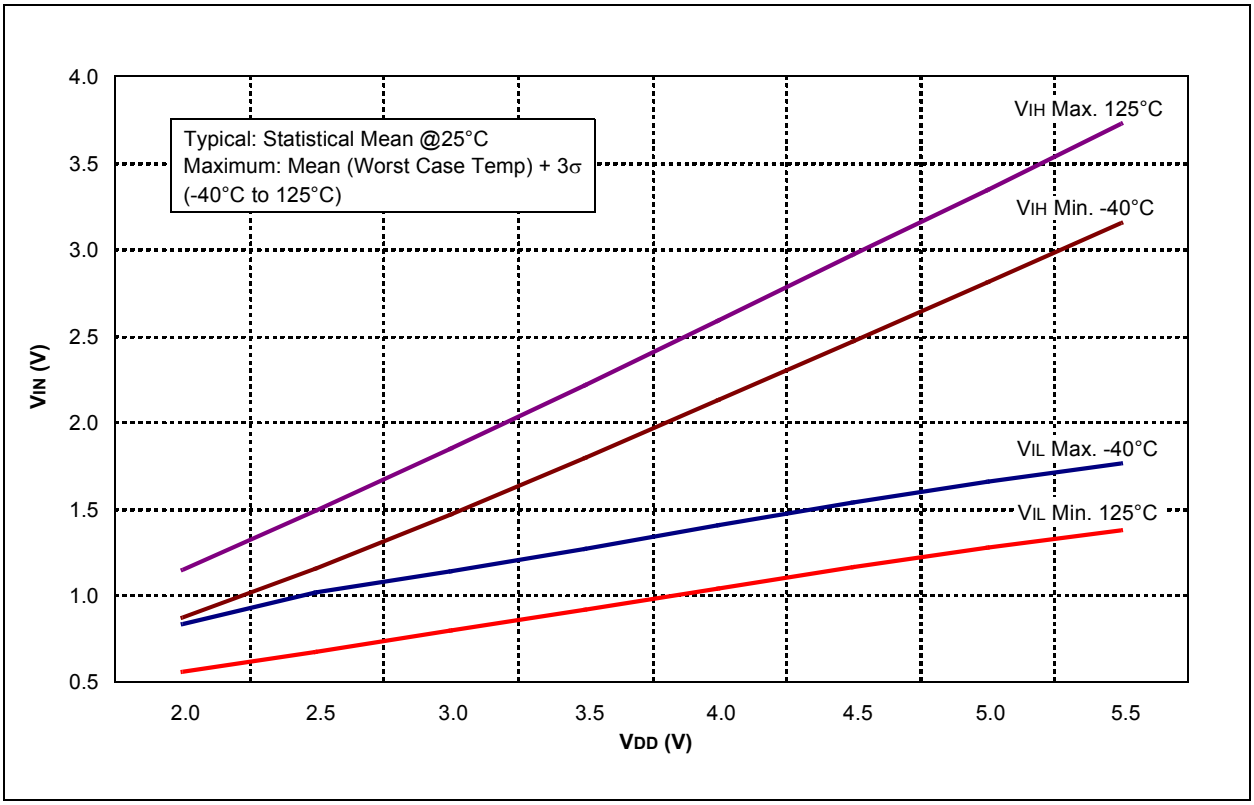


FIGURE 11-13: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD



12.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

12.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

12.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

12.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

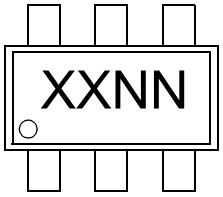
12.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

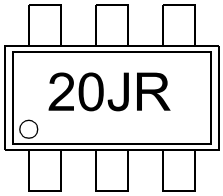
13.0 PACKAGING INFORMATION

13.1 Package Marking Information

6-Lead SOT-23*

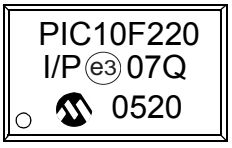


Example

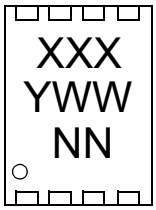


8-Lead PDIP

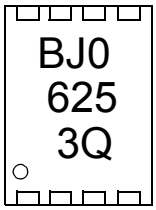
Example



8-Lead DFN*



Example

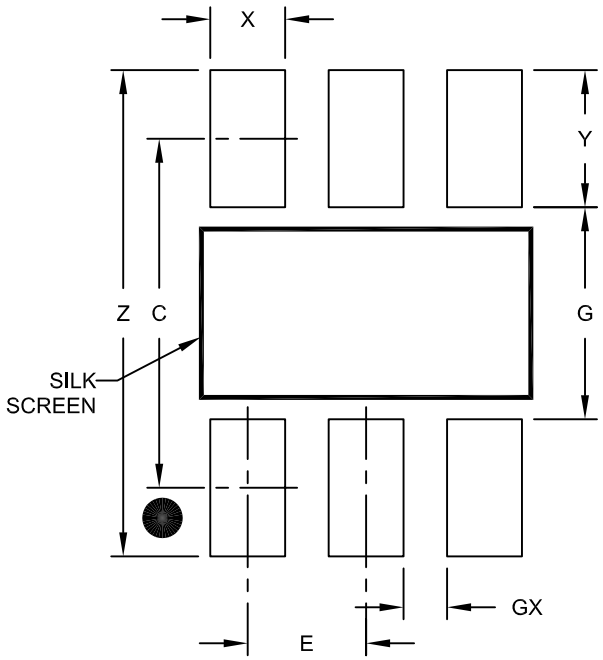


Legend:	XX...X	Product-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

© 2005-2013 Microchip Technology Inc.

W

Z

© 2005-2013 Microchip Technology Inc.

NOTES:

© 2005-2013 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC10F220 PIC10F222 PIC10F220T (Tape & Reel) PIC10F222T (Tape & Reel)	
Temperature Range:	I = -40°C to +85°C E = -40°C to +125°C	(Industrial) (Extended)
Package:	P = 300 mil PDIP (Pb-free) OT = SOT-23, 6-LD (Pb-free) MC = DFN, 8-LD 2x3 (Pb-free)	
Pattern:	Special Requirements	

Examples:

a) PIC10F220-I/P = Industrial temp., PDIP package (Pb-free)

b) PIC10F222T-E/OT = Extended temp., SOT-23 package (Pb-free), Tape and Reel

c) PIC10F222-E/MC = Extended temp., DFN package (Pb-free)

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/20/13

© 2005-2013 Microchip Technology Inc.