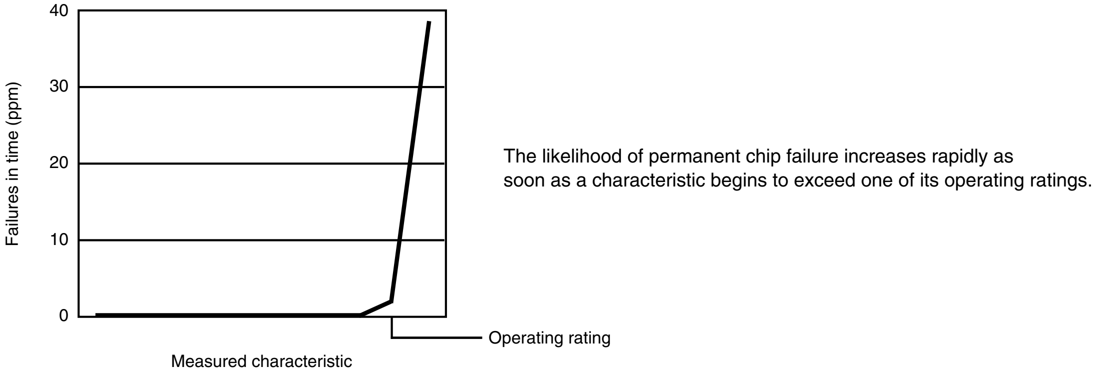
| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | Coldfire V1 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 19x12b; D/A 1x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51qu128vlhr |

### 3.4.1 Example

This is an example of an operating rating:

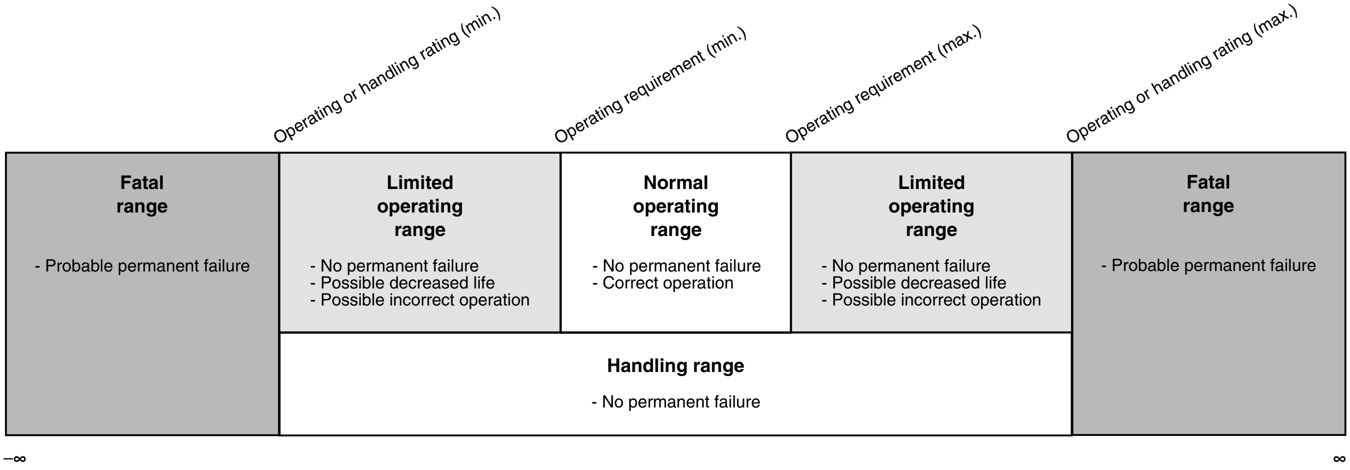
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 3.6 Relationship between ratings and operating requirements



## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

### 5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength<br>• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -9\ mA$<br>• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -3\ mA$ | <br>$V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | <br>—<br>— | <br>V<br>V | |
| | Output high voltage — low drive strength<br>• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -2\ mA$<br>• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -0.6\ mA$ | <br>$V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | <br>—<br>— | <br>V<br>V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength<br>• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 9\ mA$<br>• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 3\ mA$ | <br>—<br>— | <br>0.5<br>0.5 | <br>V<br>V | |
| | Output low voltage — low drive strength<br>• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 2\ mA$<br>• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 0.6\ mA$ | <br>—<br>— | <br>0.5<br>0.5 | <br>V<br>V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin)<br>• @ full temperature range<br>• @ 25 °C | <br>—<br>— | <br>1.0<br>0.1 | <br>μA<br>μA | 1 |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | |
| $I_{OZ}$ | Total Hi-Z (off-state) leakage current (all input pins) | — | 4 | μA | |
| $R_{PU}$ | Internal pullup resistors | 22 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 22 | 50 | kΩ | 3 |

1. Tested by ganged leakage method
2. Measured at Vinput = $V_{SS}$
3. Measured at Vinput = $V_{DD}$

### 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$ and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

5. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash memory.
6. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash memory.
7. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. OSC clocks disabled.
9. All pads disabled.
10. Data reflects devices with 32 KB of RAM. For devices with 16 KB of RAM, power consumption is reduced by 500 nA. For devices with 8 KB of RAM, power consumption is reduced by 750 nA.
11. RTC function current includes LPTMR with OSC enabled with 32.768 kHz crystal at 3.0 V

#### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL
- For the ALLON curve, all peripheral clocks are enabled, but peripherals are not in active operation
- Voltage Regulator disabled
- No GPIOs toggled
- Code execution from flash memory with cache enabled

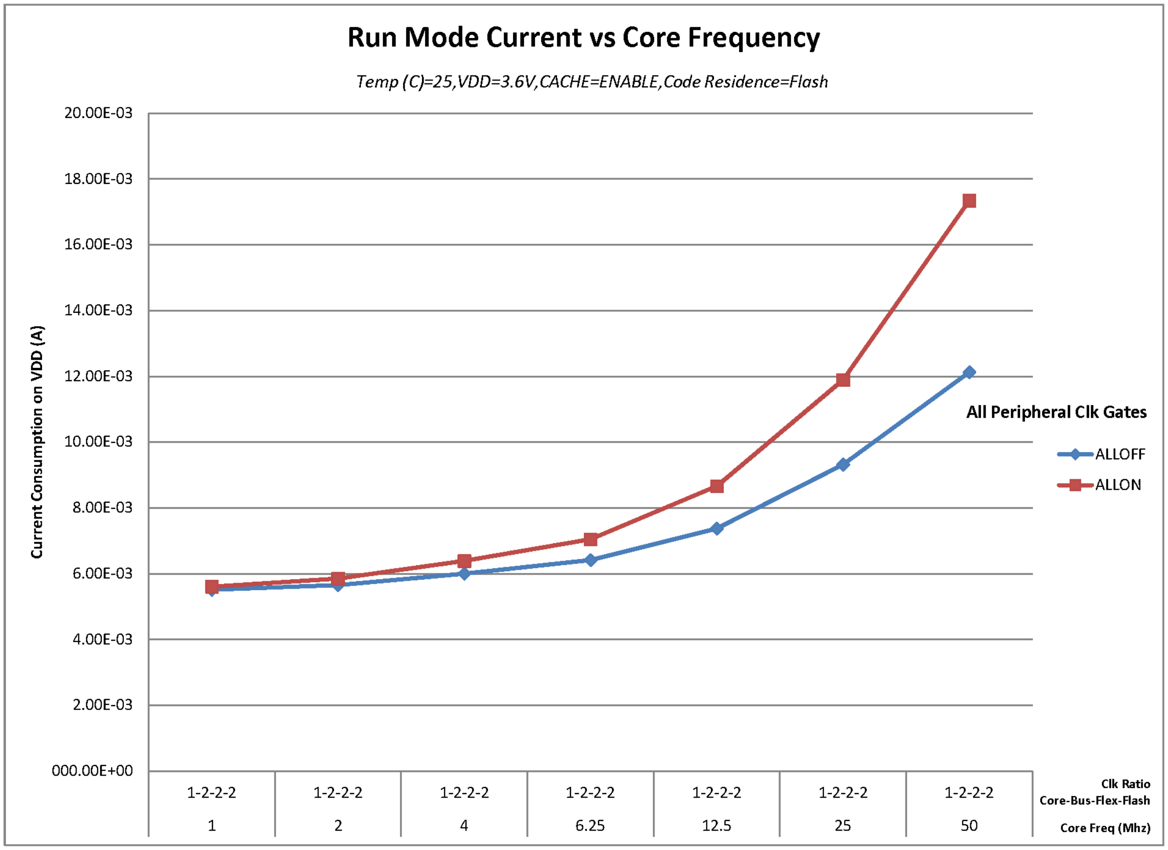


Figure 1. Run mode supply current vs. core frequency

### 5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and $I^2C$ signals. The conditions are 50 pf load, $V_{DD}$ = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

**Table 9. EGPIO General Control Timing**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| G1 | Bus clock from CLK_OUT pin high to GPIO output valid | — | 32 | ns |
| G2 | Bus clock from CLK_OUT pin high to GPIO output invalid (output hold) | 1 | — | ns |
| G3 | GPIO input valid to bus clock high | 28 | — | ns |
| G4 | Bus clock from CLK_OUT pin high to GPIO input invalid | — | 4 | ns |
| | GPIO pin interrupt pulse width (digital glitch filter disabled)<br>Synchronous path[1] | 1.5 | — | Bus clock cycles |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled)<br>Asynchronous path[2] | 100 | — | ns |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled)<br>Asynchronous path[2] | 50 | — | ns |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns |
| | Mode select (MS) hold time after reset deassertion | 2 | — | Bus clock cycles |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

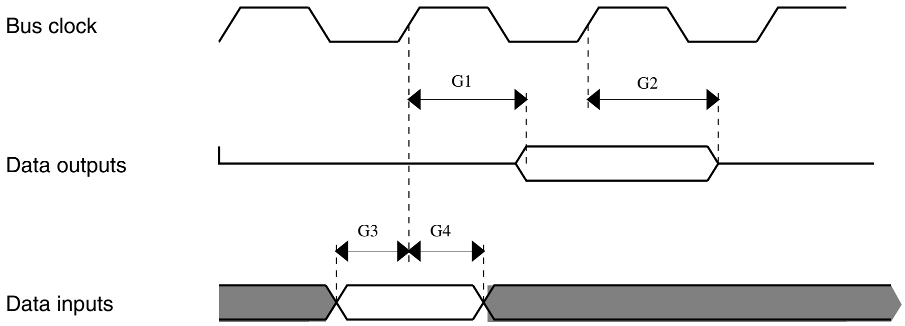


Figure 3. EGPIO timing diagram

## Table 14. MCG specifications (continued)

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00)<br>$732 \times f_{fll\_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01)<br>$1464 \times f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10)<br>$2197 \times f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11)<br>$2929 \times f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 6 |
| PLL | | | | | | | |
| $f_{vco}$ | VCO operating frequency | | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 48) | | — | 1060 | — | µA | 7 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 24) | | — | 600 | — | µA | 7 |
| $f_{pll\_ref}$ | PLL reference frequency range | | 2.0 | — | 4.0 | MHz | |
| $J_{cyc\_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | | —<br>— | 120<br>50 | —<br>— | ps<br>ps | 8 |
| $J_{acc\_pll}$ | PLL accumulated jitter over 1µs (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | | —<br>— | 1350<br>600 | —<br>— | ps<br>ps | 8 |
| $D_{lock}$ | Lock entry frequency tolerance | | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll\_lock}$ | Lock detector detection time | | — | — | $150 \times 10^{-6} + 1075(1/f_{pll\_ref})$ | s | 9 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

## Table 15. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | | | | | |
| | • 1 MHz resonator | — | 6.6 | — | kΩ | |
| | • 2 MHz resonator | — | 3.3 | — | kΩ | |
| | • 4 MHz resonator | — | 0 | — | kΩ | |
| | • 8 MHz resonator | — | 0 | — | kΩ | |
| | • 16 MHz resonator | — | 0 | — | kΩ | |
| | • 20 MHz resonator | — | 0 | — | kΩ | |
| | • 32 MHz resonator | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 17. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | μs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk32k}$ | Erase Block high-voltage time for 32 KB | — | 52 | 452 | ms | 1 |
| $t_{hversblk128k}$ | Erase Block high-voltage time for 128 KB | — | 208 | 1808 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk32k}$ | • 32 KB data flash | — | — | 0.5 | ms | |
| $t_{rd1blk128k}$ | • 128 KB program flash | — | — | 1.7 | ms | |
| $t_{rd1sec1k}$ | Read 1s Section execution time (data flash sector) | — | — | 60 | μs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | μs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | μs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | μs | |
| | Erase Flash Block execution time | | | | | 2 |
| $t_{ersblk32k}$ | • 32 KB data flash | — | 55 | 465 | ms | |
| $t_{ersblk128k}$ | • 128 KB program flash | — | 220 | 1850 | ms | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| | Program Section execution time | | | | | |
| $t_{pgmsec512}$ | • 512 B flash | — | 4.7 | — | ms | |
| $t_{pgmsec1k}$ | • 1 KB flash | — | 9.3 | — | ms | |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | μs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | μs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 275 | 2350 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | μs | 1 |
| | Program Partition for EEPROM execution time | | | | | |
| $t_{pgmpart32k}$ | • 32 KB FlexNVM | — | 70 | — | ms | |

*Table continues on the next page...*

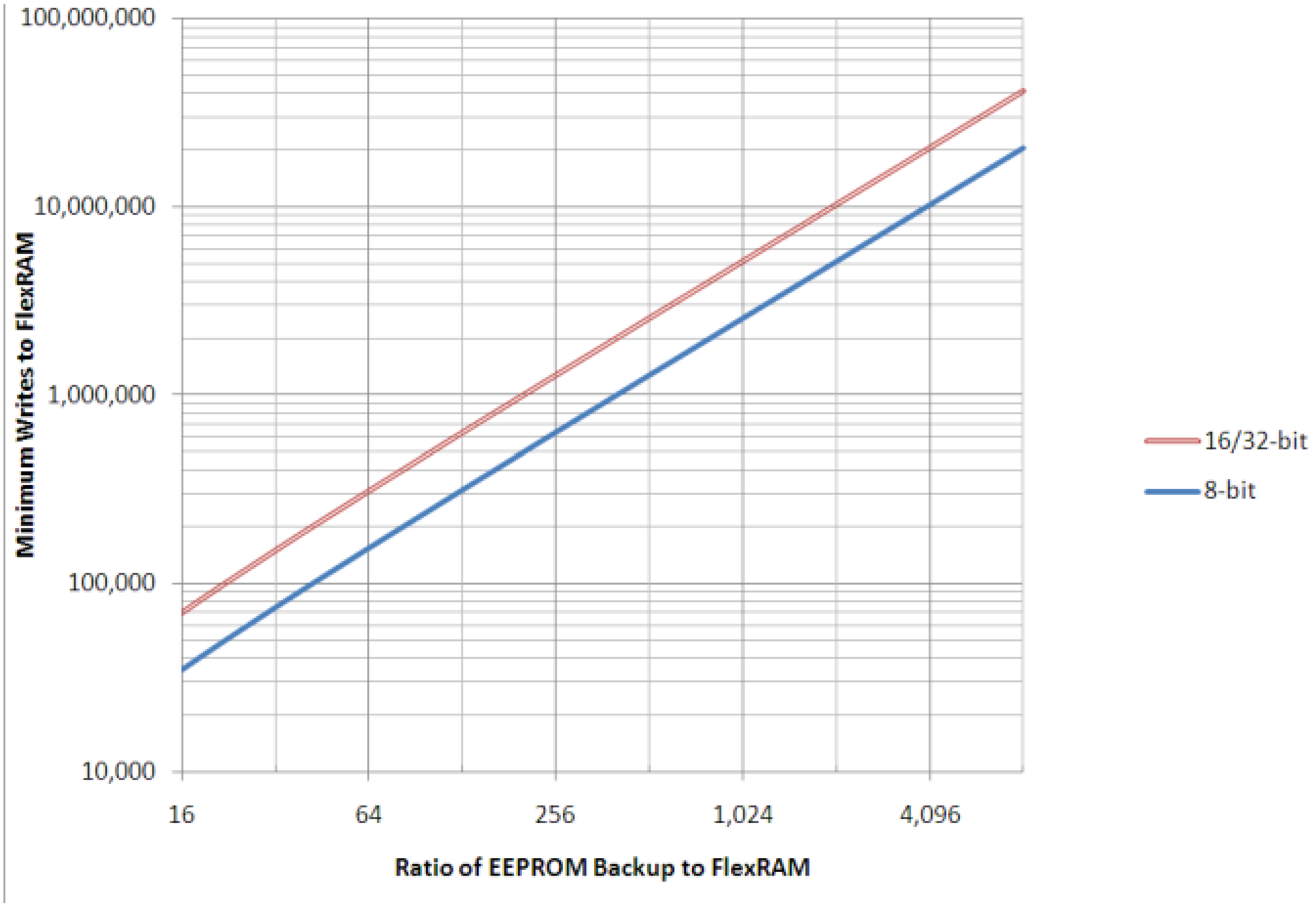


**Figure 5. EEPROM backup writes to FlexRAM**

### 6.4.2 EzPort Switching Specifications

All timing is shown with respect to a maximum pin load of 50 pF and input signal transitions of 3 ns.

**Table 21. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion | 2 x $t_{EZP\_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup) | 15 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold) | 0.0 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 15 | — | ns |

*Table continues on the next page...*

**Table 21. EzPort switching specifications (continued)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 0.0 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid (setup) | — | 25 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0.0 | — | ns |
| EP9 | $\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

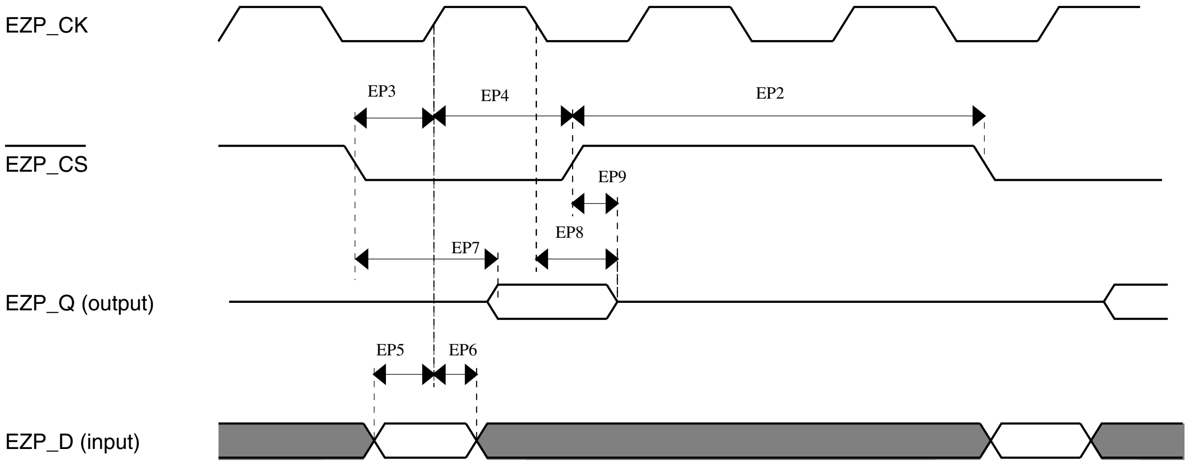


Figure 6. EzPort Timing Diagram

## 6.4.3 Mini-Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

**Table 22. Flexbus switching specifications**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| FB1 | Clock period | 40 | — | ns | |

*Table continues on the next page...*

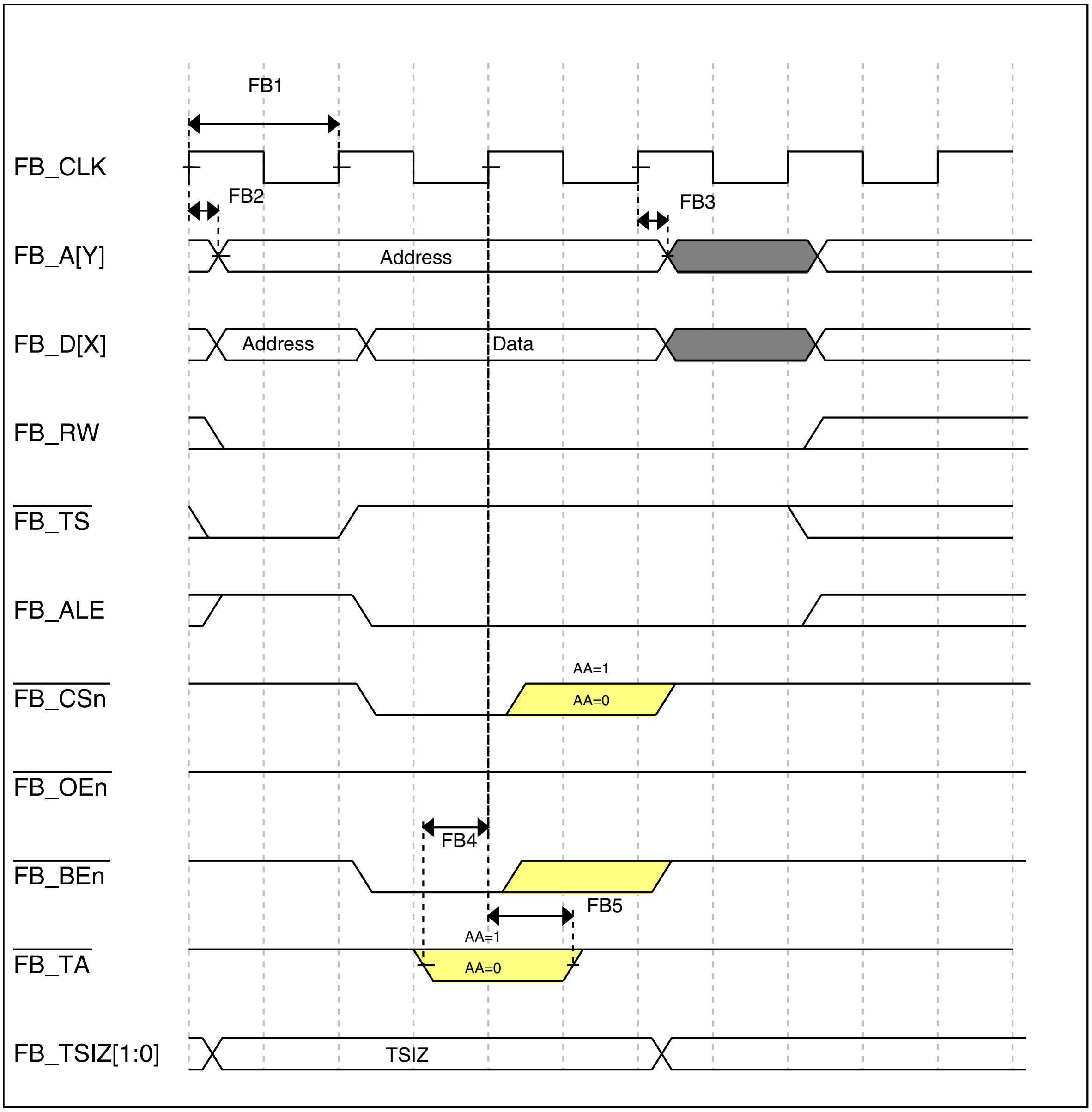


Figure 8. Mini-FlexBus write timing diagram

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

# 6.6 Analog

## 6.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

### 6.6.1.1 12-bit ADC operating conditions

Table 23. 12-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$-$V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | Reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $C_{ADIN}$ | Input capacitance | • 8/10/12 bit modes | —<br>— | 4 | 5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 12 bit modes<br>$f_{ADCK}$ < 4MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 12 bit modes | 1.0 | — | 18.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 12 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The $R_{AS}$/$C_{AS}$ time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.

## 6.8 Communication interfaces

### 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

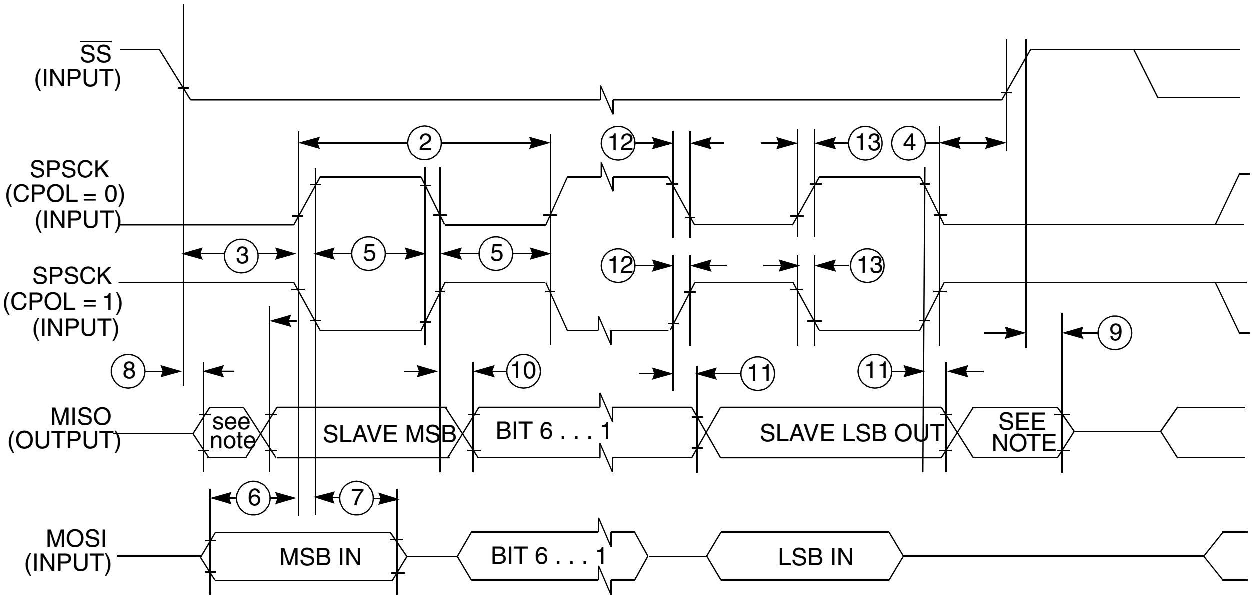
All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

**Table 32. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{BUS}$/2048 | $f_{BUS}$/2 | Hz | $f_{BUS}$ is the bus clock as defined in Table 8. |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{BUS}$ | 2048 x $t_{BUS}$ | ns | $t_{BUS}$ = 1/ $f_{BUS}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | 1024 x $t_{BUS}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 21 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
|  | $t_{FI}$ | Fall time input |  |  |  |  |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
|  | $t_{FO}$ | Fall time output |  |  |  |  |

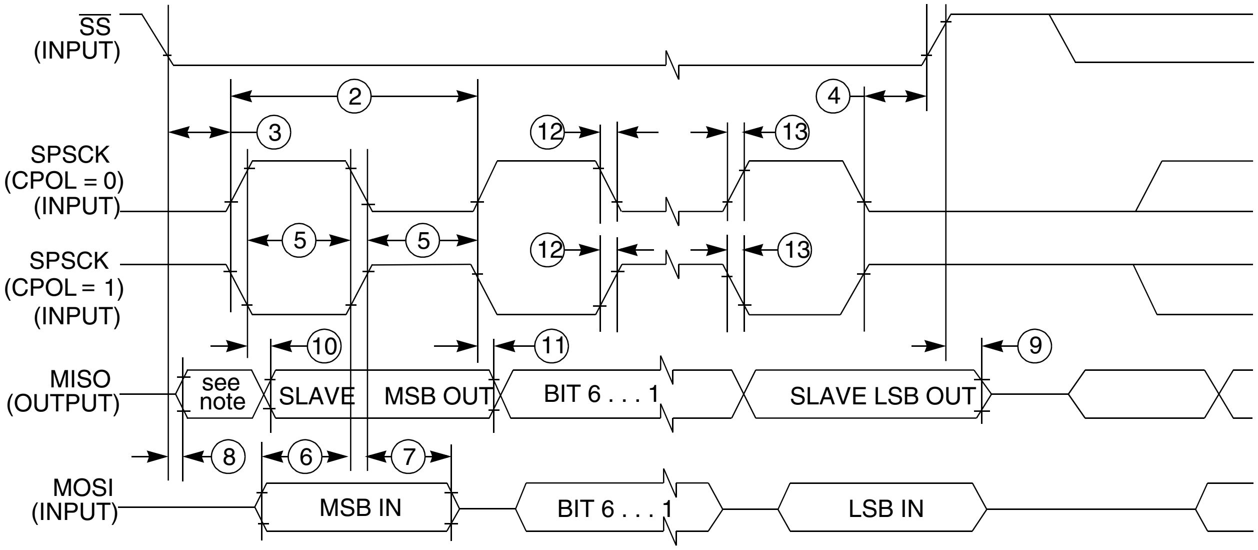
## Table 33. SPI slave mode timing (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{BUS}$ | — | ns | $t_{BUS}$ = 1/ $f_{BUS}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{BUS}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{BUS}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 19.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{BUS}$ | ns | Time to data active from high-impedance state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{BUS}$ | ns | Hold time to high-impedance state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 27 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
|  | $t_{FI}$ | Fall time input |  |  |  |  |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
|  | $t_{FO}$ | Fall time output |  |  |  |  |



NOTE: Not defined!

Figure 16. SPI slave mode timing (CPHA=0)



NOTE: Not defined!

**Figure 17. SPI slave mode timing (CPHA=1)**

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 34. TSI electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDTSI}$ | Operating voltage | 1.71 | — | 3.6 | V | |
| $C_{ELE}$ | Target electrode capacitance range | 1 | 20 | 500 | pF | 1 |
| $f_{REFmax}$ | Reference oscillator frequency | — | 5.5 | 14 | MHz | 2 |
| $f_{ELEmax}$ | Electrode oscillator frequency | — | 0.5 | 4.0 | MHz | 3 |
| $C_{REF}$ | Internal reference capacitor | 0.5 | 1 | 1.2 | pF | |
| $V_{DELTA}$ | Oscillator delta voltage | 100 | 600 | 760 | mV | 4 |
| $I_{REF}$ | Reference oscillator current source base current<br>• 1uA setting (REFCHRG=0)<br>• 32uA setting (REFCHRG=31) | —<br>— | 1.133<br>36 | 1.5<br>50 | μA | 3 , 5 |
| $I_{ELE}$ | Electrode oscillator current source base current<br>• 1uA setting (EXTCHRG=0)<br>• 32uA setting (EXTCHRG=31) | —<br>— | 1.133<br>36 | 1.5<br>50 | μA | 3 , 6 |
| Pres5 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 7 |
| Pres20 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 8 |
| Pres100 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 9 |
| MaxSens | Maximum sensitivity | 0.003 | 12.5 | — | fF/count | 10 |

*Table continues on the next page...*

# 8 Pinout

## 8.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Mux Control module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | — | — | — | VDD | VDD | | | | | | | | |
| 2 | — | — | — | VSS | VSS | | | | | | | | |
| 3 | — | — | — | Disabled | Disabled | PTC6 | UART0_TX | I2C0_SCL | RGPIO6 | SPI1_MOSI | FBa_AD11 | | |
| 4 | — | — | — | Disabled | Disabled | PTC7 | UART0_RX | I2C0_SDA | RGPIO7 | SPI1_MISO | FBa_AD12 | | |
| 5 | 1 | — | — | Disabled | Disabled | PTD0 | UART0_CTS_b | I2C1_SDA | RGPIO8 | SPI1_SCLK | FBa_AD13 | | |
| 6 | 2 | — | — | Disabled | Disabled | PTD1 | UART0_RTS_b | I2C1_SCL | RGPIO9 | SPI1_SS | FBa_AD14 | | |
| 7 | 3 | 1 | 1 | Disabled | Disabled | PTA0 | | I2C2_SCL | FTM1_CH0 | SPI0_SS | FBa_AD15 | | |
| 8 | 4 | 2 | 2 | Disabled | Disabled | PTA1 | | I2C2_SDA | FTM1_CH1 | | FBa_AD16 | | |
| 9 | 5 | 3 | 3 | Disabled | Disabled | PTA2 | UART1_TX | | FTM1_CH2 | SPI1_SS | | | |
| 10 | 6 | 4 | 4 | Disabled | Disabled | PTA3 | UART1_RX | | FTM1_CH3 | SPI1_SCLK | | | EZP_CLK |
| 11 | 7 | 5 | 5 | ADC0_SE2 | ADC0_SE2 | PTA4 | UART1_CTS_b | I2C2_SCL | FTM1_CH4 | SPI1_MISO | | | EZP_DI |
| 12 | 8 | 6 | 6 | ADC0_SE3 | ADC0_SE3 | PTA5 | UART1_RTS_b | I2C2_SDA | FTM1_CH5 | SPI1_MOSI | CLKOUT | | EZP_DO |
| 13 | 9 | 7 | 7 | VDDA | VDDA | | | | | | | | |
| 14 | 10 | 8 | — | VREFH | VREFH | | | | | | | | |
| 15 | 11 | 9 | — | VREF_OUT | VREF_OUT | | | | | | | | |
| 16 | 12 | 10 | — | VREFL | VREFL | | | | | | | | |
| 17 | 13 | 11 | 8 | VSSA | VSSA | | | | | | | | |
| 18 | 14 | 12 | 9 | DAC0_OUT | DAC0_OUT | | | | | | | | |
| 19 | 15 | 13 | 10 | ADC0_SE0 | ADC0_SE0 | | | | | | | | |
| 20 | 16 | 14 | 11 | ADC0_SE1 | ADC0_SE1 | | | | | | | | |
| 21 | 17 | 15 | 12 | VREGIN | VREGIN | | | | | | | | |
| 22 | 18 | 16 | 13 | VOUT33 | VOUT33 | | | | | | | | |
| 23 | 19 | 17 | 14 | VSS | VSS | | | | | | | | |

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24 | 20 | 18 | — | VDD | VDD | | | | | | | | |
| 25 | 21 | 19 | 15 | ADC0_SE8/TSI0_CH0 | ADC0_SE8/TSI0_CH0 | PTA6 | | LPTMR_ALT1 | FTM_FLT1 | FBa_D7 | FBa_AD17 | | |
| 26 | — | — | — | ADC0_SE9/TSI0_CH1 | ADC0_SE9/TSI0_CH1 | PTD2 | FTM0_QD_PHA | RGPIO10 | FTM0_CH0 | | | | |
| 27 | 22 | 20 | — | ADC0_SE10/TSI0_CH2 | ADC0_SE10/TSI0_CH2 | PTD3 | FTM0_QD_PHB | RGPIO11 | FTM0_CH1 | FBa_D6 | FBa_AD0 | | |
| 28 | — | — | — | ADC0_SE11/TSI0_CH3 | ADC0_SE11/TSI0_CH3 | PTD4 | | RGPIO12 | | | FBa_D7 | | |
| 29 | — | — | — | ADC0_SE12/TSI0_CH4 | ADC0_SE12/TSI0_CH4 | PTD5 | | RGPIO13 | | | FBa_D6 | | |
| 30 | 23 | 21 | 16 | ADC0_SE13/TSI0_CH5 | ADC0_SE13/TSI0_CH5 | PTA7 | UART0_TX | | FTM0_QD_PHA | | FBa_D5 | | |
| 31 | 24 | 22 | — | ADC0_SE14/TSI0_CH6 | ADC0_SE14/TSI0_CH6 | PTD6 | UART0_RX | RGPIO14 | | | FBa_D4 | | |
| 32 | — | — | — | ADC0_SE15/TSI0_CH7 | ADC0_SE15/TSI0_CH7 | PTD7 | UART0_CTS_b | I2C3_SCL | RGPIO15 | | FBa_D3 | | |
| 33 | — | — | — | TSI0_CH8 | TSI0_CH8 | PTE0 | UART0_RTS_b | I2C3_SDA | | | FBa_D2 | | |
| 34 | — | — | — | TSI0_CH9 | TSI0_CH9 | PTE1 | SPI0_SS | | FTM_FLT0 | | FBa_D1 | | |
| 35 | 25 | 23 | 17 | IRQ/EZP_MS_b | Disabled | PTB0 | | I2C0_SCL | | IRQ/EZP_MS_b | | | EZP_CS_b |
| 36 | 26 | 24 | 18 | TSI0_CH10 | TSI0_CH10 | PTB1 | SPI0_SCLK | I2C0_SDA | FTM_FLT2 | LPTMR_ALT2 | FTM0_QD_PHB | FB_CLKOUT | |
| 37 | — | — | — | TSI0_CH11 | TSI0_CH11 | PTE2 | | I2C3_SCL | | | FBa_D0 | | |
| 38 | — | — | — | ADC0_SE16/TSI0_CH12 | ADC0_SE16/TSI0_CH12 | PTE3 | SPI0_MOSI | I2C3_SDA | | | FBa_OE_b | | |
| 39 | 27 | 25 | 19 | ADC0_SE17/TSI0_CH13 | ADC0_SE17/TSI0_CH13 | PTB2 | SPI0_MISO | | | | FBa_CS0_b | | |
| 40 | 28 | 26 | 20 | ADC0_SE18/TSI0_CH14 | ADC0_SE18/TSI0_CH14 | PTB3 | SPI0_MOSI | | | FBa_CS1_b | FBa_ALE | | |
| 41 | 29 | — | — | ADC0_SE19/TSI0_CH15 | ADC0_SE19/TSI0_CH15 | PTE4 | UART0_RTS_b | LPTMR_ALT3 | SPI1_SS | | FBa_AD1 | | |
| 42 | 30 | — | — | ADC0_SE20 | ADC0_SE20 | PTE5 | UART0_CTS_b | I2C1_SCL | SPI1_SCLK | | FBa_AD2 | | |
| 43 | — | — | — | ADC0_SE21 | ADC0_SE21 | PTE6 | UART0_RX | I2C1_SDA | SPI1_MISO | | FBa_AD3 | | |
| 44 | 31 | 27 | — | ADC0_SE22 | ADC0_SE22 | PTE7 | UART0_TX | PDB0_EXTRG | SPI1_MOSI | FBa_RW_b | FBa_AD4 | | |
| 45 | 32 | 28 | 21 | BKGD/MS | Disabled | PTB4 | BKGD/MS | | | | | | |
| 46 | 33 | 29 | 22 | XTAL2 | XTAL2 | PTB5 | | | | | | | |
| 47 | 34 | 30 | 23 | EXTAL2 | EXTAL2 | PTB6 | | | | | | | |
| 48 | 35 | 31 | 24 | VDD | VDD | | | | | | | | |

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 48 | 35 | 31 | 24 | | VDD |
| 2 | | | | | VSS |
| 23 | 19 | 17 | 14 | | VSS |
| 49 | 36 | 32 | 25 | | VSS |
| System | | | | | |
| 45 | 32 | 28 | 21 | PTB4 | BKGD/MS |
| 12 | 8 | 6 | 6 | PTA5 | CLKOUT |
| 62 | 46 | 42 | 30 | PTC3 | CLKOUT |
| 10 | 6 | 4 | 4 | PTA3 | EZP_CLK |
| 11 | 7 | 5 | 5 | PTA4 | EZP_DI |
| 12 | 8 | 6 | 6 | PTA5 | EZP_DO |
| 35 | 25 | 23 | 17 | PTB0 | IRQ/EZP_MS_b, EZP_CS_b |
| 52 | 39 | 35 | 28 | PTC1 | RESET_b |
| OSC | | | | | |
| 50 | 37 | 33 | 26 | PTB7 | EXTAL1 |
| 47 | 34 | 30 | 23 | PTB6 | EXTAL2 |
| 51 | 38 | 34 | 27 | PTC0 | XTAL1 |
| 46 | 33 | 29 | 22 | PTB5 | XTAL2 |
| LLWU | | | | | |
| 4 | | | | PTC7 | LLWU_P0 |
| 6 | 2 | | | PTD1 | LLWU_P1 |
| 12 | 8 | 6 | 6 | PTA5 | LLWU_P2 |
| 30 | 23 | 21 | 16 | PTA7 | LLWU_P3 |
| 32 | | | | PTD7 | LLWU_P4 |
| 35 | 25 | 23 | 17 | PTB0 | LLWU_P5 |
| 36 | 26 | 24 | 18 | PTB1 | LLWU_P6 |
| 39 | 27 | 25 | 19 | PTB2 | LLWU_P7 |
| 44 | 31 | 27 | | PTE7 | LLWU_P8 |
| 45 | 32 | 28 | 21 | PTB4 | LLWU_P9 |
| 55 | | | | PTF2 | LLWU_P10 |
| 56 | 40 | 36 | | PTF3 | LLWU_P11 |
| 57 | 41 | 37 | 29 | PTC2 | LLWU_P12 |
| 59 | 43 | 39 | | PTF5 | LLWU_P13 |
| 62 | 46 | 42 | 30 | PTC3 | LLWU_P14 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 11 | 7 | 5 | 5 | PTA4 | PTA4 |
| 12 | 8 | 6 | 6 | PTA5 | PTA5 |
| 25 | 21 | 19 | 15 | PTA6 | PTA6 |
| 30 | 23 | 21 | 16 | PTA7 | PTA7 |
| PTB | | | | | |
| 35 | 25 | 23 | 17 | PTB0 | PTB0 |
| 36 | 26 | 24 | 18 | PTB1 | PTB1 |
| 39 | 27 | 25 | 19 | PTB2 | PTB2 |
| 40 | 28 | 26 | 20 | PTB3 | PTB3 |
| 45 | 32 | 28 | 21 | PTB4 | PTB4 |
| 46 | 33 | 29 | 22 | PTB5 | PTB5 |
| 47 | 34 | 30 | 23 | PTB6 | PTB6 |
| 50 | 37 | 33 | 26 | PTB7 | PTB7 |
| PTC | | | | | |
| 51 | 38 | 34 | 27 | PTC0 | PTC0 |
| 52 | 39 | 35 | 28 | PTC1 | PTC1 |
| 57 | 41 | 37 | 29 | PTC2 | PTC2 |
| 62 | 46 | 42 | 30 | PTC3 | PTC3 |
| 63 | 47 | 43 | 31 | PTC4 | PTC4 |
| 64 | 48 | 44 | 32 | PTC5 | PTC5 |
| 3 | | | | PTC6 | PTC6 |
| 4 | | | | PTC7 | PTC7 |
| PTD | | | | | |
| 5 | 1 | | | PTD0 | PTD0 |
| 6 | 2 | | | PTD1 | PTD1 |
| 26 | | | | PTD2 | PTD2 |
| 27 | 22 | 20 | | PTD3 | PTD3 |
| 28 | | | | PTD4 | PTD4 |
| 29 | | | | PTD5 | PTD5 |
| 31 | 24 | 22 | | PTD6 | PTD6 |
| 32 | | | | PTD7 | PTD7 |
| PTE | | | | | |
| 33 | | | | PTE0 | PTE0 |
| 34 | | | | PTE1 | PTE1 |
| 38 | | | | PTE3 | PTE2 |

*Table continues on the next page...*

Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 44 | 31 | 27 | | PTE7 | UART0_TX |
| 64 | 48 | 44 | 32 | PTC5 | UART0_TX |
| UART1 | | | | | |
| 11 | 7 | 5 | 5 | PTA4 | UART1_CTS_b |
| 58 | 42 | 38 | | PTF4 | UART1_CTS_b |
| 12 | 8 | 6 | 6 | PTA5 | UART1_RTS_b |
| 57 | 41 | 37 | 29 | PTC2 | UART1_RTS_b |
| 10 | 6 | 4 | 4 | PTA3 | UART1_RX |
| 59 | 43 | 39 | | PTF5 | UART1_RX |
| 9 | 5 | 3 | 3 | PTA2 | UART1_TX |
| 60 | 44 | 40 | | PTF6 | UART1_TX |

# 9 Revision History

The following table summarizes content changes since the previous release of this document.

Table 36. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 4 | 01/2012 | Thermal operating requirements: Changed maximum $T_J$ value from 125°C to 115°C |