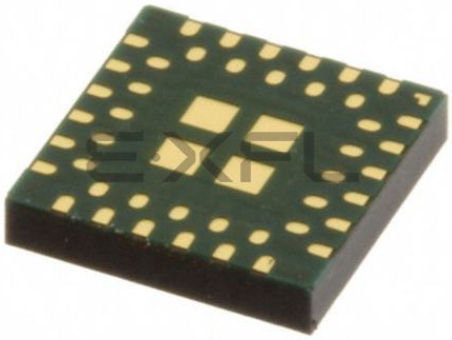

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFLGA Exposed Pad
Supplier Device Package	44-MAPLGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51qu128vhs

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

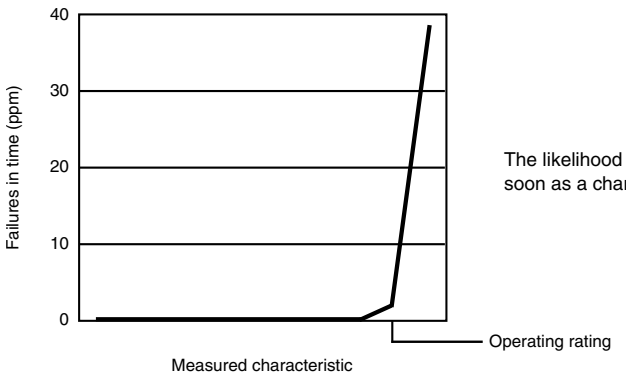
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

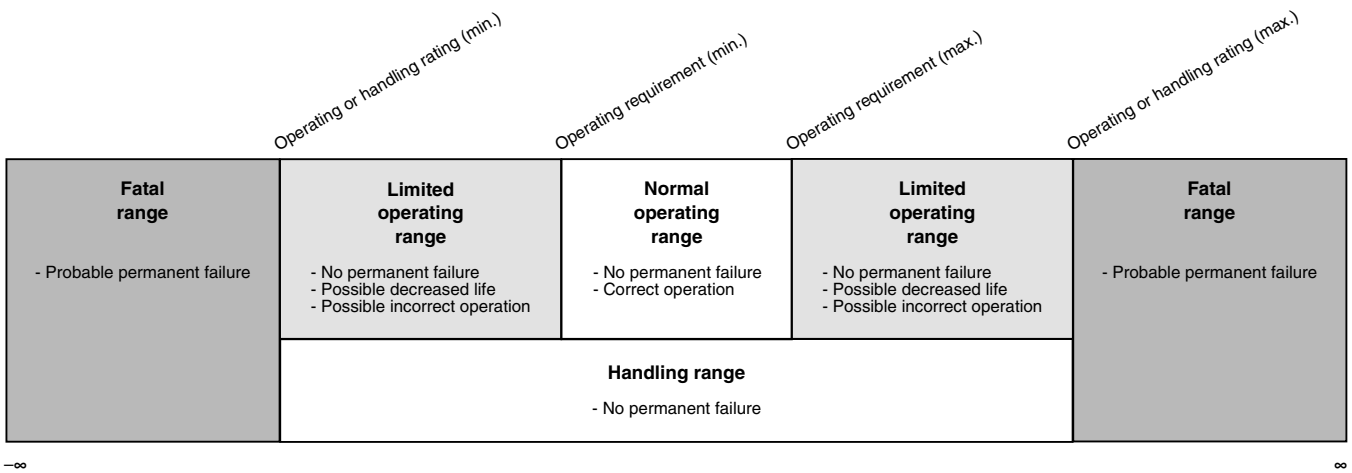
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

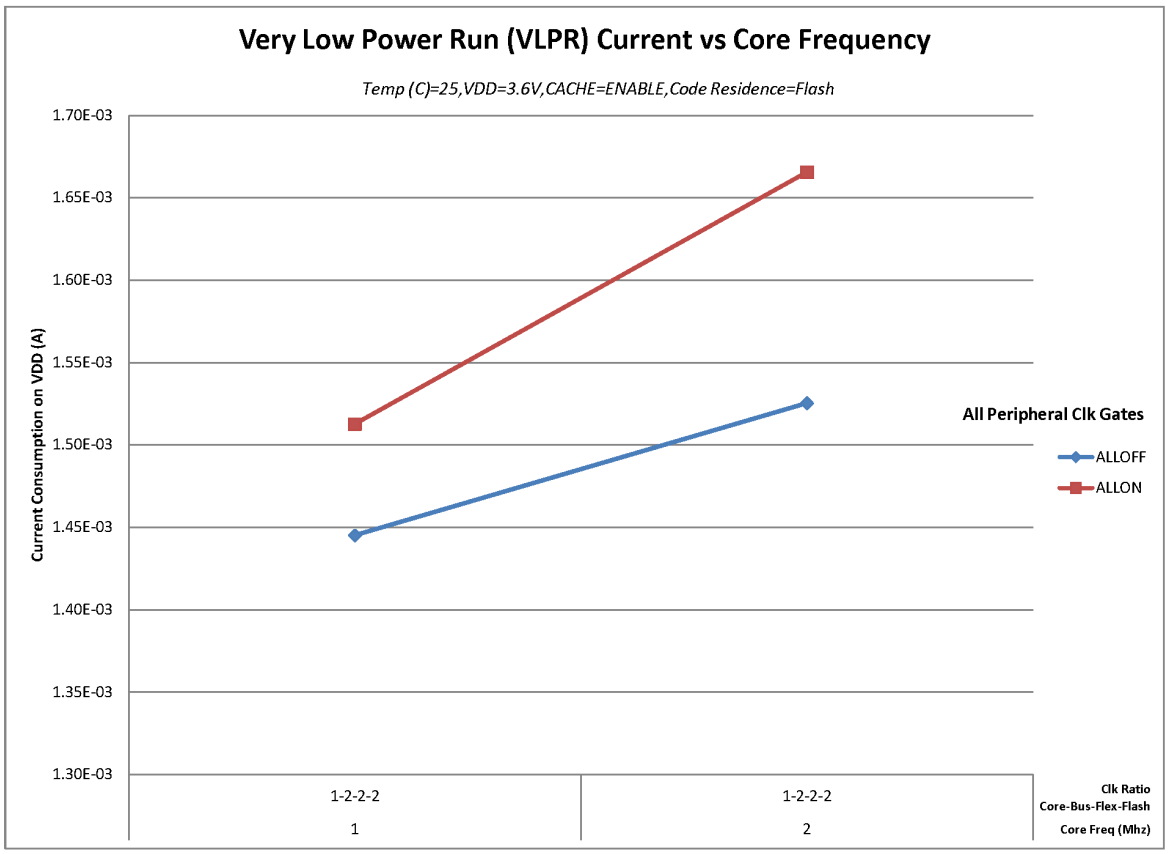


Figure 2. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	19		
V_{RE3}	Radiated emissions voltage, band 3	150–500	17		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16		
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and I^2C signals. The conditions are 50 pf load, V_{DD} = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 9. EGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
	External reset pulse width (digital glitch filter disabled)	100	—	ns
	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

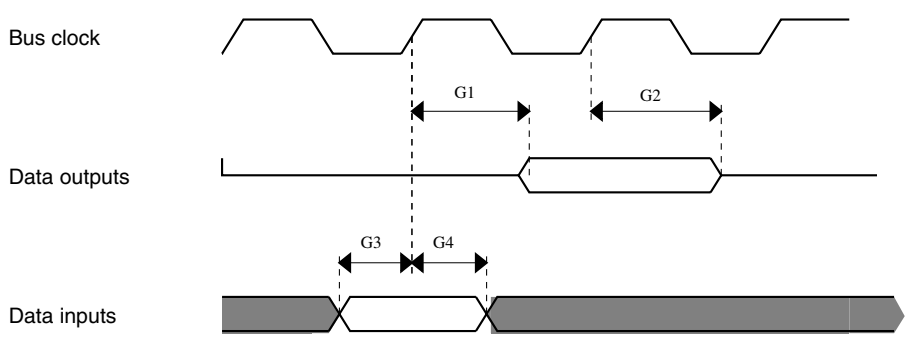


Figure 3. EGPIO timing diagram

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	44 Laminate QFN	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	73	79	108	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	54	55	69	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	61	66	91	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	48	63	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	37	34	44	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	20	31	2.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5.0	4.0	6.0	6.0	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug specifications

Table 12. Background debug mode (BDM) timing

Number	Symbol	Description	Min.	Max.	Unit
1	t_{MSSU}	BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM	500	—	ns
2	t_{MSH}	BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1]	100	—	µs

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 10	—	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 1.0	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	3.3	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	1350 600	— —	ps ps	8
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write\_efficiency} \times n_{\text{nvmcycd}}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance

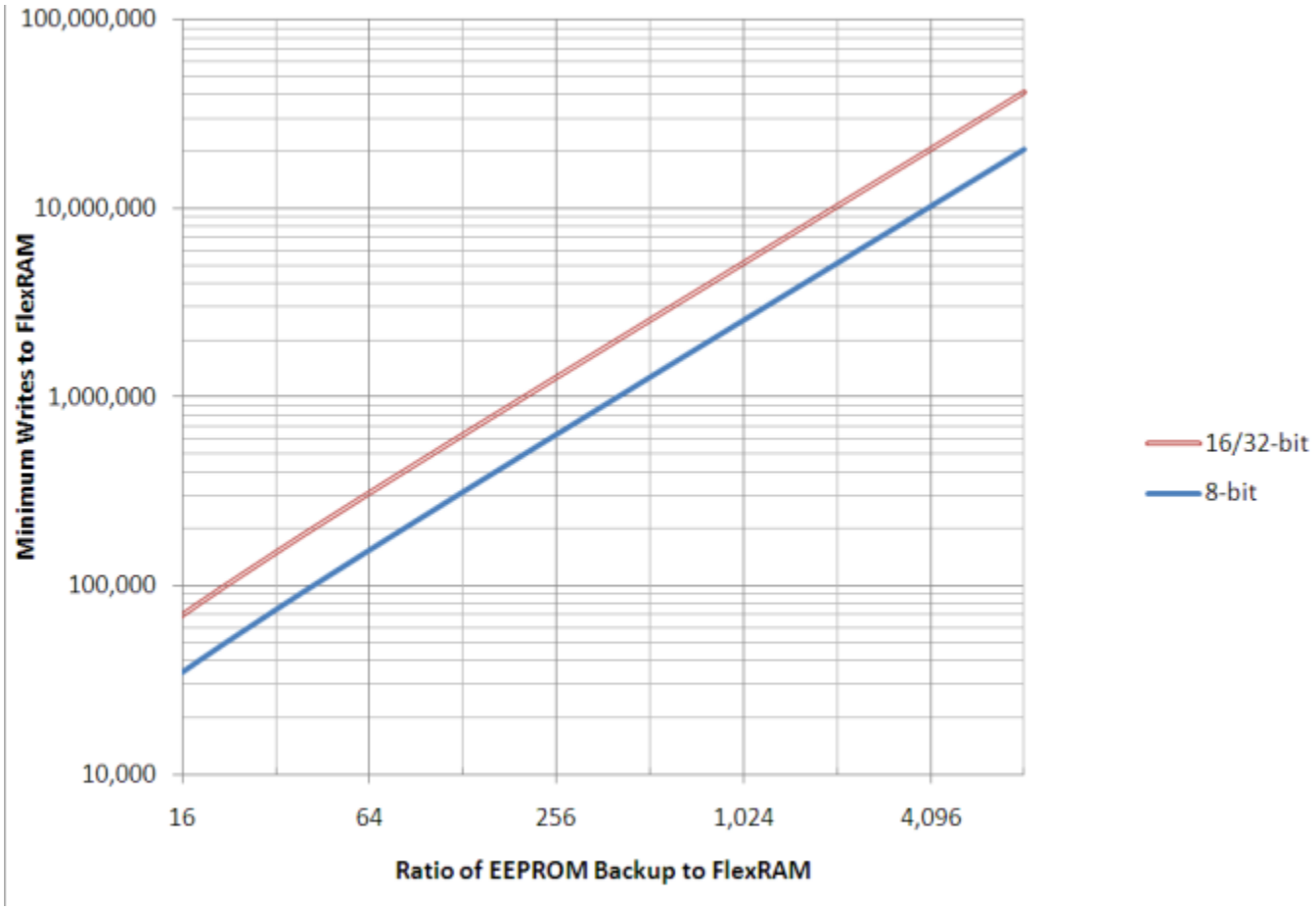


Figure 5. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

All timing is shown with respect to a maximum pin load of 50 pF and input signal transitions of 3 ns.

Table 21. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	15	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	0.0	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	15	—	ns

Table continues on the next page...

Table 22. Flexbus switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB2	Address, data, and control output valid	—	20	ns	1
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	20	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	10	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_CS}}n$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0].

Note

The following diagrams refer to signal names that may not be included on your particular device. Ignore these extraneous signals.

Also, ignore the AA=0 portions of the diagrams because this setting is not supported in the Mini-FlexBus.

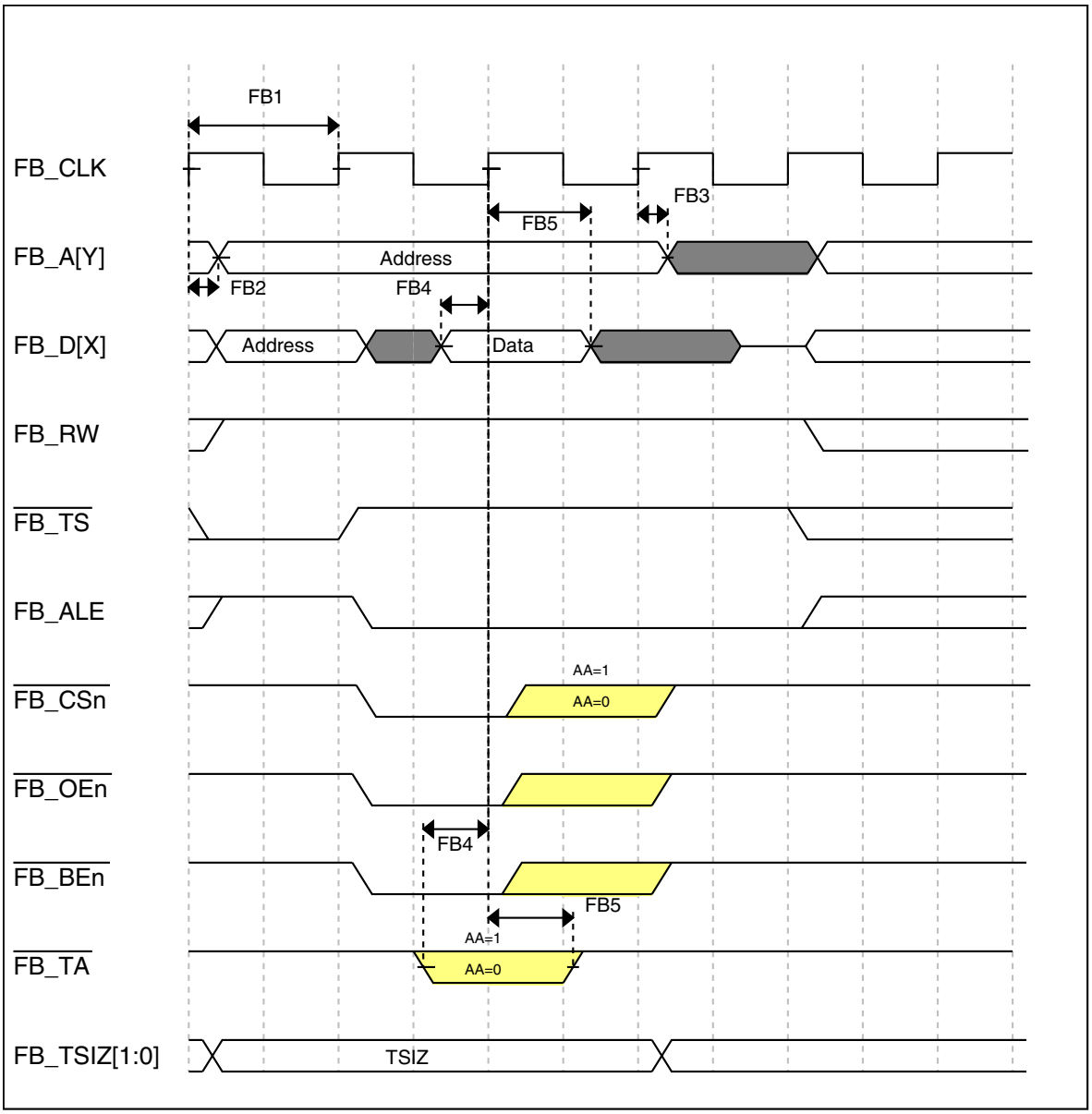


Figure 7. Mini-FlexBus read timing diagram

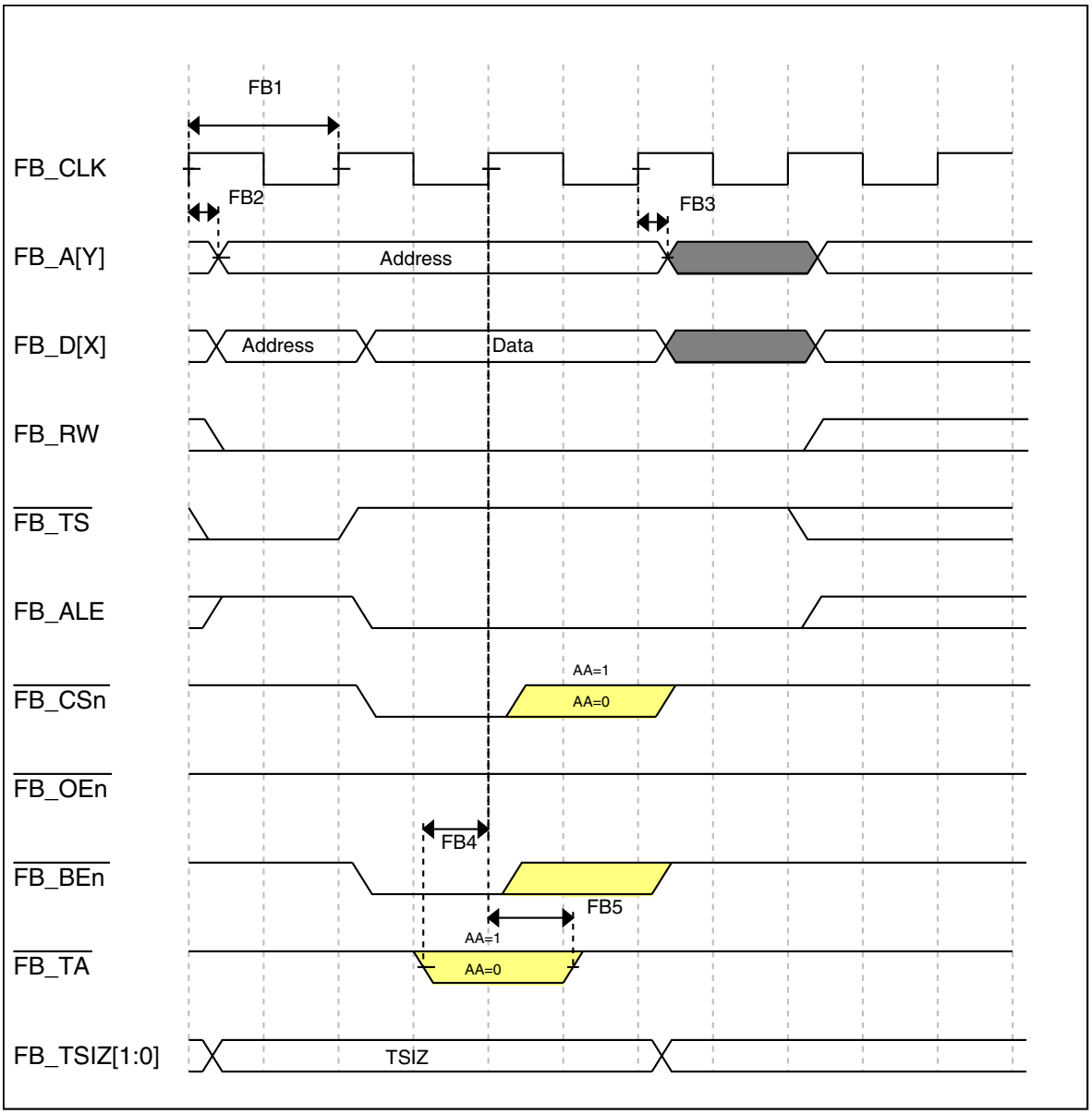


Figure 8. Mini-FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

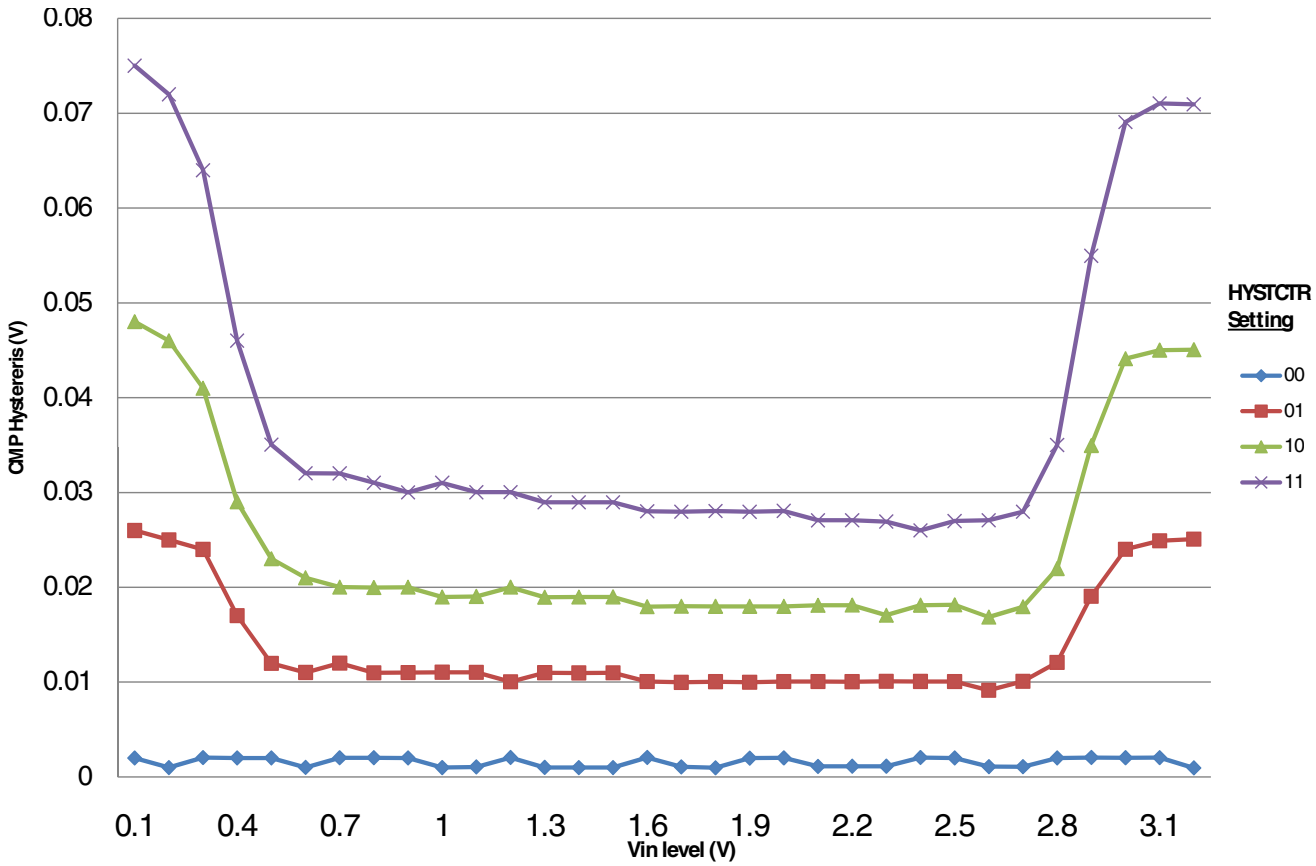


Figure 10. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

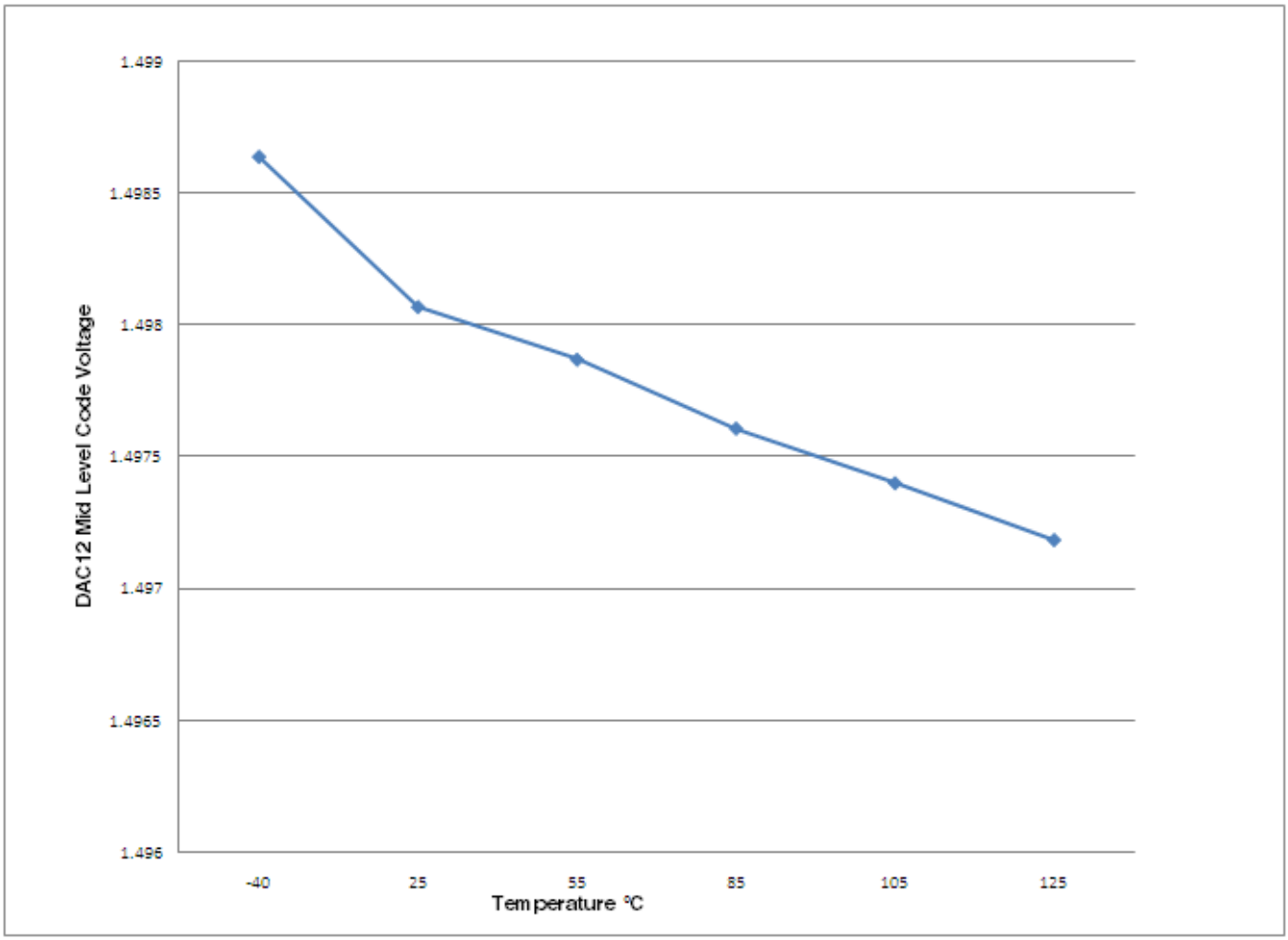


Figure 13. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

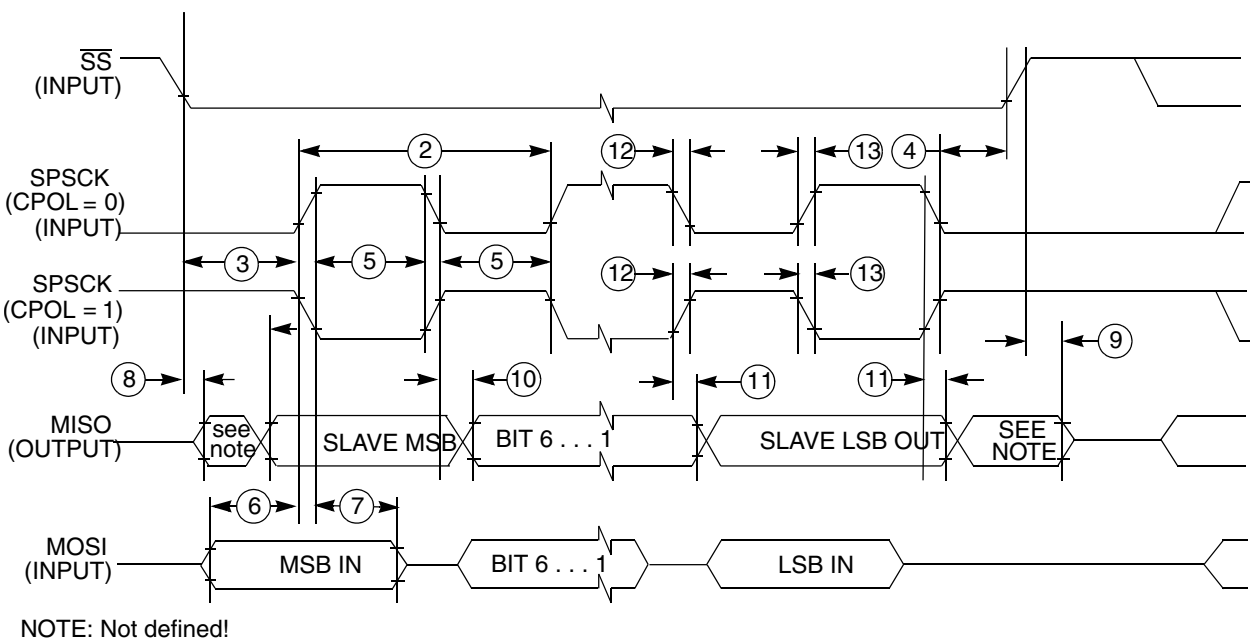
Table 28. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

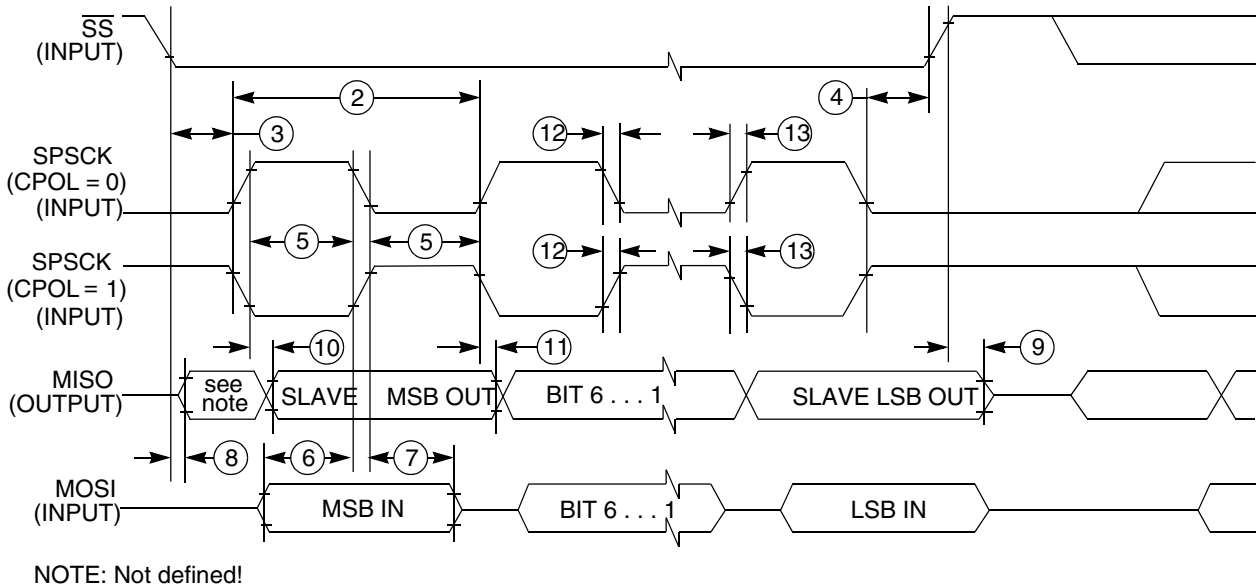
Table 33. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedanc e state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedanc e state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 16. SPI slave mode timing (CPHA=0)



NOTE: Not defined!

Figure 17. SPI slave mode timing (CPHA=1)

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 34. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	5.5	14	MHz	2
f_{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C_{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V_{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I_{REF}	Reference oscillator current source base current • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 5
I_{ELE}	Electrode oscillator current source base current • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	%	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	%	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	%	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10

Table continues on the next page...

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
24	20	18	—	VDD	VDD								
25	21	19	15	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTA6		LPTMR_ALT1	FTM_FLT1	FBa_D7	FBa_AD17		
26	—	—	—	ADC0_SE9/ TSI0_CH1	ADC0_SE9/ TSI0_CH1	PTD2	FTM0_QD_PHA	RGPIO10	FTM0_CH0				
27	22	20	—	ADC0_SE10/TSI0_CH2	ADC0_SE10/TSI0_CH2	PTD3	FTM0_QD_PHB	RGPIO11	FTM0_CH1	FBa_D6	FBa_AD0		
28	—	—	—	ADC0_SE11/TSI0_CH3	ADC0_SE11/TSI0_CH3	PTD4		RGPIO12			FBa_D7		
29	—	—	—	ADC0_SE12/TSI0_CH4	ADC0_SE12/TSI0_CH4	PTD5		RGPIO13			FBa_D6		
30	23	21	16	ADC0_SE13/TSI0_CH5	ADC0_SE13/TSI0_CH5	PTA7	UART0_TX		FTM0_QD_PHA		FBa_D5		
31	24	22	—	ADC0_SE14/TSI0_CH6	ADC0_SE14/TSI0_CH6	PTD6	UART0_RX	RGPIO14			FBa_D4		
32	—	—	—	ADC0_SE15/TSI0_CH7	ADC0_SE15/TSI0_CH7	PTD7	UART0_CTS_b	I2C3_SCL	RGPIO15		FBa_D3		
33	—	—	—	TSI0_CH8	TSI0_CH8	PTE0	UART0_RTS_b	I2C3_SDA			FBa_D2		
34	—	—	—	TSI0_CH9	TSI0_CH9	PTE1	SPI0_SS		FTM_FLT0		FBa_D1		
35	25	23	17	IRQ/ EZP_MS_b	Disabled	PTB0		I2C0_SCL		IRQ/ EZP_MS_b			EZP_CS_b
36	26	24	18	TSI0_CH10	TSI0_CH10	PTB1	SPI0_SCLK	I2C0_SDA	FTM_FLT2	LPTMR_ALT2	FTM0_QD_PHB	FB_CLKOUT	
37	—	—	—	TSI0_CH11	TSI0_CH11	PTE2		I2C3_SCL			FBa_D0		
38	—	—	—	ADC0_SE16/ TSI0_CH12	ADC0_SE16/ TSI0_CH12	PTE3	SPI0_MOSI	I2C3_SDA			FBa_OE_b		
39	27	25	19	ADC0_SE17/ TSI0_CH13	ADC0_SE17/ TSI0_CH13	PTB2	SPI0_MISO				FBa_CS0_b		
40	28	26	20	ADC0_SE18/ TSI0_CH14	ADC0_SE18/ TSI0_CH14	PTB3	SPI0_MOSI			FBa_CS1_b	FBa_ALE		
41	29	—	—	ADC0_SE19/ TSI0_CH15	ADC0_SE19/ TSI0_CH15	PTE4	UART0_RTS_b	LPTMR_ALT3	SPI1_SS		FBa_AD1		
42	30	—	—	ADC0_SE20	ADC0_SE20	PTE5	UART0_CTS_b	I2C1_SCL	SPI1_SCLK		FBa_AD2		
43	—	—	—	ADC0_SE21	ADC0_SE21	PTE6	UART0_RX	I2C1_SDA	SPI1_MISO		FBa_AD3		
44	31	27	—	ADC0_SE22	ADC0_SE22	PTE7	UART0_TX	PDB0_EXTRG	SPI1_MOSI	FBa_RW_b	FBa_AD4		
45	32	28	21	BKGD/MS	Disabled	PTB4	BKGD/MS						
46	33	29	22	XTAL2	XTAL2	PTB5							
47	34	30	23	EXTAL2	EXTAL2	PTB6							
48	35	31	24	VDD	VDD								

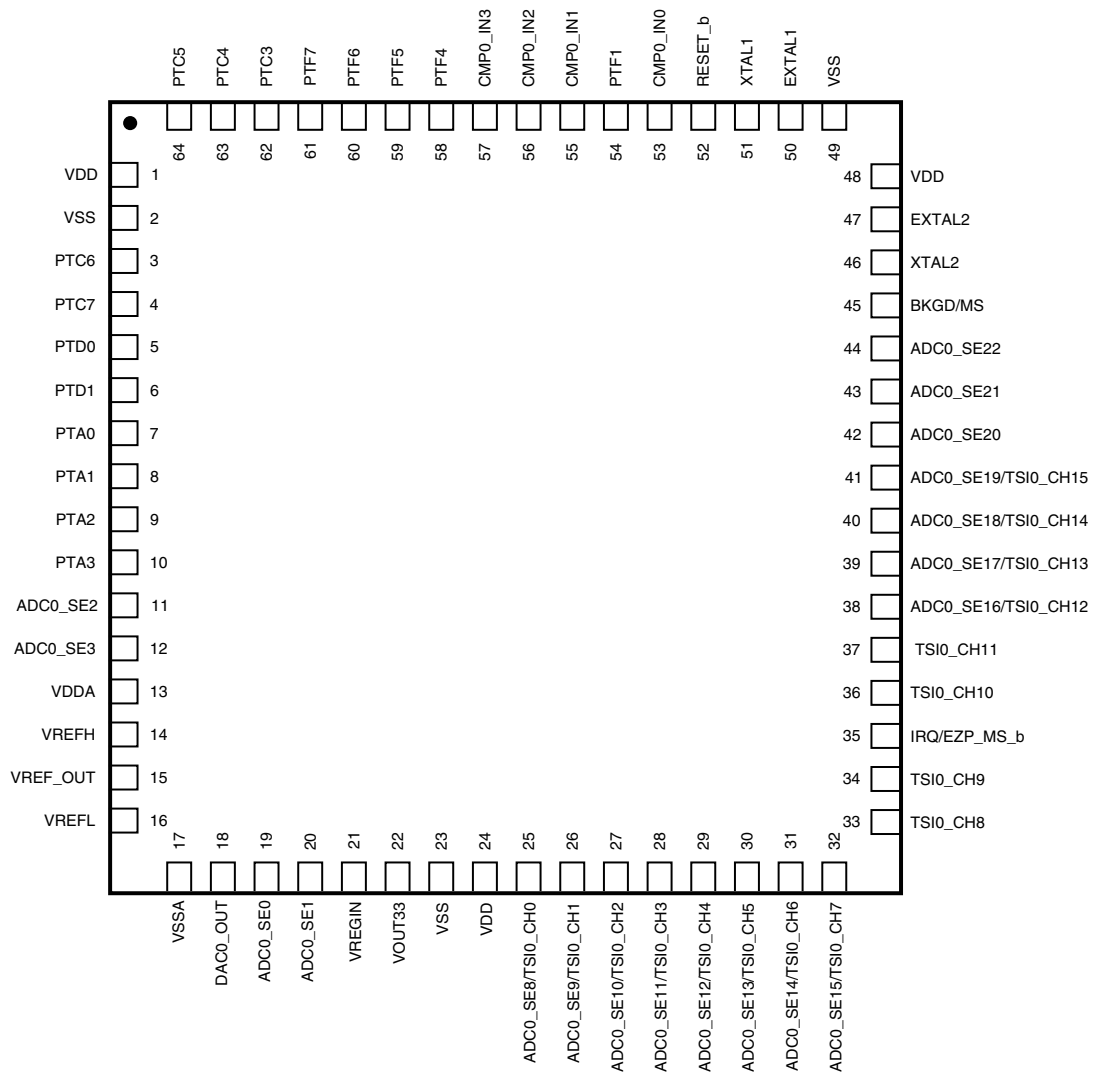


Figure 18. 64-pin LQFP

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
63	47	43	31	PTC4	PDB0_EXTRG
FTM0					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2 / FTM0_QD_PHB
26				PTD2	FTM0_CH0/ FTM0_QD_PHA
27	22	20		PTD3	FTM0_CH1 / FTM0_QD_PHB
30	23	21	16	PTA7	FTM0_QD_PHA
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
FTM1					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2
7	3	1	1	PTA0	FTM1_CH0
8	4	2	2	PTA1	FTM1_CH1
9	5	3	3	PTA2	FTM1_CH2
10	6	4	4	PTA3	FTM1_CH3
11	7	5	5	PTA4	FTM1_CH4
12	8	6	6	PTA5	FTM1_CH5
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
MTIM					
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
Mini-FlexBus					
36	26	24	18	PTB1	FB_CLKOUT
27	22	20		PTD3	FBa_AD0
41	29			PTE4	FBa_AD1
42	30			PTE5	FBa_AD2
43				PTE6	FBa_AD3
44	31	27		PTE7	FBa_AD4
53				PTF0	FBa_AD5

Table continues on the next page...