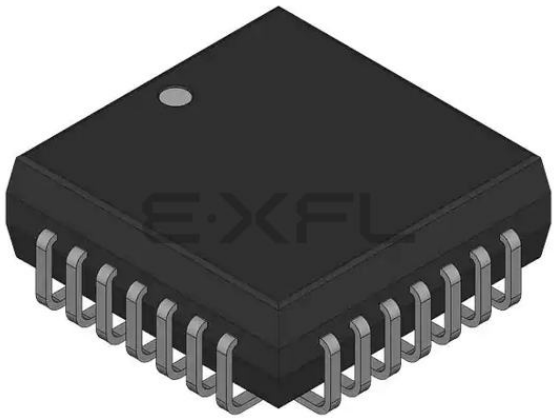

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=pcf51qu64vlf

Field	Description	Values
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB
T	Temperature range, ambient (°C)	V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • HS = 44 Laminate QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)

1. All parts also have FlexNVM, FlexRAM, and RAM.

2.4 Example

This is an example part number:

MCF51QU128VLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

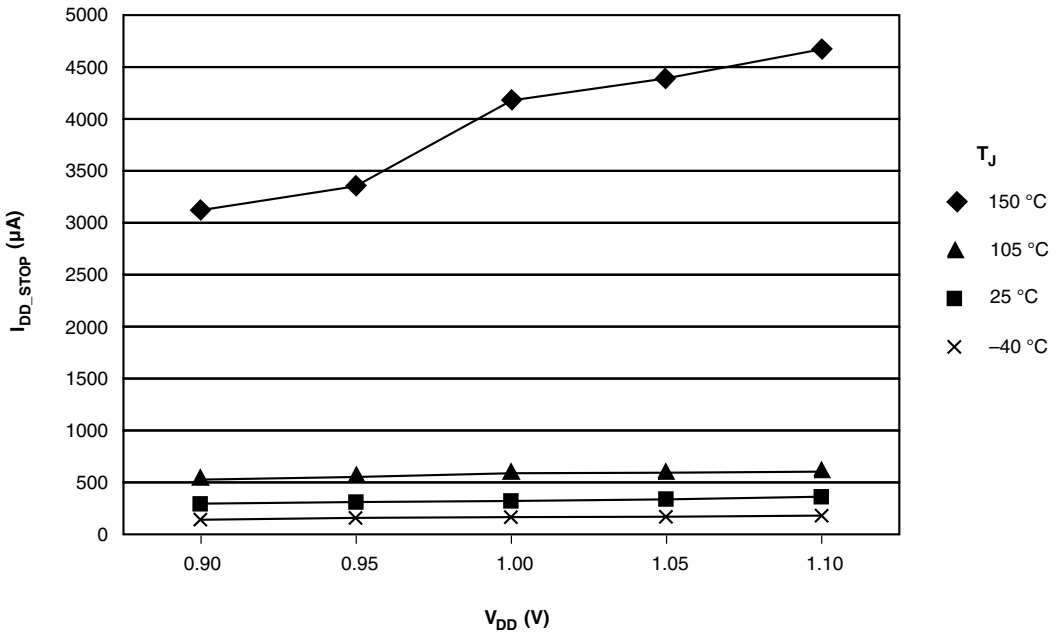
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2 Nonswitching electrical specifications

5.2.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	0.7 × V_{DD}	—	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	0.75 × V_{DD}	—	V	
V_{IL}	Input low voltage				2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.35 × V_{DD}	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	
I_{IC}	DC injection current — single pin				3
	• V_{IN} > V_{DD}	0	2	mA	
	• V_{IN} < V_{SS}	0	–0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				3
	• V_{IN} > V_{DD}	0	25	mA	
	• V_{IN} < V_{SS}	0	–5	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. The device always interprets an input as a 1 when the input is greater than or equal to V_{IH} (min.) and less than or equal to V_{IH} (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to V_{IL} (max.) and greater than or equal to V_{IL} (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (VIn > VDD) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

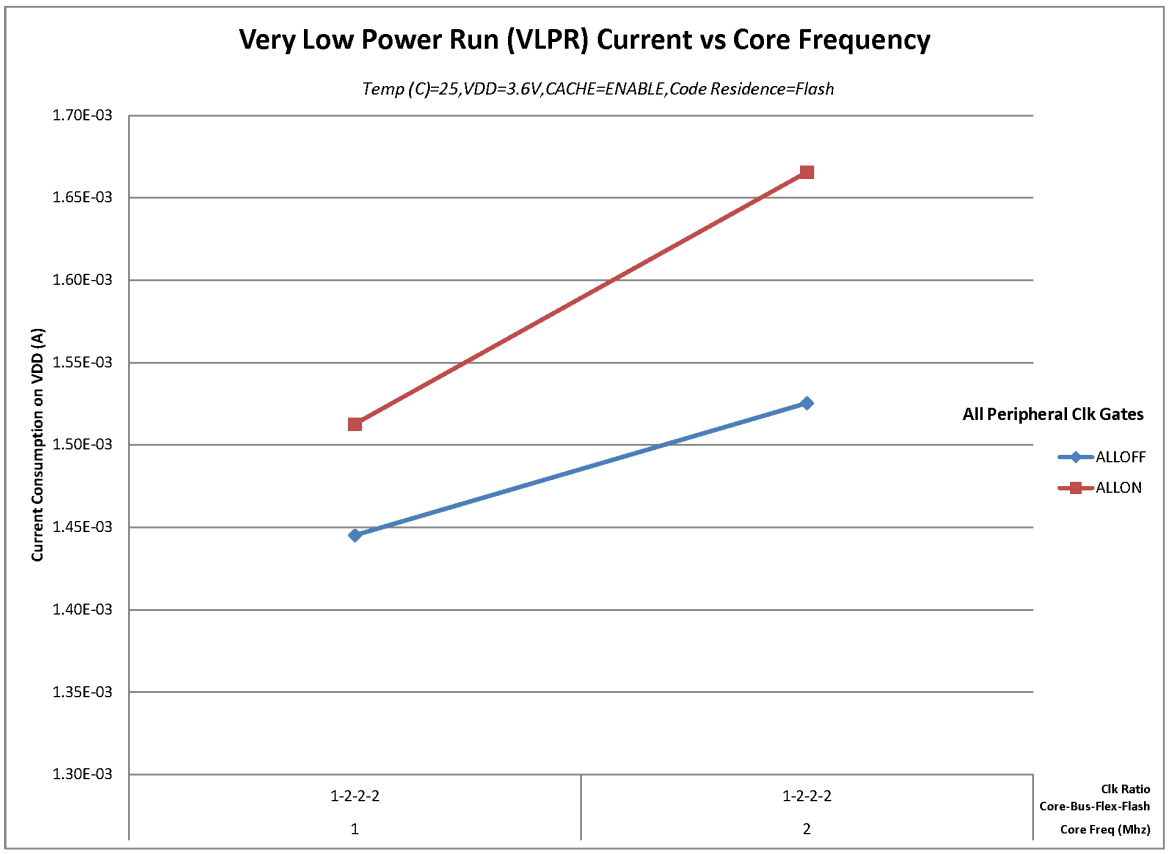


Figure 2. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	19		
V_{RE3}	Radiated emissions voltage, band 3	150–500	17		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16		
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 10	—	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 1.0	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	3.3	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 18. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFL) current and power specfications

Table 19. Flash (FTFL) current and power specfications

Symbol	Description	Typ.	Unit
I_{DD_PGM}	Worst case programming current in program flash	10	mA

6.4.1.4 Reliability specifications

Table 20. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	2
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	10	100	—	years	2
$t_{nvmretp100}$	Data retention after up to 100 cycles	15	100	—	years	2
$n_{nvmcycp}$	Cycling endurance	10 K	35 K	—	cycles	3
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	2
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	10	100	—	years	2
$t_{nvmretd100}$	Data retention after up to 100 cycles	15	100	—	years	2
$n_{nvmcycd}$	Cycling endurance	10 K	35 K	—	cycles	3
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	2
$t_{nvmretee10}$	Data retention up to 10% of write endurance	10	100	—	years	2
$t_{nvmretee1}$	Data retention up to 1% of write endurance	15	100	—	years	2
	Write endurance					4
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on T_{javg} = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
4. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

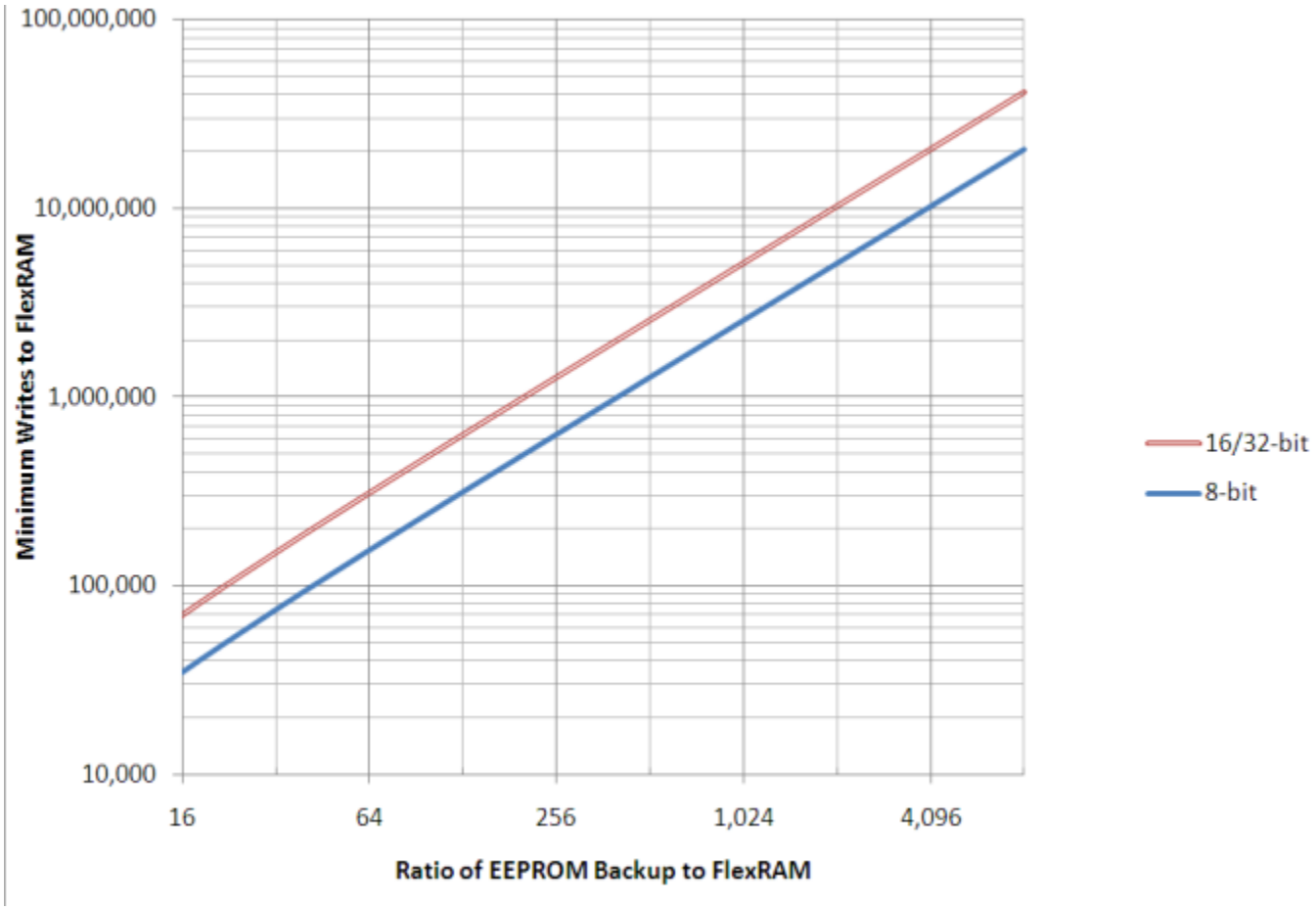


Figure 5. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

All timing is shown with respect to a maximum pin load of 50 pF and input signal transitions of 3 ns.

Table 21. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	15	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	0.0	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	15	—	ns

Table continues on the next page...

Table 22. Flexbus switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB2	Address, data, and control output valid	—	20	ns	1
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	20	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	10	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_CS}}n$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0].

Note

The following diagrams refer to signal names that may not be included on your particular device. Ignore these extraneous signals.

Also, ignore the AA=0 portions of the diagrams because this setting is not supported in the Mini-FlexBus.

5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

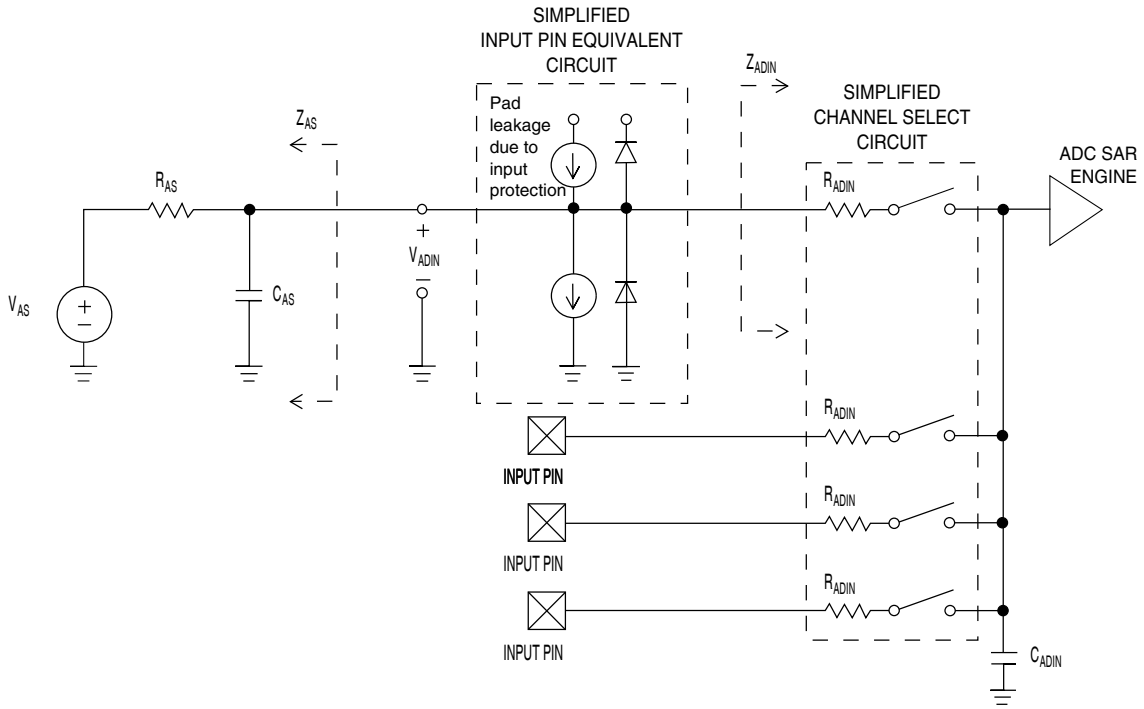


Figure 9. ADC input impedance equivalency diagram

6.6.1.2 12-bit ADC electrical characteristics

Table 24. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5

Table continues on the next page...

Table 25. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

6.8 Communication interfaces

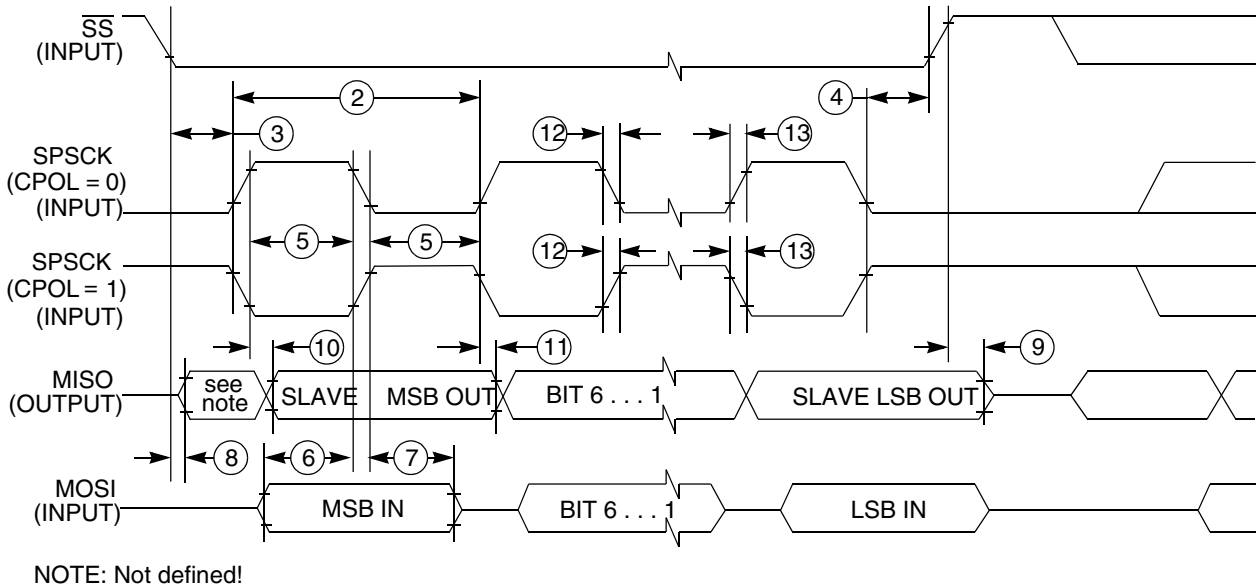
6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

Table 32. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{BUS}/2048$	$f_{BUS}/2$	Hz	f_{BUS} is the bus clock as defined in Table 8.
2	t_{SPSCK}	SPSCK period	2 x t_{BUS}	2048 x t_{BUS}	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	1024 x t_{BUS}	ns	—
6	t_{SU}	Data setup time (inputs)	21	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 17. SPI slave mode timing (CPHA=1)

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 34. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	5.5	14	MHz	2
f_{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C_{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V_{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I_{REF}	Reference oscillator current source base current • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 5
I_{ELE}	Electrode oscillator current source base current • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	%	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	%	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	%	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10

Table continues on the next page...

Table 34. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	11
I_{TSI_RUN}	Current added in run mode	—	55	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	µA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
7. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
10. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: Iext = 5 µA, EXTCHRG = 4, PS = 128, NSCN = 2, I_{ref} = 16 µA, REFCHRG = 15, C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I_{ext} = 1 µA, EXTCHRG = 0, PS = 128, NSCN = 32, I_{ref} = 32 µA, REFCHRG = 31, C_{ref}= 0.5 pF
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ARE10566D
44-pin Laminate QFN	98ASA00239D
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
49	36	32	25	VSS	VSS								
50	37	33	26	EXTAL1	EXTAL1	PTB7		I2C1_SDA	TMR_CLKIN1				
51	38	34	27	XTAL1	XTAL1	PTC0		I2C1_SCL	TMR_CLKIN0	RGPIO0			
52	39	35	28	RESET_b	Disabled	PTC1	RESET_b						
53	—	—	—	CMP0_IN0	CMP0_IN0	PTF0	SPI0_SS				FBa_AD5		
54	—	—	—	Disabled	Disabled	PTF1	SPI0_SCLK			CMP0_OUT	FBa_AD6		
55	—	—	—	CMP0_IN1	CMP0_IN1	PTF2	SPI0_MISO				FBa_AD7		
56	40	36	—	CMP0_IN2	CMP0_IN2	PTF3	SPI0_MOSI			RGPIO1	FBa_AD8		
57	41	37	29	CMP0_IN3	CMP0_IN3	PTC2	UART1_RTS_b	SPI1_SS		RGPIO2	FBa_AD18		
58	42	38	—	Disabled	Disabled	PTF4	UART1_CTS_b	SPI1_SCLK		FBa_D3	FBa_AD19		
59	43	39	—	Disabled	Disabled	PTF5	UART1_RX	SPI1_MISO		FBa_D2	FBa_RW_b		
60	44	40	—	Disabled	Disabled	PTF6	UART1_TX	SPI1_MOSI		FBa_D1	FBa_AD9		
61	45	41	—	Disabled	Disabled	PTF7	UART0_RTS_b		SPI0_SS	FBa_D0	FBa_AD10		
62	46	42	30	Disabled	Disabled	PTC3	UART0_CTS_b	RGPIO3	SPI0_SCLK	CLKOUT			
63	47	43	31	Disabled	Disabled	PTC4	UART0_RX	RGPIO4	SPI0_MISO	PDB0_EXTRG			
64	48	44	32	Disabled	Disabled	PTC5	UART0_TX	RGPIO5	SPI0_MOSI	CMT_IRO			

8.2 Pinout diagrams

The following diagrams show pinouts for the 64-pin, 48-pin, 44-pin, and 32-pin packages. These diagrams are representations for ease of reference. See the package drawings for mechanical details.

For each pin, the diagrams show the default function or (when disabled is the default) the ALT1 signal for a GPIO function. However, many signals may be multiplexed onto a single pin.

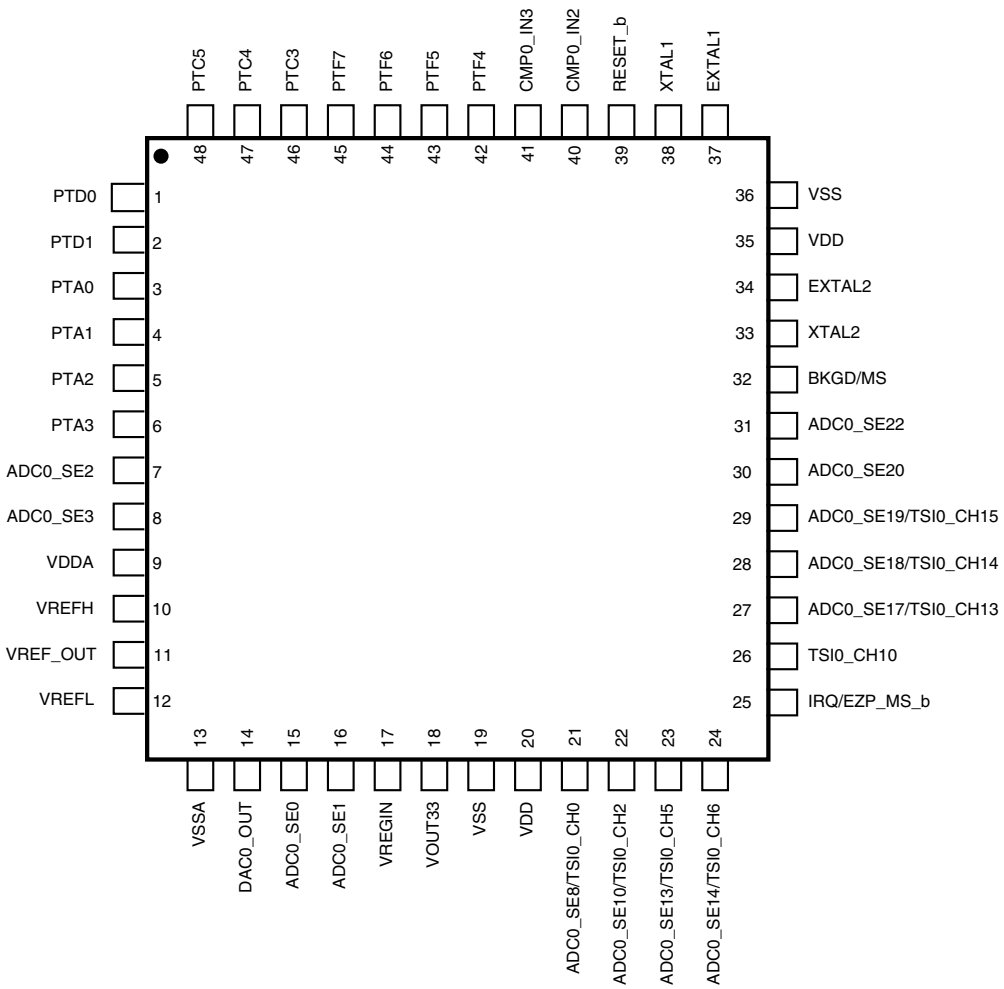


Figure 19. 48-pin LQFP

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
39	27	25	19	PTB2	PTE3
41	29			PTE4	PTE4
42	30			PTE5	PTE5
43				PTE6	PTE6
44	31	27		PTE7	PTE7
PTF					
53				PTF0	PTF0
54				PTF1	PTF1
55				PTF2	PTF2
56	40	36		PTF3	PTF3
58	42	38		PTF4	PTF4
59	43	39		PTF5	PTF5
60	44	40		PTF6	PTF6
61	45	41		PTF7	PTF7
5 V VREG					
22	18	16	13		VOUT33
21	17	15	12		VREGIN
ADC0					
11	7	5	5	PTA4	ADC0_SE2
12	8	6	6	PTA5	ADC0_SE3
25	21	19	15	PTA6	ADC0_SE8
26				PTD2	ADC0_SE9
27	22	20		PTD3	ADC0_SE10
28				PTD4	ADC0_SE11
29				PTD5	ADC0_SE12
30	23	21	16	PTA7	ADC0_SE13
31	24	22		PTD6	ADC0_SE14
32				PTD7	ADC0_SE15
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17
40	28	26	20	PTB3	ADC0_SE18
41	29			PTE4	ADC0_SE19
42	30			PTE5	ADC0_SE20
43				PTE6	ADC0_SE21
44	31	27		PTE7	ADC0_SE22

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
27	22	20		PTD3	FBa_D6
25	21	19	15	PTA6	FBa_D7
44	31	27		PTE7	FBa_RW_b
I2C0 and I2C1					
3				PTC6	I2C0_SCL
35	25	23	17	PTB0	I2C0_SCL
4				PTC7	I2C0_SDA
36	26	24	18	PTB1	I2C0_SDA
6	2			PTD1	I2C1_SCL
42	30			PTE5	I2C1_SCL
51	38	34	27	PTC0	I2C1_SCL
5	1			PTD0	I2C1_SDA
43				PTE6	I2C1_SDA
50	37	33	26	PTB7	I2C1_SDA
I2C2 and I2C3					
7	3	1	1	PTA0	I2C2_SCL
11	7	5	5	PTA4	I2C2_SCL
8	4	2	2	PTA1	I2C2_SDA
12	8	6	6	PTA5	I2C2_SDA
32				PTD7	I2C3_SCL
37				PTE2	I2C3_SCL
33				PTE0	I2C3_SDA
38				PTE3	I2C3_SDA
SPI0					
39	27	25	19	PTB2	SPI0_MISO
55				PTF2	SPI0_MISO
63	47	43	31	PTC4	SPI0_MISO
38				PTE3	SPI0_MOSI
40	28	26	20	PTB3	SPI0_MOSI
56	40	36		PTF3	SPI0_MOSI
64	48	44	32	PTC5	SPI0_MOSI
36	26	24	18	PTB1	SPI0_SCLK
54				PTF1	SPI0_SCLK
62	46	42	30	PTC3	SPI0_SCLK
7	3	1	1	PTA0	SPI0_SS

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
44	31	27		PTE7	UART0_TX
64	48	44	32	PTC5	UART0_TX
UART1					
11	7	5	5	PTA4	UART1_CTS_b
58	42	38		PTF4	UART1_CTS_b
12	8	6	6	PTA5	UART1_RTS_b
57	41	37	29	PTC2	UART1_RTS_b
10	6	4	4	PTA3	UART1_RX
59	43	39		PTF5	UART1_RX
9	5	3	3	PTA2	UART1_TX
60	44	40		PTF6	UART1_TX

9 Revision History

The following table summarizes content changes since the previous release of this document.

Table 36. Revision History

Rev. No.	Date	Substantial Changes
4	01/2012	Thermal operating requirements: Changed maximum T_J value from 125°C to 115°C