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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-1
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417034af20v

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.2.10 Parity Control Register (PCR)

The parity control register (PCR) is a 16-bit read/write register that selects the parity polarity and space to be parity checked. PCR is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	PEF	PFRC	PEO	PCHK1	PCHK0	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit 15—Parity Error Flag (PEF): When a parity check is carried out, PEF indicates whether a parity error has occurred. 0 indicates that no parity error has occurred; 1 indicates that a parity error has occurred.

Bit 15: PEF	Description
0	No parity error (Initial value) Cleared by reading PEF after it has been set to 1, then writing 0 in PEF
1	Parity error has occurred

Self-Refresh Mode: Some DRAMs have a self-refresh mode (battery back-up mode). This is a type of a standby mode in which the refresh timing and refresh addresses are generated inside the DRAM chip. When the RFSHE and RMODE bits in RCR are both set to 1, the DRAM will enter self-refresh mode when the $\overline{CAS}$ and $\overline{RAS}$ signals are output as shown in figure 8.31. See sections 20.1.3 (3) and 20.2.3 (3), Bus Timing, for details. DRAM self-refresh mode is cleared when the RMODE bit in RCR is cleared to 0 (figure 8.31). The RFSHE bit should be left at 1 when this is done. Some DRAM vendors recommend that after exiting self-refresh mode, all row addresses should be refreshed again. This can be done using the BSC's CBR refresh function to set all row addresses for refresh in software.

To access a DRAM area while in self-refresh mode, first clear the RMODE bit to 0 and exit self-refresh mode.

The chip can be kept in the self-refresh state and shifted to standby mode by setting it to self-refresh mode, setting the standby bit (SBY) in the standby control register (SBYCR) to 1, and then executing a SLEEP instruction.

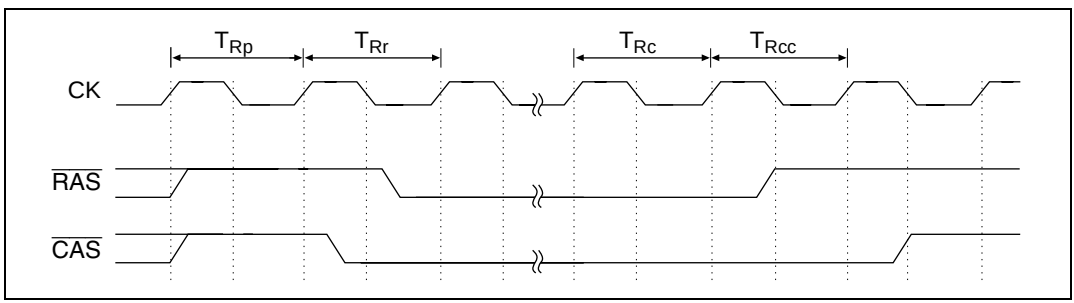


Figure 8.31 Output Timing for Self-Refresh Signal

Refresh Requests and Bus Cycle Requests: When a CAS-before-RAS refresh or self-refresh is requested during bus cycle execution, parallel execution is sometimes possible. Table 8.11 summarizes the operation when refresh and bus cycles are in contention.

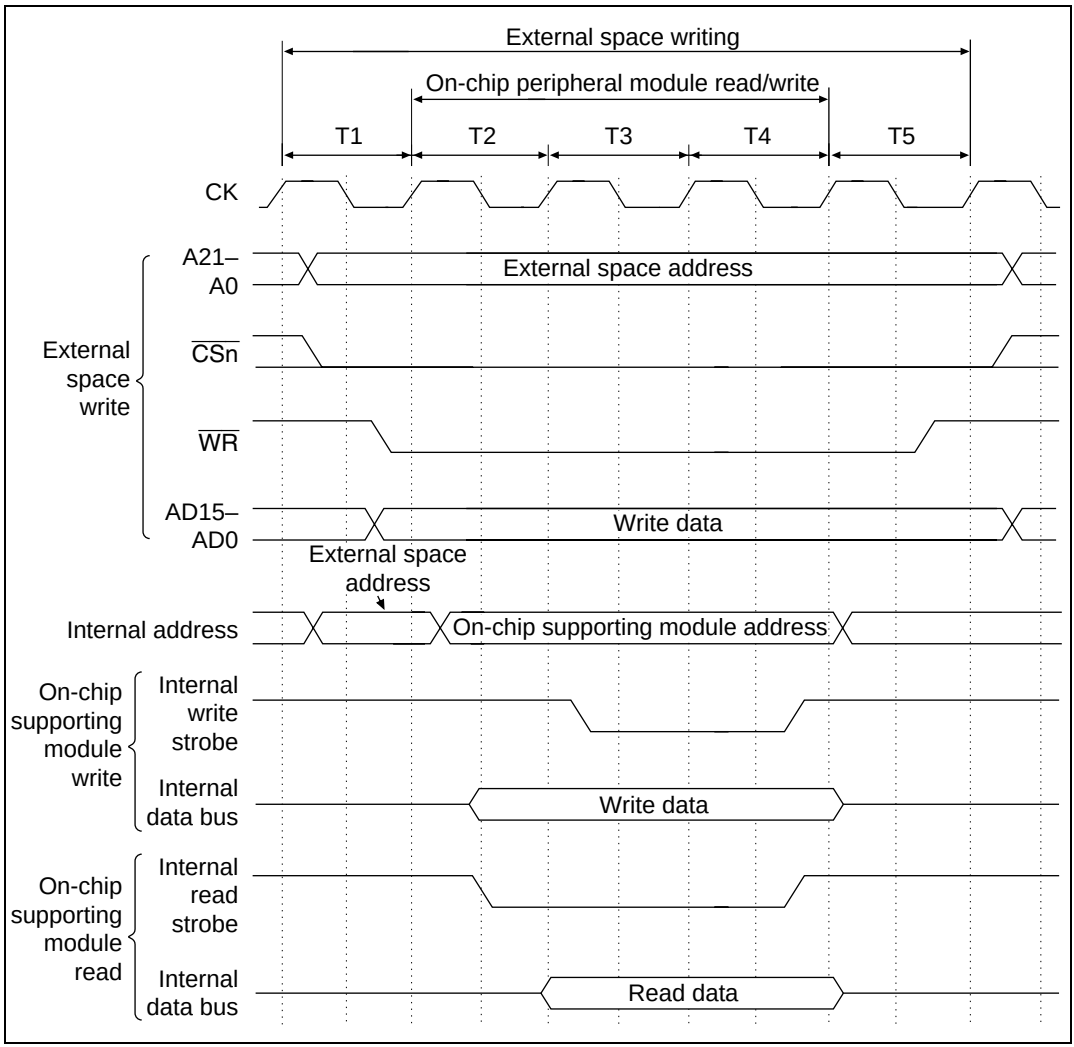


Figure 8.34 Warp Mode Timing (Access to On-Chip Supporting Module and External Write Cycle)

8.9 Wait State Control

The WCR1–WCR3 registers of the BSC can be set to control sampling of the $\overline{\text{WAIT}}$ signal when accessing various areas, and the number of bus cycle states. Table 8.12 shows the number of bus cycle states when accessing various areas.

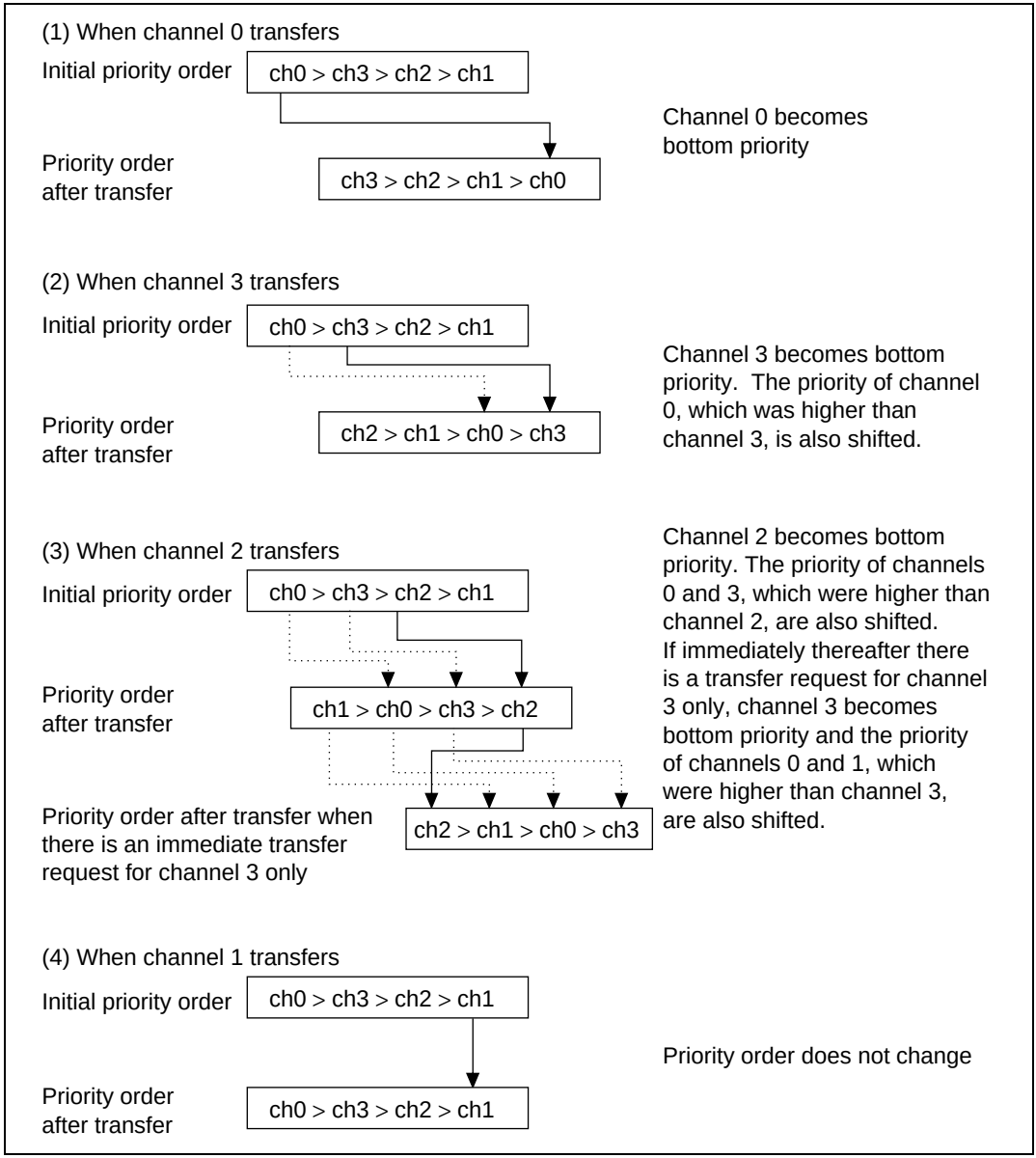


Figure 9.3 Round-Robin Mode

Figure 9.4 shows how the priority order changes when channel 0 and channel 1 transfers are requested simultaneously and a channel 3 transfer is requested during the channel 0 transfer. The DMAC operates as follows:

External-Pin Round-Robin Mode: External-pin round-robin mode switches the priority levels of channel 0 and channel 1, which are the channels that can receive transfer requests from external pins $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$. The priority levels are changed after each (byte or word) transfer on channel 0 or channel 1 is completed. The channel which just finished the transfer rotates to the bottom of the priority order. The priority levels of channels 2 and 3 do not change. The initial priority order after a reset is channel 3 > channel 2 > channel 1 > channel 0.

Figure 9.5 shows how the priority order changes when channel 0 and channel 1 transfers are requested simultaneously and a channel 0 transfer is requested again after both channels finish their transfers. The DMAC operates as follows:

1. Transfer requests are generated simultaneously for channels 1 and 0.
2. Channel 1 has a higher priority, so the channel 1 transfer begins first (channel 0 waits for transfer).
3. When the channel 1 transfer ends, channel 1 becomes the lowest priority.
4. The channel 0 transfer begins.
5. When the channel 0 transfer ends, channel 0 becomes the lowest priority.
6. A channel 0 transfer request occurs again.
7. The channel 0 transfer begins.
8. When the channel 0 transfer ends, the priority order does not change, because channel 0 is already the lowest priority.

Bit	7	6	5	4	3	2	1	0
	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value	*	0	0	0	1	0	0	0
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: * Undefined

Bit 7—Reserved: Bit 7 is read as undefined. The write value should be 0 or 1.

Bits 6–4—I/O Control B2–B0 (IOB2–IOB0): IOB2–IOB0 selects the GRB function.

Bit 6: IOB2	Bit 5: IOB1	Bit 4: IOB0	GRB Function	
0	0	0	GRB is an output compare register	Compare match with pin output disabled (Initial value)
		1		0 output at GRB compare match*[1]
	1	0		1 output at GRB compare match*[1]
		1		Output toggles at GRB compare match (1 output for channel 2 only)*[1] *[2]
1	0	0	GRB is an input capture register	GRB captures rising edge of input
		1		GRB captures falling edge of input
	1	0		GRB captures both edges of input
		1		

Notes: 1. After reset, the value output is 0 until the first compare match occurs.
2. Channel 2 has no compare-match driven toggle output function. If it is set for toggle, 1 is automatically selected as the output.

Bit 3—Reserved: Bit 3 always is read as 1. The write value should always be 1.

Synchronized Operation: Figure 10.27 shows an example of synchronized operation. Channels 0, 1, and 2 are set to synchronized operation and PWM output. Channel 0 is set for a counter clear upon compare match with GRB0. Channels 1 and 2 are set for counter clears by synchronizing clears. Accordingly, their timers are sync preset, then sync cleared by a GRB0 compare match, and then a three-phase PWM waveform is output from the TIOCA0, TIOCA1, and TIOCA2 pins. See section 10.4.4, PWM Mode, for details on PWM mode.

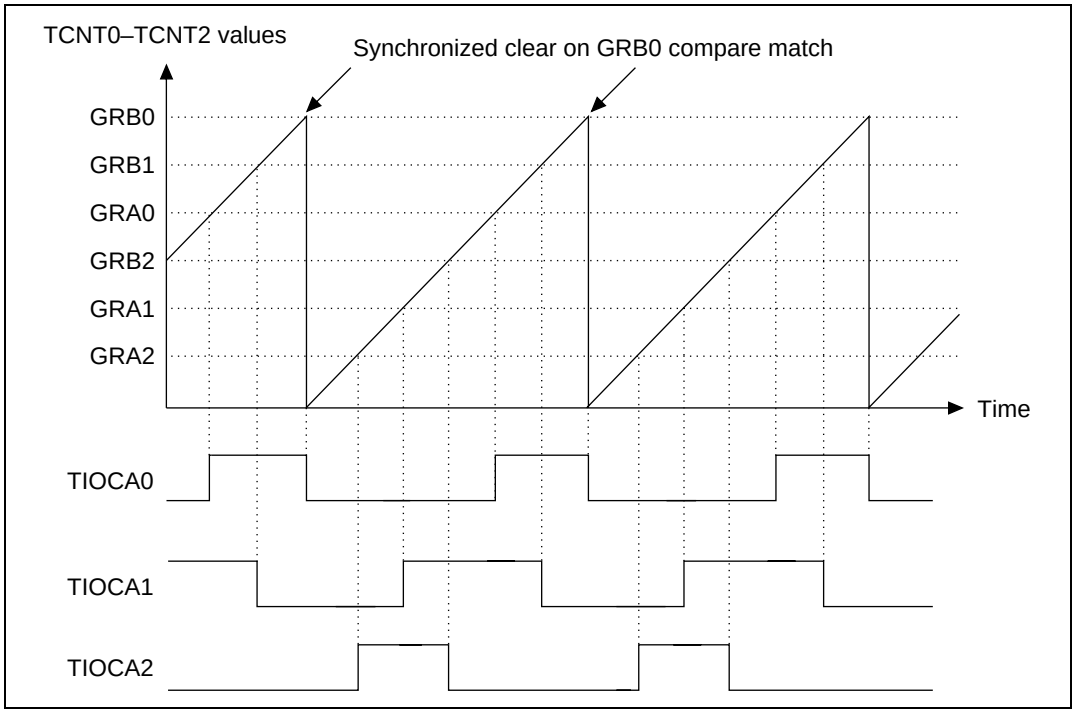


Figure 10.27 Example of Synchronized Operation

Bit 2—Group 2 Non-Overlap Mode (G2NOV): G2NOV selects ordinary or non-overlap mode for TPC output group 2 (TP11–TP8).

Bit 2: G2NOV	Description
0	TPC output group 2 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 2 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

Bit 1—Group 1 Non-Overlap Mode (G1NOV): G1NOV selects ordinary or non-overlap mode for TPC output group 1 (TP7–TP4).

Bit 1: G1NOV	Description
0	TPC output group 1 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 1 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

Bit 0—Group 0 Non-Overlap Mode (G0NOV): G0NOV selects ordinary or non-overlap mode for TPC output group 0 (TP3–TP0).

Bit 0: G0NOV	Description
0	TPC output group 0 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 0 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

11.3 Operation

11.3.1 Overview

When corresponding bits in the PBCR1, PBCR2, NDERA, and NDERB registers are set to 1, TPC output is enabled and the PBDR data register values are output. After that, when the compare match event selected by TPCR occurs, the next data register contents (NDRA and NDRB) are transferred to PBDR and output values are updated. Figure 11.2 illustrates the TPC output operation.

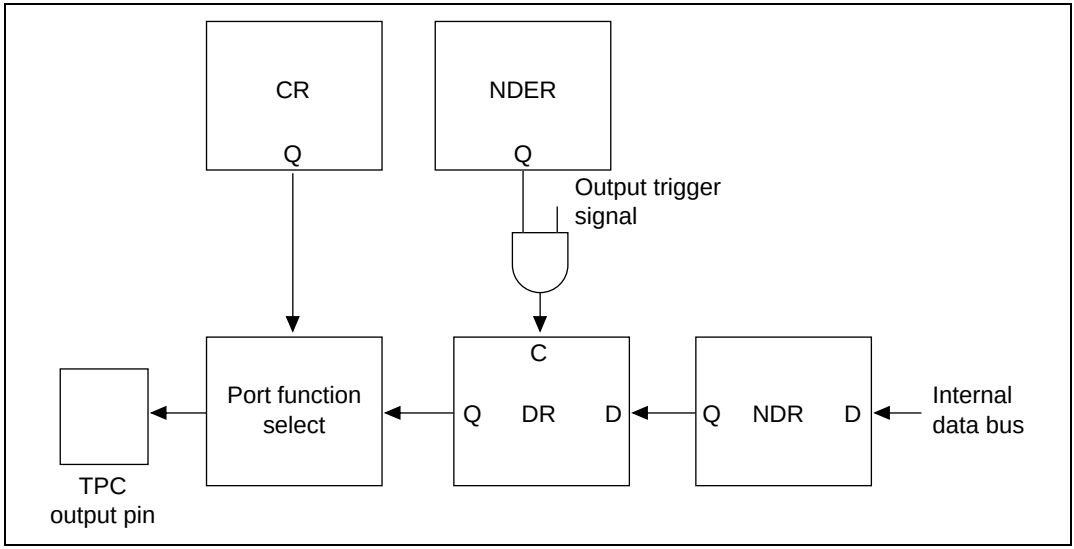


Figure 11.2 TPC Output Operation

If new data is written in next data registers A and B before the next compare match occurs, a maximum 16 bits of data can be output at each successive compare match. See section 11.3.4, TPC Output Non-Overlap Operation, for details on non-overlap operation.

11.3.2 Output Timing

If TPC output is enabled, next data register (NDRA/NDRB) contents are transferred to the data register (PBDR) and output when the selected compare match occurs. Figure 11.3 shows the timing of these operations. The example is for ordinary output upon compare match A with groups 2 and 3.

	φ (MHz)											
	17.2032			18			19.6608			20		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	75	0.48	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	223	0.00	2	233	0.16	2	255	0.00	3	64	0.16
300	2	111	0.00	2	116	0.16	2	127	0.00	2	129	0.16
600	1	223	0.00	1	233	0.16	1	255	0.00	2	64	0.16
1200	1	111	0.00	1	116	0.16	1	127	0.00	1	129	0.16
2400	0	223	0.00	0	233	0.16	0	255	0.00	1	64	0.16
4800	0	111	0.00	0	116	0.16	0	127	0.00	0	129	0.16
9600	0	55	0.00	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	27	0.00	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	16	1.20	0	17	0.00	0	19	–1.70	0	19	0.00
38400	0	13	0.00	0	14	–2.34	0	15	0.00	0	15	1.73

Note: Settings with an error of 1% or less are recommended.

Section 19 Power-Down State

19.1 Overview

In the power-down state, all CPU functions are halted. This lowers power consumption of the SH microprocessor dramatically.

19.1.1 Power-Down Modes

The power-down state includes the following two modes:

1. Sleep mode
2. Standby mode

Sleep mode and standby mode are entered from the program execution state according to the transition conditions given in table 19.1. Table 19.1 also describes procedures for exiting each mode and the states of the CPU and supporting functions.

Table 19.1 Power-Down State

		State						
Mode	**Entering Procedure**	**Clock**	**CPU**	**Supporting Functions**	**CPU Registers**	**RAM**	**I/O Ports**	**Exiting Procedure**
Sleep mode	Execute SLEEP instruction with SBY bit set to 0 in SBYCR	Runs	Halted	Run	Held	Held	Held	• Interrupt • DMA address error • Power-on reset • Manual reset
Standby mode	Execute SLEEP instruction with SBY bit set to 1 in SBYCR	Halted	Halted	Halted*1	Held	Held	Held or high-Z*2	• NMI interrupt • Power-on reset • Manual reset

SBYCR: Standby control register

SBY: Standby bit

Notes: 1. Some of the registers of the on-chip supporting modules are not initialized in standby mode. For details, see table 19.3, Register States in Standby Mode, in section 19.4.1, Transition to Standby Mode, or the descriptions of registers given where the on-chip supporting modules are covered.

2. The status of I/O ports in standby mode are set by the port high-impedance bit (HIZ) in SBYCR. See section 19.2, Standby Control Register (SBYCR), for details. The status of pins other than the I/O ports are described in appendix B, Pin States.

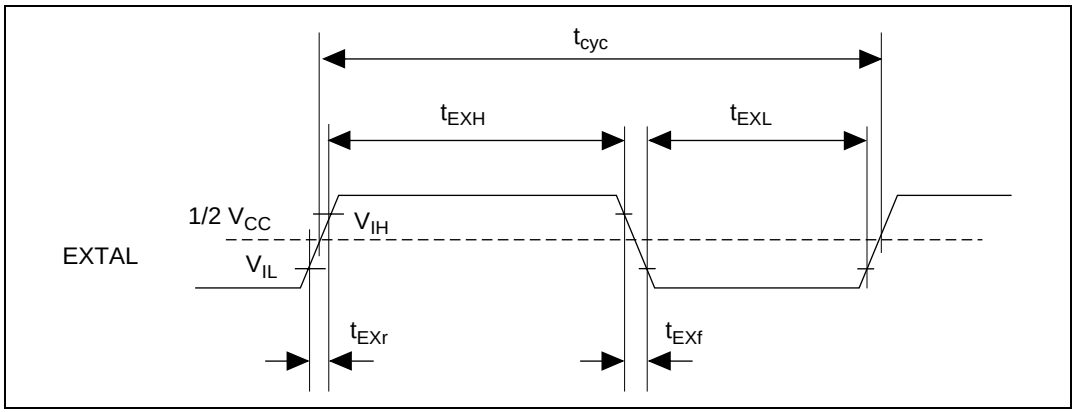


Figure 20.1 EXTAL Input Timing

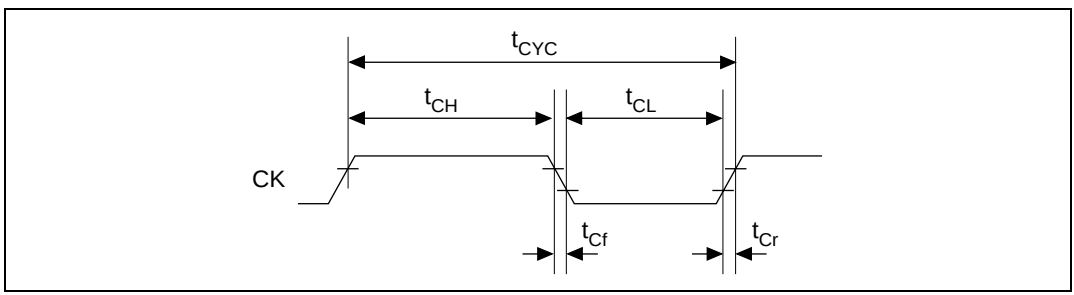


Figure 20.2 System Clock Timing

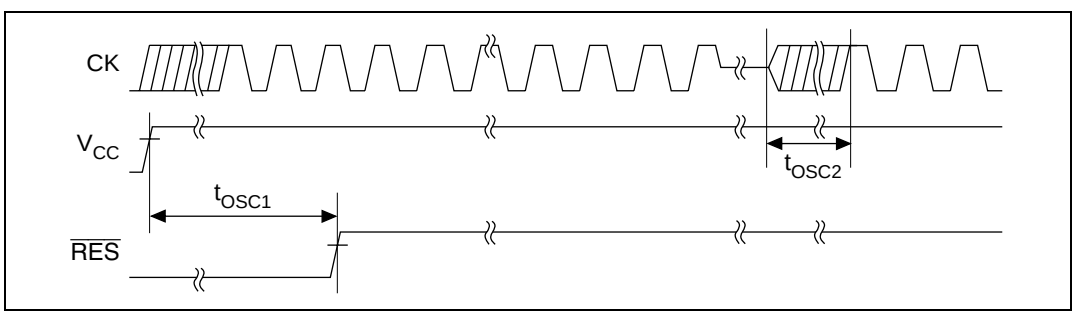


Figure 20.3 Oscillation Settling Time

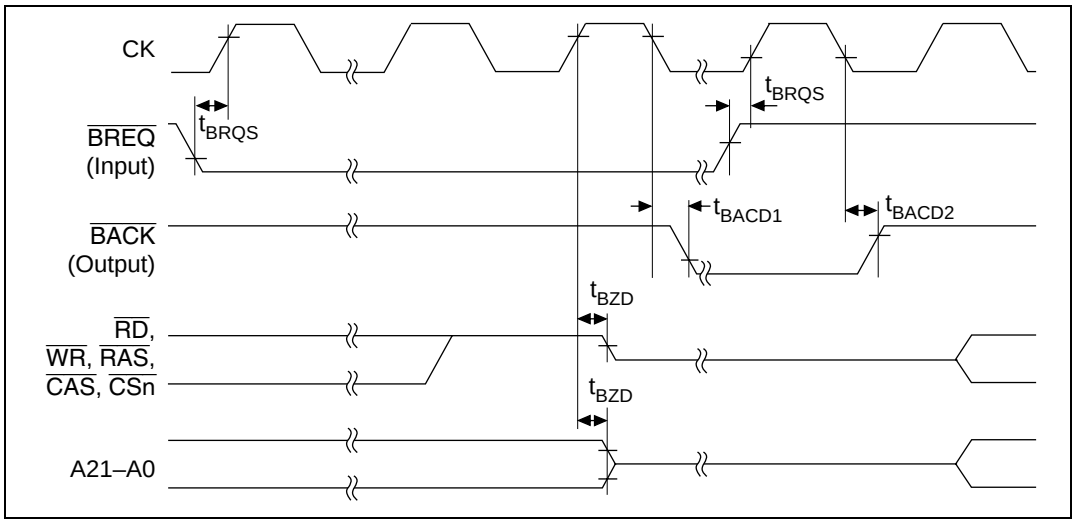
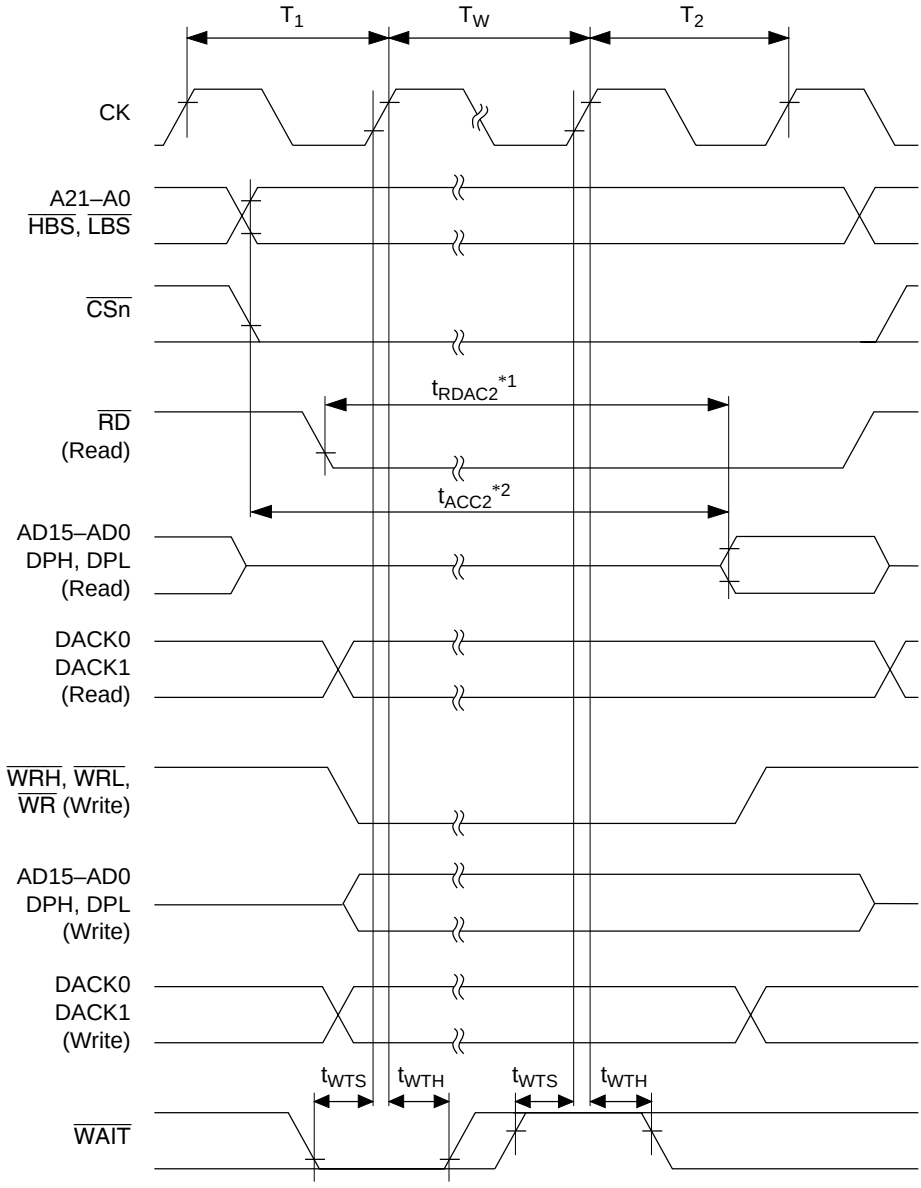


Figure 20.7 Bus Release Timing



Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n+1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n+1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n+2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n+2) - 30$ instead of $t_{cyc} \times (n+2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.10 Basic Bus Cycle: Two States + Wait State

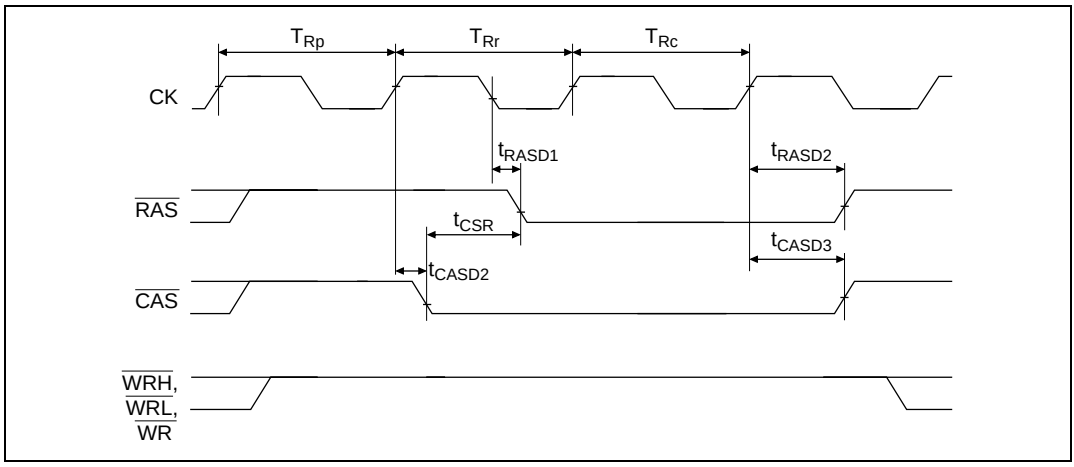


Figure 20.29 CAS-before-RAS Refresh (Short-Pitch)

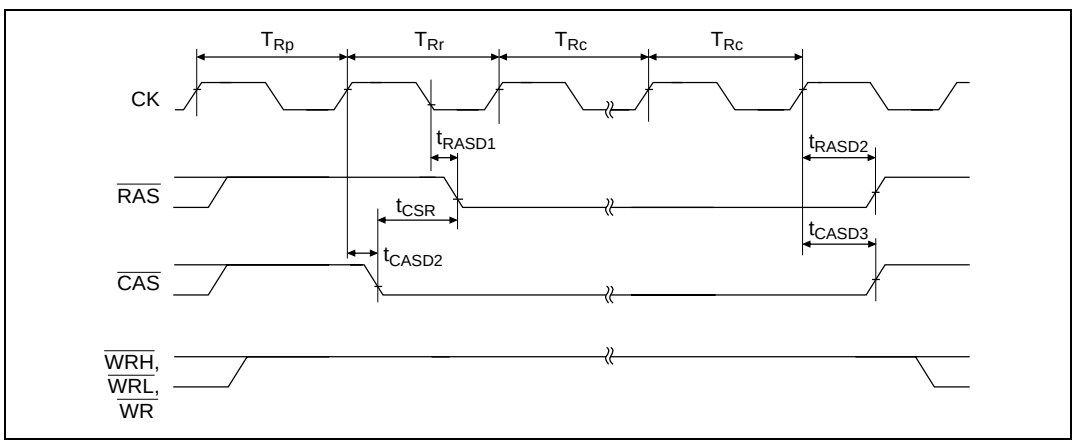


Figure 20.30 CAS-before-RAS Refresh (Long-Pitch)

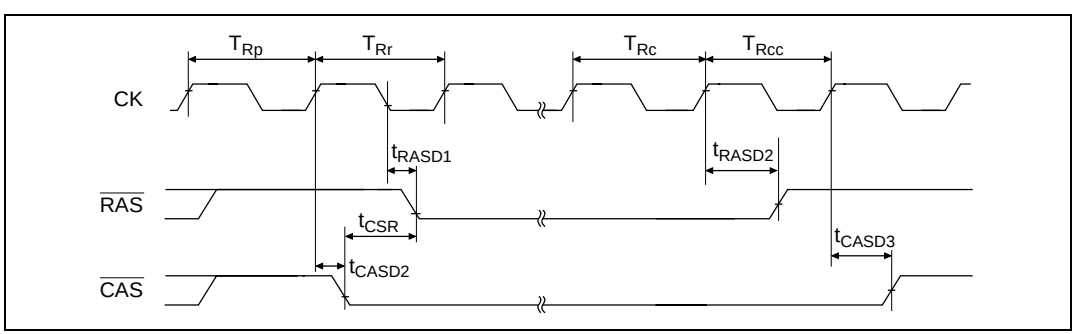
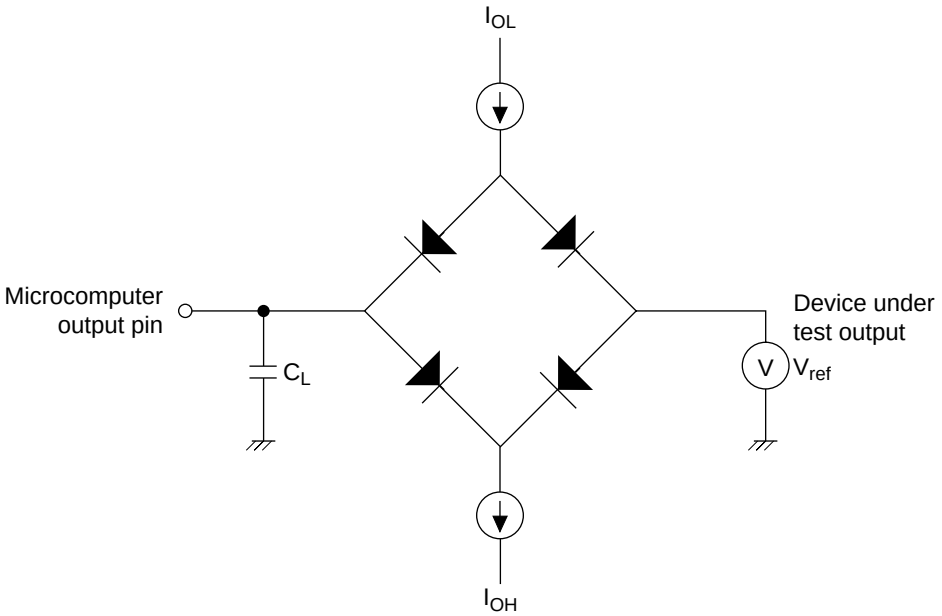


Figure 20.31 Self-Refresh

(10) AC Characteristics Test Conditions



C_L is set as follows for each pin.
30pF: CK, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{CS0}}$–$\overline{\text{CS7}}$, $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{AH}}$, $\overline{\text{IRQOUT}}$, $\overline{\text{RAS}}$, DACK0, DACK1
50pF: A21–A0, AD15–AD0, DPH, DPL, $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{HBS}}$, $\overline{\text{LBS}}$, $\overline{\text{WR}}$
70pF: All port outputs and supporting module output pins other than the above.
I_{OL} and I_{OH} values are as shown in section 20.1.2, DC Characteristics, and table 20.3, Permitted Output Current Values.

Figure 20.44 Output Load Circuit

Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	40	ns	20.63
$\overline{AH}$ delay time 2		t_{AHD2}	—	40	ns	
Multiplexed address delay time		t_{MAD}	—	40	ns	
Multiplexed address hold time		t_{MAH}	–10	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	40	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
DACK0, DACK1 delay time 2		t_{DACD2}	—	40	ns	
DACK0, DACK1 delay time 3*5		t_{DACD3}	—	40	ns	20.53, 20.57, 20.58, 20.63
DACK0, DACK1 delay time 4		t_{DACD4}	—	40	ns	20.55, 20.56
DACK0, DACK1 delay time 5		t_{DACD5}	—	40	ns	
Read delay time	35% duty*1	t_{RDD}	—	$t_{cyc} \times 0.35 + 35$	ns	20.52, 20.53, 20.55–20.59, 20.63
	50% duty		—	$t_{cyc} \times 0.5 + 35$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*3	—	ns	20.55, 20.57
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.60–20.62
Row address hold time		t_{RAH}	10	—	ns	20.55, 20.57
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*1	t_{WCS}	0	—	ns	20.55
	50% duty		0	—	ns	
Access time from $\overline{CAS}$ precharge*4		t_{ACP}	t_{cyc} –20	—	ns	20.56

Notes: 1. When frequency is 10 MHz or more.
2. n is the number of wait cycles.
3. –5ns for parity output of DRAM long-pitch access.
4. If the access time is satisfied, t_{RDS} need not be satisfied.
5. In the relationship between t_{CASD2} and t_{CASD3} for t_{DACD3}, the pair of Min-Max is not exist in the logical structure.

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF60	SAR2*5									DMAC channel 2
H'5FFFF61										
H'5FFFF62										
H'5FFFF63										
H'5FFFF64	DAR2*5									
H'5FFFF65										
H'5FFFF66										
H'5FFFF67										
H'5FFFF68	—	—	—	—	—	—	—	—	—	
H'5FFFF69	—	—	—	—	—	—	—	—	—	
H'5FFFF6A	TCR2*5									
H'5FFFF6B										
H'5FFFF6C	—	—	—	—	—	—	—	—	—	
H'5FFFF6D	—	—	—	—	—	—	—	—	—	
H'5FFFF6E	CHCR2	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'5FFFF6F		AM	AL	DS	TM	TS	IE	TE	DE	
H'5FFFF70	SAR3*5									DMAC channel 3
H'5FFFF71										
H'5FFFF72										
H'5FFFF73										
H'5FFFF74	DAR3*5									
H'5FFFF75										
H'5FFFF76										
H'5FFFF77										
H'5FFFF78	—	—	—	—	—	—	—	—	—	
H'5FFFF79	—	—	—	—	—	—	—	—	—	
H'5FFFF7A	TCR3*5									
H'5FFFF7B										
H'5FFFF7C	—	—	—	—	—	—	—	—	—	
H'5FFFF7D	—	—	—	—	—	—	—	—	—	
H'5FFFF7E	CHCR3	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H5FFFF7F		AM	AL	DS	TM	TS	IE	TE	DE	

A.2.37 Break Address Mask Register H (BAMRH) UBC

Start Address: H'5FFFF94

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	BAM16
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.38 BAMRH Bit Functions

Bit	Bit name	Description
15–0	Break address masks 31–16 (BAM31–BAM16)	Specifies the bits to be masked in the break address specified in BARH