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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-1
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417034afi20v

Table 2.17 System Control Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
CLRT		0000000000001000	0 → T	1	0
CLRMAC		0000000000101000	0 → MACH, MACL	1	—
LDC	Rm,SR	0100mmmm00001110	Rm → SR	1	LSB
LDC	Rm,GBR	0100mmmm00011110	Rm → GBR	1	—
LDC	Rm,VBR	0100mmmm00101110	Rm → VBR	1	—
LDC.L	@Rm+,SR	0100mmmm00000111	(Rm) → SR, Rm + 4 → Rm	3	LSB
LDC.L	@Rm+,GBR	0100mmmm00010111	(Rm) → GBR, Rm + 4 → Rm	3	—
LDC.L	@Rm+,VBR	0100mmmm00100111	(Rm) → VBR, Rm + 4 → Rm	3	—
LDS	Rm,MACH	0100mmmm00001010	Rm → MACH	1	—
LDS	Rm,MACL	0100mmmm00011010	Rm → MACL	1	—
LDS	Rm,PR	0100mmmm00101010	Rm → PR	1	—
LDS.L	@Rm+,MACH	0100mmmm00000110	(Rm) → MACH, Rm + 4 → Rm	1	—
LDS.L	@Rm+,MACL	0100mmmm00010110	(Rm) → MACL, Rm + 4 → Rm	1	—
LDS.L	@Rm+,PR	0100mmmm00100110	(Rm) → PR, Rm + 4 → Rm	1	—
NOP		0000000000001001	No operation	1	—
RTE		0000000000101011	Delayed branch, stack area → PC/SR	4	—
SETT		0000000000011000	1 → T	1	1
SLEEP		0000000000011011	Sleep	3*	—
STC	SR,Rn	0000nnnn00000010	SR → Rn	1	—
STC	GBR,Rn	0000nnnn00010010	GBR → Rn	1	—
STC	VBR,Rn	0000nnnn00100010	VBR → Rn	1	—
STC.L	SR,@–Rn	0100nnnn00000011	Rn–4 → Rn, SR → (Rn)	2	—
STC.L	GBR,@–Rn	0100nnnn00010011	Rn–4 → Rn, GBR → (Rn)	2	—
STC.L	VBR,@–Rn	0100nnnn00100011	Rn–4 → Rn, VBR → (Rn)	2	—
STS	MACH,Rn	0000nnnn00001010	MACH → Rn	1	—

Note: * The number of execution states before the chip enters the sleep state.

Bits 9 and 8—Multiplex Shift Count 1 and 0 (MXC1 and MXC0): Shift row addresses downward by a certain number of bits (8–10) when row and column addresses are multiplexed (MXE = 1). Regardless of the MXE bit setting, these bits also select the range of row addresses compared in burst operation.

Bit 9: MXC1	Bit 8: MXC0	Row Address Shift (MXE = 1)		Row Address Bits Compared (in Burst Operation) (MXE = 0 or 1)	
0	0	8 bits	(Initial value)	A8–A27	(Initial value)
	1	9 bits		A9–A27	
1	0	10 bits		A10–A27	
	1	Reserved		Reserved	

Bits 7–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.6 Refresh Control Register (RCR)

The refresh control register (RCR) is a 16-bit read/write register that controls the start of refreshing and selects the refresh mode and the number of wait states during refreshing. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

To prevent RCR from being written incorrectly, it must be written by a different method from most other registers. A word transfer operation is used, H'5A is written in the upper byte, and the actual data is written in the lower byte. For details, see section 8.2.11, Notes on Register Access.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	RFSHE	RMODE	RLW1	RLW0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Bit 15–8—Reserved: These bits are always read as 0.

8.4.2 Wait State Control

The number of external memory space access states and the insertion of wait states can be controlled using the WCR1–WCR3 bits. The bus cycles that can be controlled are the CPU read cycle and the DMAC dual mode read cycle. The bus cycle that can be controlled using the WCR2 is the DMAC single-mode read/write cycle.

Table 8.9 shows the number of states and number of wait states in access cycles to external memory spaces.

Table 8.9 Number of States and Number of Wait States in Access Cycles to External Memory Spaces

	CPU Read Cycle, DMAC Dual Mode Read Cycle, DMAC Single Mode Read/Write Cycle		CPU Write Cycle and DMAC Dual Mode Write Cycle (Cannot be controlled by WCR1)*2
Area	Corresponding Bits in WCR1 and WCR2 = 0	Corresponding Bits in WCR1 and WCR2 = 1	
1, 3–5, 7	1 cycle fixed; $\overline{\text{WAIT}}$ signal ignored	2 cycles fixed + wait state from $\overline{\text{WAIT}}$ signal*3	
0, 2, 6 (long wait available)	1 cycle + long wait state, $\overline{\text{WAIT}}$ signal ignored	1 cycle + long wait state*1 + wait state from $\overline{\text{WAIT}}$ signal	

Notes: 1. The number of long wait states is set by WCR3.
2. When DRAME = 1, short pitch/long pitch is selected with the WW1 bit in WCR1.
3. Pin wait cannot be used for the CS7 and $\overline{\text{WAIT}}$ pins of area 3 because they are multiplexed.

For the CPU read cycle, DMAC dual mode read cycle, and DMAC single mode read/write cycle, the access cycle is completed in 1 state when the corresponding bits of WCR1 and WCR2 for areas 1, 3–5, and 7 are cleared to 0 and the $\overline{\text{WAIT}}$ pin input signal is not sampled. When the bits are set to 1, the $\overline{\text{WAIT}}$ signal is sampled and the number of states is 2 plus the number of wait states set by the $\overline{\text{WAIT}}$ signal. The $\overline{\text{WAIT}}$ signal is sampled at the rise of the system clock (CK) directly preceding the second state of the bus cycle and the wait states are inserted as long as the level is low. When a high level is detected, it shifts to the second state (final state). Figure 8.13 shows the wait state timing when accessing the external memory spaces of areas 1, 3, 4, 5, and 7.

8.6 Address/Data Multiplexed I/O Space Access

The BSC is equipped with a function that multiplexes address and data input/output on pins AD15–AD0 in area 6. This allows the SH microprocessor to be directly connected to peripheral chips that require address/data multiplexing.

8.6.1 Basic Timing

When the multiplexed I/O enable bit (IOE) in BCR is set to 1, the area 6 space with address bit A27 as 0 (H'6000000–H'6FFFFFF) becomes an address/data multiplexed I/O space that, when accessed, multiplexes addresses and data. When the A14 address bit is 0, the bus width is 8 bits and address output and data input/output are performed on the AD7–AD0 pins. When the A14 address bit is 1, the bus width is 16 bits and address output and data input/output are performed on the AD15–AD0 pins. In the address/data multiplexed I/O space, access is controlled with the $\overline{AH}$, $\overline{RD}$, and $\overline{WR}$ signals. Accesses in the address/data multiplexed I/O space are performed in 4 states, regardless of the WCR settings. Figure 8.32 shows the timing when the address/data multiplexed I/O space is accessed.

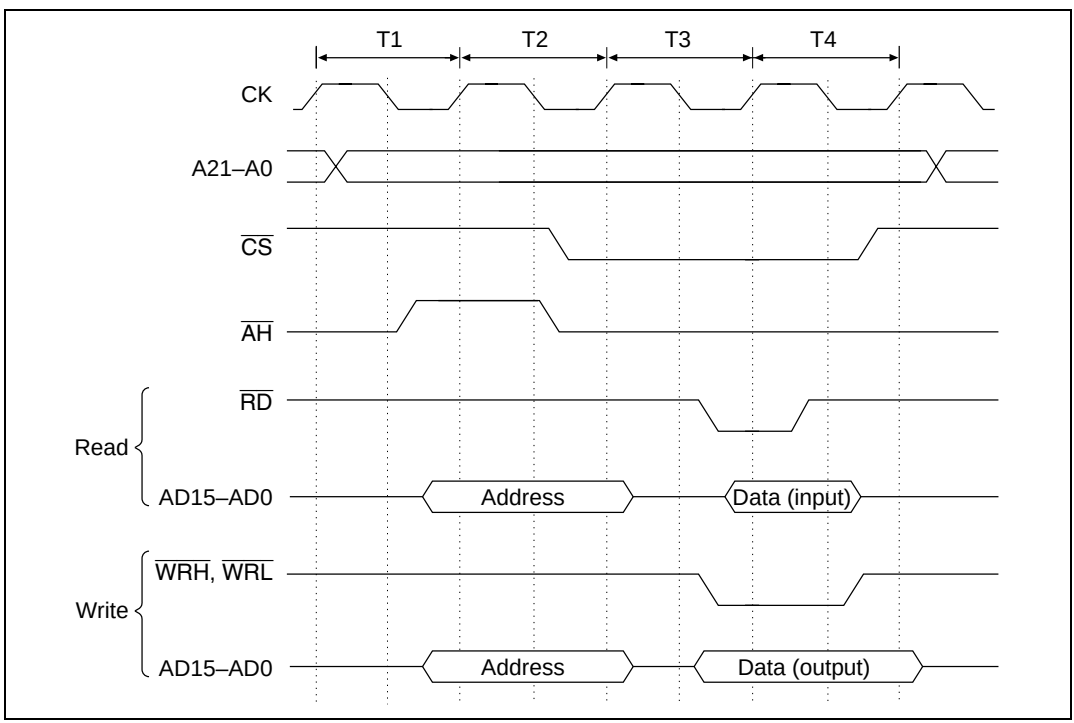


Figure 8.32 Access Timing For Address/Data Multiplexed I/O Space

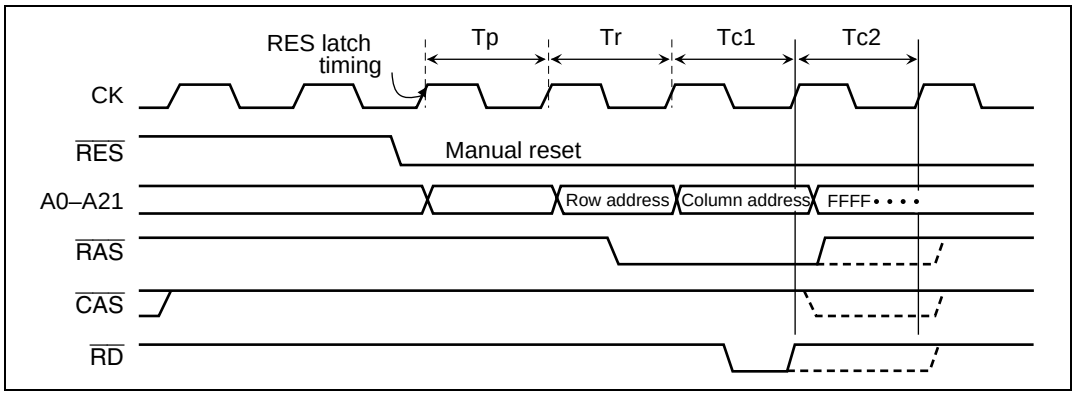


Figure 8.40 Long-Pitch Mode Read (1)

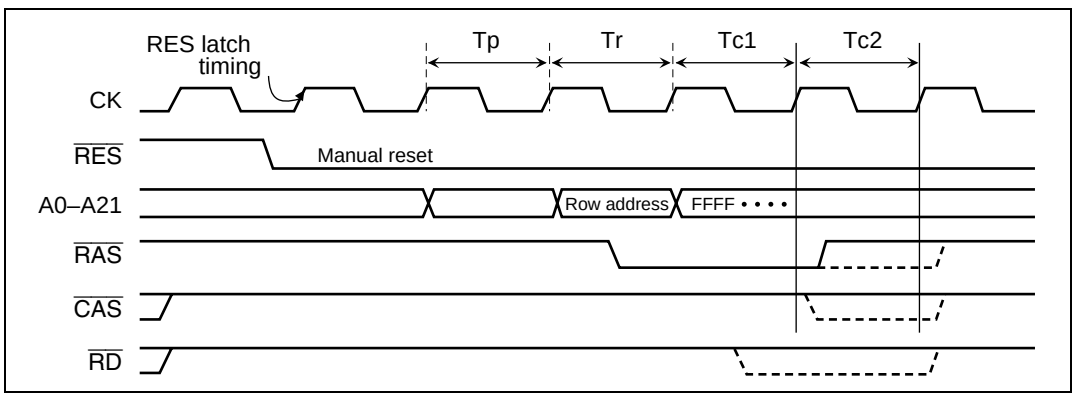


Figure 8.41 Long-Pitch Mode Read (2)

For the signal output shown by solid lines, DRAM data may not be held. Therefore, when DRAM data must be held after a reset, take one of the measures described below.

1. When resetting manually, use the watchdog timer (WDT) reset function.
2. Even if the low width of $\overline{RAS}$ becomes as short as 1.5 tcyc as shown above, use with a frequency that satisfies the DRAM standard (t_{RAS}).
3. Even if the low width of $\overline{RAS}$ is 1.5 tcyc, use an external circuit so that a $\overline{RAS}$ signal with a low width of 2.5 tcyc is input in the DRAM (if the low width of $\overline{RAS}$ is higher than 2.5 tcyc, operate so that the current waveform is input in the DRAM).

These measures are not required when DRAM data is initialized or loaded again after a manual reset.

Section 9 Direct Memory Access Controller (DMAC)

9.1 Overview

The SuperH microcomputer chip includes a four-channel direct memory access controller (DMAC). The DMAC can be used in place of the CPU to perform high speed transfers between external devices that have DACK (transfer request acknowledge signal), external memory, memory-mapped external devices, on-chip memory, and on-chip supporting modules (excluding the DMAC itself). Using the DMAC reduces the burden on the CPU and increases overall operating efficiency.

9.1.1 Features

The DMAC has the following features.

- Four channels
- Four Gbytes of address space in the architecture
- Byte or word selectable as data transfer unit
- 65536 transfers (maximum)
- Single address mode transfers (channels 0 and 1): Either the transfer source or transfer destination (peripheral device) is accessed by a DACK signal (selectable) while the other is accessed by address. One transfer unit of data is transferred in each bus cycle.

  Device combinations for which transfer is possible:

  — External device with DACK and memory-mapped external device (including external memories)

  — External device with DACK and memory-mapped external memory
- Dual address mode transfer (channels 0–3): Both the transfer source and transfer destination are accessed by address. One transfer unit of data is transferred in 2 bus cycles.

  Device combinations for which transfer is possible:

  — Two external memories

  — External memory and memory-mapped external device

  — Two memory-mapped devices

  — External memory and on-chip memory

  — Memory-mapped external device and on-chip supporting module (excluding the DMAC)

  — External memory and on-chip memory

  — Memory-mapped external device and on-chip supporting module (excluding the DMAC)

  — Two on-chip memories

9.1.3 Pin Configuration

Table 9.1 shows the DMAC pins.

Table 9.1 Pin Configuration

Channel	Name	Symbol	I/O	Function
0	DMA transfer request	$\overline{\text{DREQ0}}$	I	DMA transfer request input from external device to channel 0
	DMA transfer request acknowledge	DACK0	O	DMA transfer request acknowledge output from channel 0 to external device
1	DMA transfer request	$\overline{\text{DREQ1}}$	I	DMA transfer request input from external device to channel 1
	DMA transfer request acknowledge	DACK1	O	DMA transfer request acknowledge output from channel 1 to external device

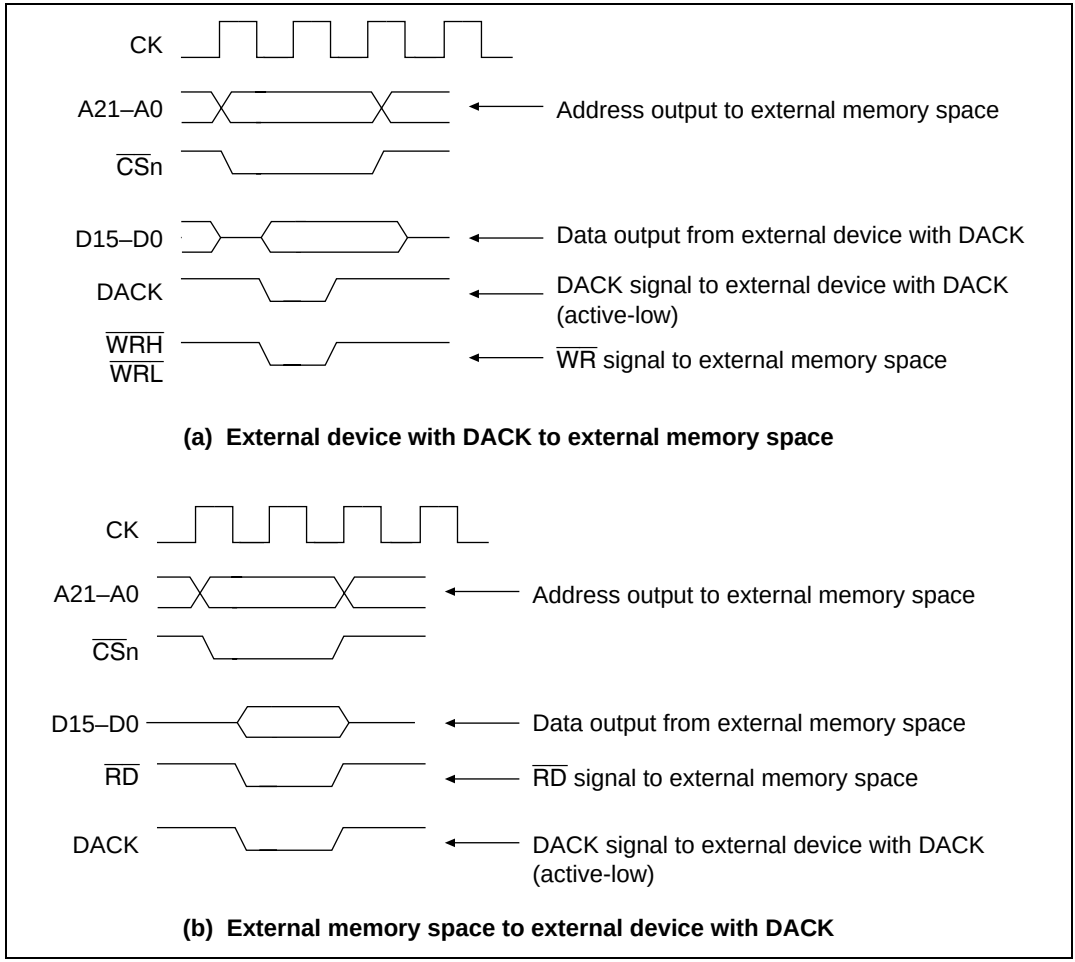


Figure 9.7 Examples of DMA Transfer Timing in Single Address Mode

- Dual Address Mode

  In dual address mode, both the transfer source and destination are accessed (selectable) by an address. The source and destination can be located externally or internally. The source is accessed in the read cycle and the destination in the write cycle, so the transfer is performed in two separate bus cycles. The transfer data is temporarily stored in the DMAC. Figure 9.8 shows an example of a transfer between two external memories in which data is read from one memory in the read cycle and written to the other memory in the following write cycle.

Bit 3—Count Start 3 (STR3): STR3 starts and stops TCNT3.

Bit 3: STR3	Description	
0	TCNT3 is halted	(Initial value)
1	TCNT3 is counting	

Bit 2—Count Start 2 (STR2): STR2 starts and stops TCNT2.

Bit 2: STR2	Description	
0	TCNT2 is halted	(Initial value)
1	TCNT2 is counting	

Bit 1—Count Start 1 (STR1): STR1 starts and stops TCNT1.

Bit 1: STR1	Description	
0	TCNT1 is halted	(Initial value)
1	TCNT1 is counting	

Bit 0—Count Start 0 (STR0): STR0 starts and stops TCNT0.

Bit 0: STR0	Description	
0	TCNT0 is halted	(Initial value)
1	TCNT0 is counting	

10.2.2 Timer Synchro Register (TSNC)

The timer synchro register (TSNC) is an eight-bit read/write register that selects timer synchronizing modes for channels 0–4. Channels for which 1 is set in the corresponding bit will be synchronized. TSNC is initialized to H'E0 or H'60 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	—	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	*	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bit	7	6	5	4	3	2	1	0
	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value	*	0	0	0	1	0	0	0
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: * Undefined

Bit 7—Reserved: Bit 7 is read as undefined. The write value should be 0 or 1.

Bits 6–4—I/O Control B2–B0 (IOB2–IOB0): IOB2–IOB0 selects the GRB function.

Bit 6: IOB2	Bit 5: IOB1	Bit 4: IOB0	GRB Function	
0	0	0	GRB is an output compare register	Compare match with pin output disabled (Initial value)
		1		0 output at GRB compare match*[1]
	1	0		1 output at GRB compare match*[1]
		1		Output toggles at GRB compare match (1 output for channel 2 only)*[1] *[2]
1	0	0	GRB is an input capture register	GRB captures rising edge of input
		1		GRB captures falling edge of input
	1	0		GRB captures both edges of input
		1		

Notes: 1. After reset, the value output is 0 until the first compare match occurs.
2. Channel 2 has no compare-match driven toggle output function. If it is set for toggle, 1 is automatically selected as the output.

Bit 3—Reserved: Bit 3 always is read as 1. The write value should always be 1.

Bits 13 and 12—PB6 Mode (PB6MD1 and PB6MD0): PB6MD1 and PB6MD0 select the function of the PB6/TP6/TOCXA4/TCLKC pin.

Bit 13: PB6MD1	Bit 12: PB6MD0	Function	
0	0	Input/output (PB6)	(Initial value)
	1	ITU timer clock input (TCLKC)	
1	0	ITU output compare (TOCXA4)	
	1	Timing pattern output (TP6)	

Bits 11 and 10—PB5 Mode (PB5MD1 and PB5MD0): PB5MD1 and PB5MD0 select the function of the PB5/TP5/TIOCB4 pin.

Bit 11: PB5MD1	Bit 10: PB5MD0	Function	
0	0	Input/output (PB5)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCB4)	
	1	Timing pattern output (TP5)	

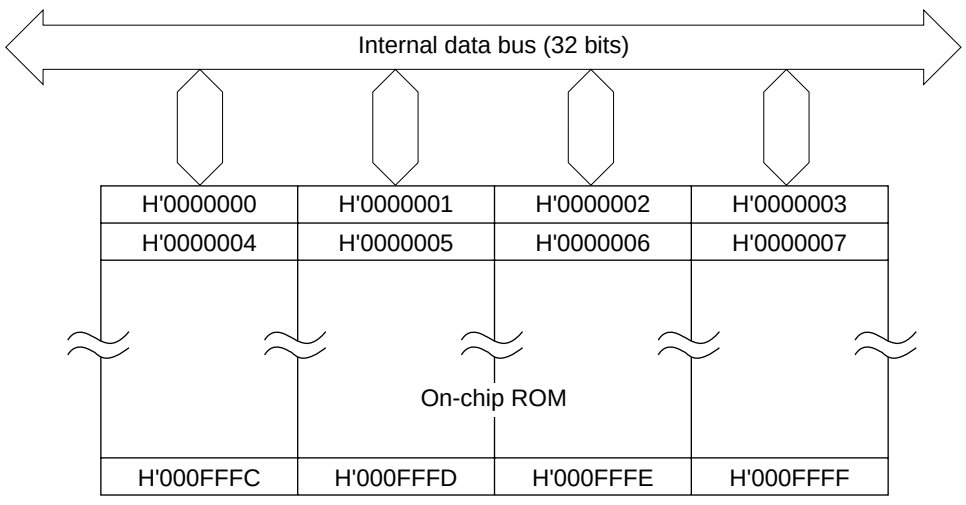
Bits 9 and 8—PB4 Mode (PB4MD1 and PB4MD0): PB4MD1 and PB4MD0 select the function of the PB4/TP4/TIOCA4 pin.

Bit 9: PB4MD1	Bit 8: PB4MD0	Function	
0	0	Input/output (PB4)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCA4)	
	1	Timing pattern output (TP4)	

Section 17 ROM

17.1 Overview

The SH7034 microcomputer has 64 kbytes of on-chip ROM (mask ROM or PROM). The on-chip ROM is connected to the CPU and the direct memory access controller (DMAC) through a 32-bit data bus (figure 17.1). The CPU can access the on-chip ROM in 8-, 16- and 32-bit widths and the DMAC can access the ROM in 8- and 16-bit widths. Data in the on-chip ROM can always be accessed in one cycle.



Note: The addresses shown in the figure are the uppermost shadow addresses in the on-chip ROM space.

Figure 17.1 Block Diagram of ROM

The operating mode determines whether the on-chip ROM is valid or not. The operating mode is selected using mode-setting pins MD0–MD2 as shown in table 17.1. When using the on-chip ROM, select mode 2; otherwise, select mode 0 or 1. The on-chip ROM is allocated to addresses H'0000000–H'000FFFF of memory area 0. Memory area 0 (H'0000000–H'0FFFFFF and H'8000000–H'8FFFFFF) is divided into 64-kbyte shadows. No matter which shadow is accessed, the on-chip ROM is accessed. See section 8, Bus State Controller (BSC), for more information on shadows.

Bits 5–0—Reserved: Bit 5 is a read-only bit that is always read as 0. Only write 0 in bit 5. Writing to bits 4–0 is disabled. These bits are always read as 1.

19.3 Sleep Mode

19.3.1 Transition to Sleep Mode

Execution of the SLEEP instruction when the standby bit (SBY) in the standby control register (SBYCR) is cleared to 0 causes a transition from the program execution state to sleep mode. Although the CPU halts immediately after executing the SLEEP instruction, the contents of its internal registers remain unchanged. The on-chip supporting modules do not halt in sleep mode.

19.3.2 Exiting Sleep Mode

Sleep mode is exited by an interrupt, DMA address error, power-on reset, or manual reset.

Exit by Interrupt: When an interrupt occurs, sleep mode is exited and interrupt exception handling is executed. Sleep mode is not exited if the interrupt cannot be accepted because its priority level is equal to or less than the mask level set in the CPU's status register (SR). Likewise, sleep mode is not exited if the interrupt is disabled by the on-chip supporting module.

Exit by DMA Address Error: If the DMAC operates during sleep mode and a DMA address error occurs, sleep mode is exited and DMA address error exception handling is executed.

Exit by Power-On Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is high, sleep mode is exited and the power-on reset state is entered. If the NMI signal is brought from low to high in order to set the chip for a power-on reset, an NMI interrupt will occur whenever the rising edge of NMI is selected as the valid edge (with NMI edge select bit NMIE in the interrupt control register (ICR) of the interrupt controller). When this occurs, the NMI interrupt clears sleep mode.

Exit by Manual Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is low, sleep mode is exited and the manual reset state is entered. If the NMI signal is brought from high to low in order to set the chip for a manual reset, sleep mode will be exited by an NMI interrupt whenever the falling edge of NMI is selected as the valid edge (with the NMIE bit).

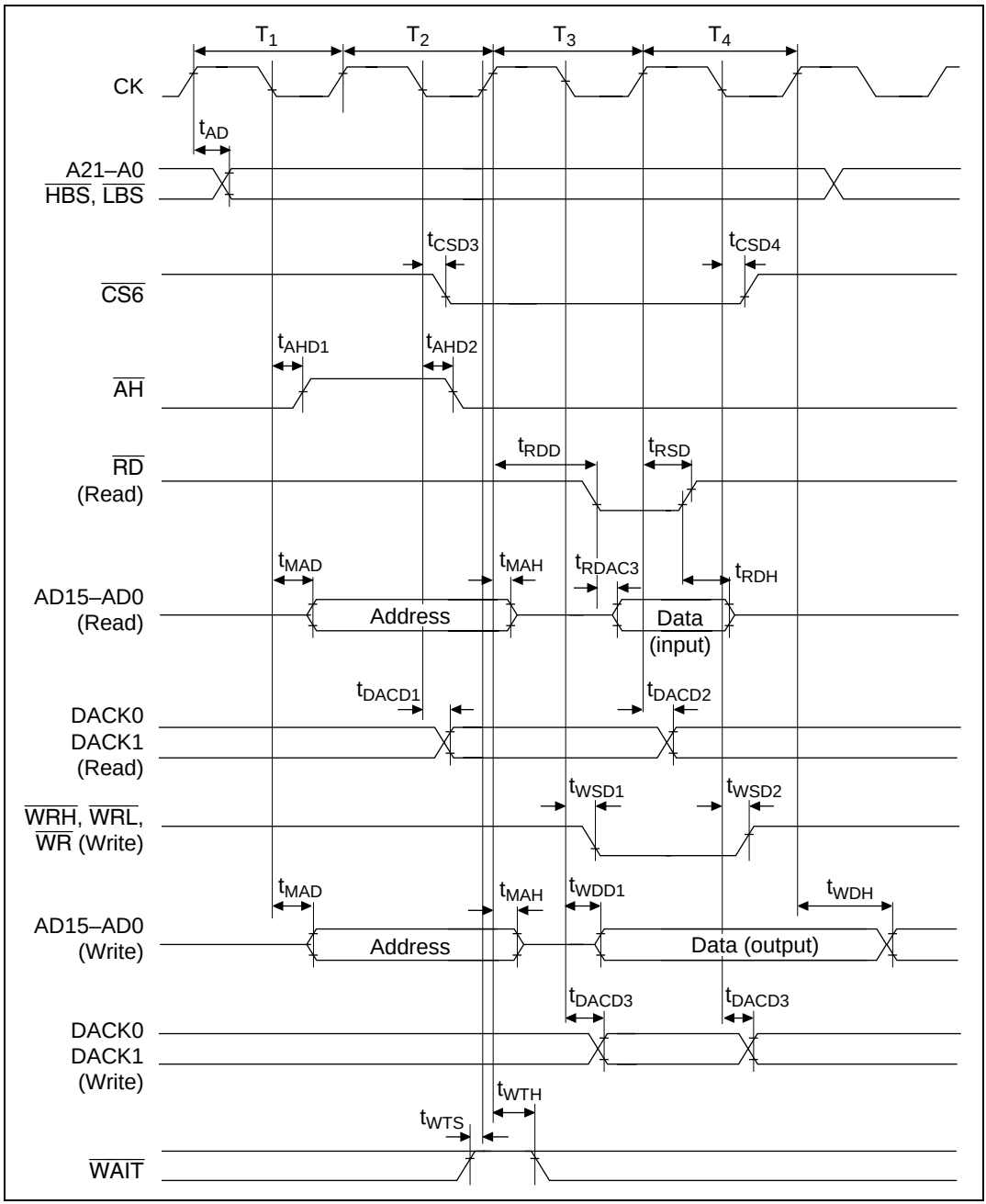


Figure 20.19 Address/Data Multiplex I/O Bus Cycle

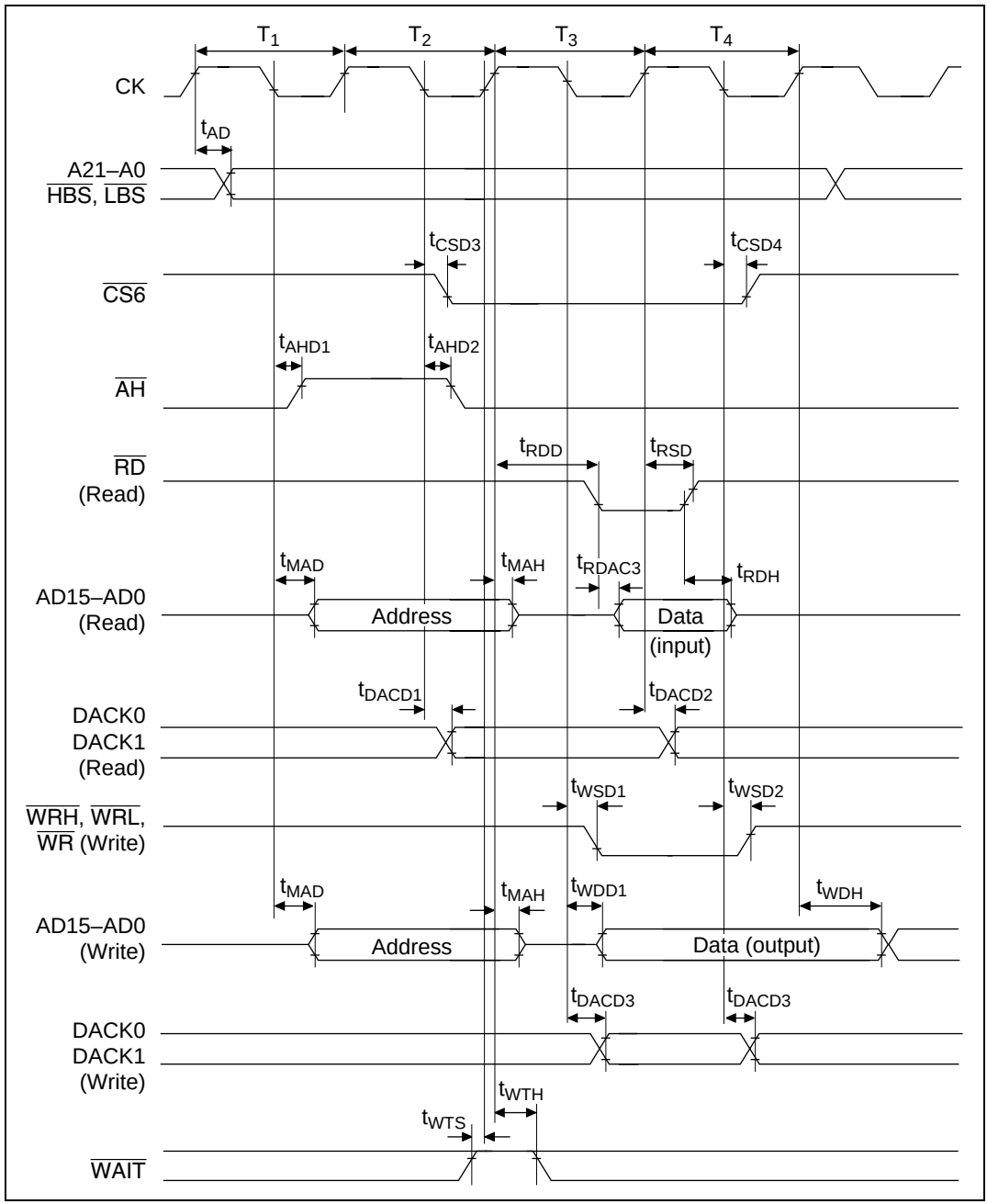


Figure 20.32 Address/Data Multiplex I/O Bus Cycle

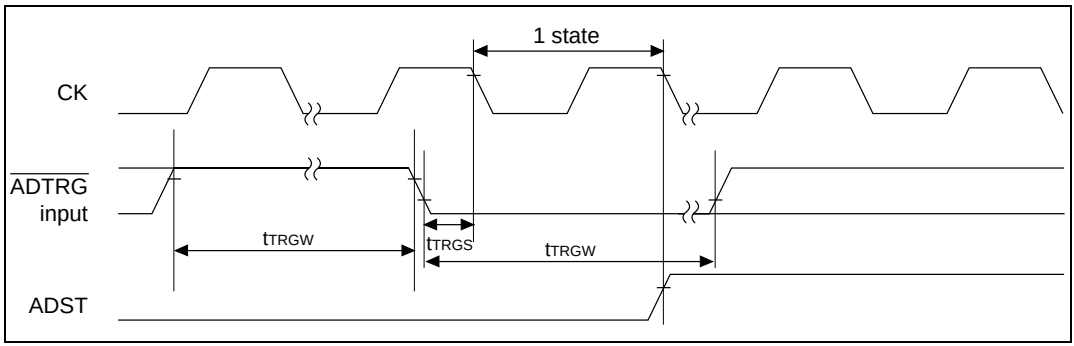


Figure 20.42 External Trigger Input Timing

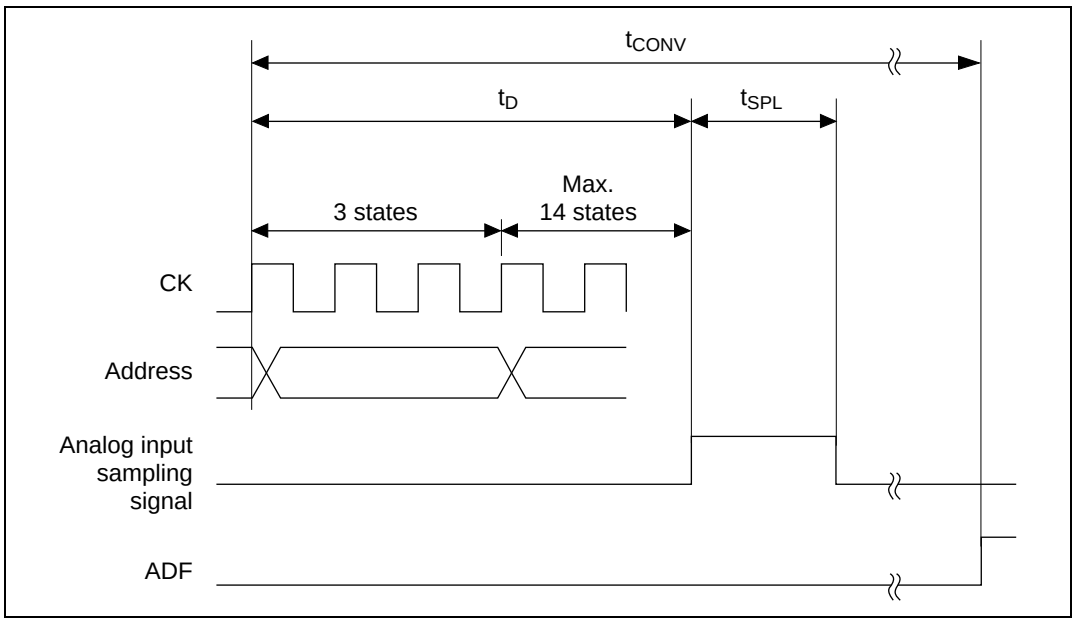


Figure 20.43 Analog Conversion Timing

Table 20.16 DC Characteristics

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	EXTAL	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	Port C		$V_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
	Other input pins		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
Input low-level voltage	Other Schmidt trigger input pins	V_{IL}	–0.3	—	$V_{CC} \times 0.2$	V	
Schmidt trigger input voltage	$\overline{RES}$, NMI, MD2–MD0, PA13–10, PA2, PA0, PB7–PB0	V_T^+	$V_{CC} \times 0.9$	—	—	V	
		V_T^-	—	—	$V_{CC} \times 0.1$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input leakage current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leakage current (off state)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.7	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

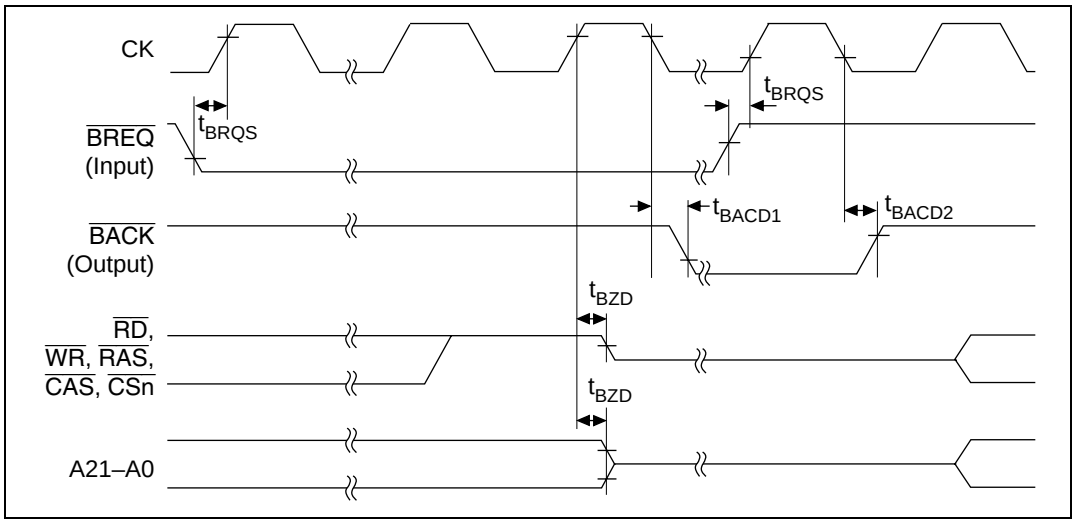


Figure 20.51 Bus Release Timing

Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	20	ns	20.63
$\overline{AH}$ delay time 2		t_{AHD2}	—	20	ns	
Multiplexed address delay time		t_{MAD}	—	30	ns	
Multiplexed address hold time		t_{MAH}	0	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	23	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
DACK0, DACK1 delay time 2		t_{DACD2}	—	23	ns	
DACK0, DACK1 delay time 3*7		t_{DACD3}	—	20	ns	20.53, 20.57, 20.58, 20.63
DACK0, DACK1 delay time 4		t_{DACD4}	—	20	ns	20.55, 20.56
DACK0, DACK1 delay time 5		t_{DACD5}	—	20	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.52, 20.53, 20.55–20.59, 20.63
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*5	—	ns	20.55, 20.57
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.60–20.62
Row address hold time		t_{RAH}	10	—	ns	20.55, 20.57
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	20.55
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge*6		t_{ACP}	t_{cyc} –20	—	ns	20.56

Notes: 1. HBS and LBS signals are 25 ns.
2. When frequency is 10 MHz or more.
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25 ns.
5. –5ns for parity output of DRAM long-pitch access.
6. It is not necessary to meet the t_{RDS} specification as long as the access time specification is met.
7. In the relationship of t_{CASD2} and t_{CASD3} with respect to t_{DACD3}, a Min-Max combination does not occur because of the logic structure.