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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dp512cpv

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Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.16	31 Mar 2003	31 Mar 2003		- Corrections in App. A ÒNVM, Flash and EEPROMÓ - Number of words per flash row = 64 - Replaced ÒburstprogrammingÓwith Òrow programmingÓ - Sector erase size = 1024 bytes - Corrected feature description ECT - Corrected min. bus freq. in table ÒOperating ConditionsÓ
V01.17	30 May 2003	30 May 2003		- Replaced references to HCS12 Core Guide with the individual HCS12 Block guides throughout document - Table ÒAbsolute Maximum RatingsÓcorrected footnote on clamp of TEST pin
V01.18	23 Jul 2003	23 Jul 2003		- Mentioned ÒS12 LRAEÓbootloader in Flash section - Document References: corrected S12 CPU document reference
V01.19	24 Jul 2003	24 Jul 2003		- Added part ID for 2L00M maskset.
V01.20	01 Sep 2003	01 Sep 2003		- Added part ID for 3L00M maskset. - Added cycle definition to ÒCPU 12 Block DescriptionÓ - Diagram ÒClock ConnectionsÓConnected Bus Clock to HCS12 Core. - Corrected ÒBackground Debug ModuleÓto ÒHCS12 BreakpointÓat address $0028 - $002F in table 1-1. - Corrected ÒBlank Check Time FlashÓvalue in table ÒNVM Timing CharacteristicsÓ - Added EXTAL pin VIH, VIL and EXTAL pin hysteresis value to ÒOscillator CharacteristicsÓUpdated oscillator description and table note.
V01.21	08 Mar 2004	08 Mar 2004		- Added part ID for 4L00M maskset. - Corrected pin name KWP5 in device pinout.
V01.22	23 Aug 2004	23 Aug 2004		- Updated $V_{IH,EXTAL}$ and $V_{IL,EXTAL}$ in table ÒOscillator CharacteristicsÓ - Removed item ÒOscillatorÓfrom table ÒOperating ConditionsÓas already covered in table ÒOscillator CharacteristicsÓ
V01.23	09 Feb 2005	09 Feb 2005		- Corrected Flash Row Programming Time in NVM Timing Characteristics
V01.24	01 Apr 2005	01 Apr 2005		- Changed T_{Javg} and added footnote to data retention time in NVM Reliability Characteristics
V01.25	05 Jul 2005	05 Jul 2005		- Updated NVM Reliability Characteristics

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- The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN0.
- The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC.
- Do not write MODRR1 and MODRR0 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN0.
- Do not write MODRR3 and MODRR2 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN4.

Document References

The Device Guide provides information about the MC9S12DP512 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the individual Block Guides of the implemented modules. In an effort to reduce redundancy, all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

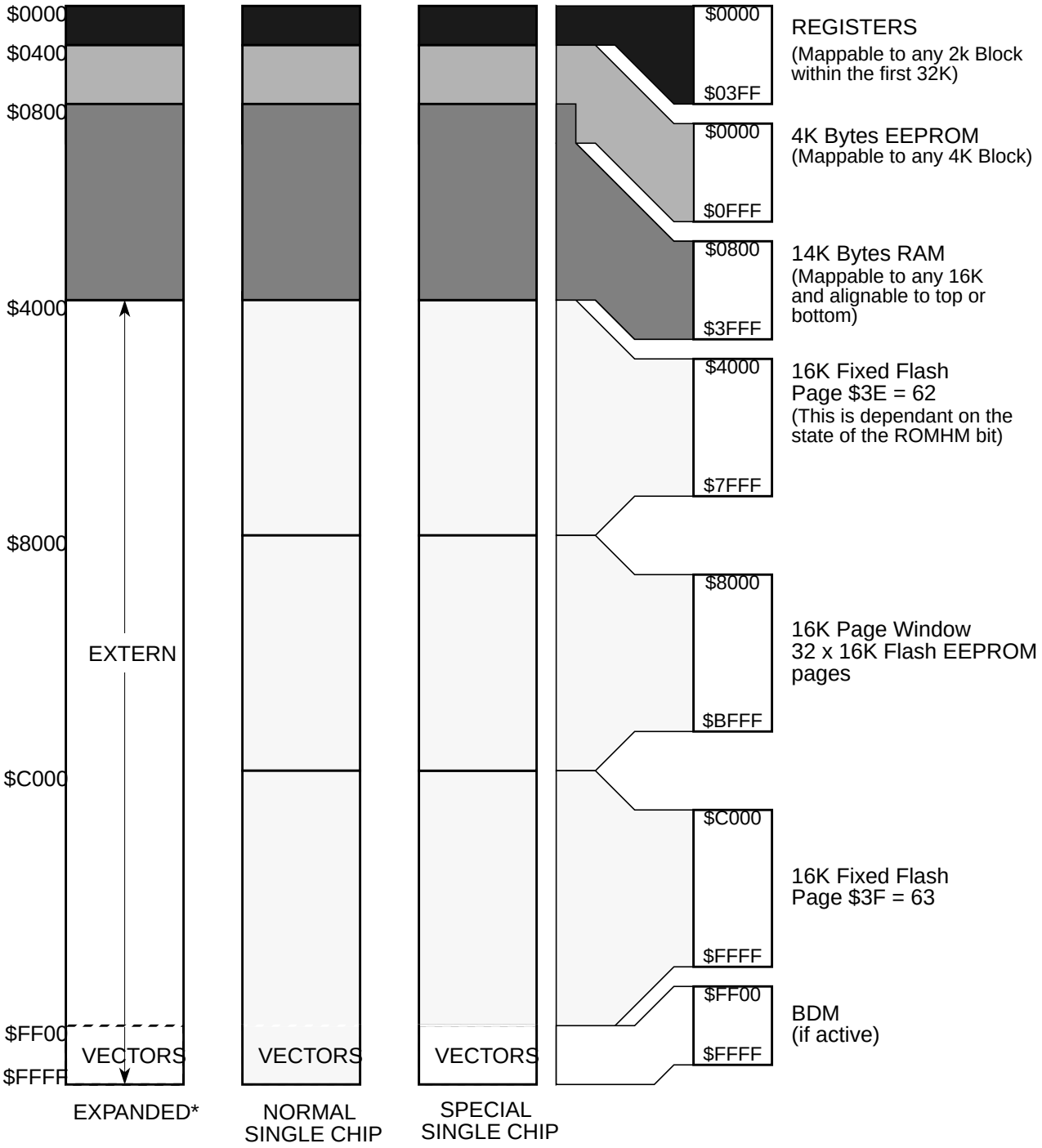
See Table 0-2 for names and versions of the referenced documents throughout the Device Guide.

Table 0-2 Document References

Block Guide	Version	Document Order Number
HCS12 CPU Reference Manual	V02	S12CPUV2/D
HCS12 Module Mapping Control (MMC) Block Guide	V04	S12MMCV4/D
HCS12 Multiplexed External Bus Interface (MEBI) Block Guide	V03	S12MEBIV3/D
HCS12 Interrupt (INT) Block Guide	V01	S12INTV1/D
HCS12 Background Debug (BDM) Block Guide	V04	S12BDMV4/D
HCS12 Breakpoint (BKP) Block Guide	V01	S12BKPV1/D
Clock and Reset Generator (CRG) Block Guide	V04	S12CRGV4/D
Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block Guide	V01	S12ECT16B8V1/D
Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block Guide	V02	S12ATD10B8CV2/D
Inter IC Bus (IIC) Block Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block Guide	V03	S12SPIV3/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block Guide	V01	S12PWM8B8CV1/D
512K Byte Flash (FTS512K4) Block Guide	V01	S12FTS512K4V1/D
4K Byte EEPROM (EETS4K) Block Guide	V02	S12EETS4KV2/D
Byte Level Data Link Controller -J1850 (BDLC) Block Guide	V01	S12BDLCV1/D
Freescale Scalable CAN (MSCAN) Block Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG) Block Guide	V01	S12VREGV1/D
Port Integration Module (PIM_9DP256) Block Guide[1]	V03	S12DP256PIMV3/D
Oscillator (OSC) Block Guide	V02	S12OSCV2/D

  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 512K Flash EEPROM
  - 4K byte EEPROM
  - 14K byte RAM
- Two 8-channel Analog-to-Digital Converters
  - 10-bit resolution
  - External conversion trigger capability
- Five 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Enhanced Capture Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Three Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
  - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications

Figure 1-2 MC9S12DP512 Memory Map



* Assuming that a Ô0Õ was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

$0015 - $0016 INT map 1 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

$0017 - $0019 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017-$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$001A - $001B Device ID Register (Table 1-3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020 - $0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATD0CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATD0CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATD0CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATD0CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATD0STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATD0TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATD0TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008B	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008D	ATD0DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$008E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008F	PORTAD0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0090	ATD0DR0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0091	ATD0DR0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0092	ATD0DR1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0093	ATD0DR1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0094	ATD0DR2H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0095	ATD0DR2L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0096	ATD0DR3H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0097	ATD0DR3L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0098	ATD0DR4H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	ATD1CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0121	ATD1CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0122	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0123	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0124	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0125	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0126	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0128	ATD1TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0129	ATD1TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$012A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$012C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012D	ATD1DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012F	PORTAD1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0130	ATD1DR0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0131	ATD1DR0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0132	ATD1DR1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0133	ATD1DR1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0134	ATD1DR2H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0135	ATD1DR2L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0136	ATD1DR3H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0137	ATD1DR3L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0138	ATD1DR4H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0200 - $023F CAN3 (**Freescale** Scalable CAN - **F**SCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$021C - $021F	CAN3IDMR4 - CAN3IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0220 - $022F	CAN3RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-2							
		Write:								
$0230 - $023F	CAN3TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see Table 1-2							

$0240 - $027F PIM (Port Integration Module PIM_9DP256)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0240	PTT	Read: Write:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0242	DDRT	Read: Write:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
$0243	RDRT	Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
$0244	PERT	Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
$0245	PPST	Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
$0246 - $0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTS	Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$024A	DDRS	Read: Write:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
$024B	RDRS	Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
$024C	PERS	Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
$024D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PS7	$\overline{SS0}$	Ñ	Ñ	Ñ	VDDX	PERS/ PPSS	Up	Port S I/O, $\overline{SS}$ of SPI0
PS6	SCK0	Ñ	Ñ	Ñ				Port S I/O, SCK of SPI0
PS5	MOSI0	Ñ	Ñ	Ñ				Port S I/O, MOSI of SPI0
PS4	MISO0	Ñ	Ñ	Ñ				Port S I/O, MISO of SPI0
PS3	TXD1	Ñ	Ñ	Ñ				Port S I/O, TXD of SCI1
PS2	RXD1	Ñ	Ñ	Ñ				Port S I/O, RXD of SCI1
PS1	TXD0	Ñ	Ñ	Ñ				Port S I/O, TXD of SCI0
PS0	RXD0	Ñ	Ñ	Ñ				Port S I/O, RXD of SCI0
PT[7:0]	IOC[7:0]	Ñ	Ñ	Ñ	VDDX	PERT/ PPST	Disabled	Port T I/O, Timer channels

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL ÑOscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{RESET}$ ÑExternal Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST ÑTest Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN ÑVoltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.25 PH3 / KWH3 / $\overline{SS1}$ ÑPort H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.26 PH2 / KWH2 / SCK1 ÑPort H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.27 PH1 / KWH1 / MOSI1 ÑPort H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.28 PH0 / KWH0 / MISO1 ÑPort H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.29 PJ7 / KWJ7 / TXCAN4 / SCL / TXCAN0 ÑPORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for theFreescale Scalable Controller Area Network controller 0 or 4 (CAN0 or CAN4) or the serial clock pin SCL of the IIC module.

2.3.30 PJ6 / KWJ6 / RXCAN4 / SDA / RXCAN0 ÑPORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXCAN for the Freescale Scalable Controller Area Network controller 0 or 4 (CAN 0 or CAN4) or the serial data pin SDA of the IIC module.

2.3.31 PJ[1:0] / KWJ[1:0] ÑPort J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.32 PK7 / $\overline{ECS}$ / ROMCTL ÑPort K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{ECS}$). During MCU normal expanded modes of operation, this pin is

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12DP512. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device (**Section 4.4 Low Power Modes**).

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (Table 4-1). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 means the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PK7 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	0	1	Emulation Expanded Narrow, BDM allowed
			1	0	
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	0	1	Emulation Expanded Wide, BDM allowed
			1	0	
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide.

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{\text{XCLKS}}$	Description
1	Colpitts Oscillator selected
0	Pierce Oscillator/external clock selected

Table 4-3 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

Section 6 HCS12 Core Block Description

6.1 CPU12 Block Description

Consult the HCS12 CPU Reference Manual for information on the CPU.

6.1.1 Device-specific information

When the HCS12 CPU Reference Manual refers to *cycles* this is equivalent to *Bus Clock periods*.
So *1 cycle* is equivalent to *1 Bus Clock period*.

6.2 HCS12 Module Mapping Control (MMC) Block Description

Consult the MMC Block Guide for information on the HCS12 Module Mapping Control module.

6.2.1 Device-specific information

- INITEE
  - Reset state: $01
  - Bits EE11-EE15 are "Write once in Normal and Emulation modes and write anytime in Special modes".
- PPAGE
  - Reset state: $00
  - Register is "Write anytime in all modes"

6.3 HCS12 Multiplexed External Bus Interface (MEBI) Block Description

Consult the MEBI Block Guide for information on HCS12 Multiplexed External Bus Interface module.

6.3.1 Device-specific information

- PUCR
  - Reset state: $90

6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in Table A-7 and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the $\overline{XCLKS}$ signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC} . The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-15 Oscillator Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5	-	16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5	-	40	MHz
2	P	Startup Current	i_{OSC}	100	-	-	µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}	-	8[2]	100[3]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45	-	2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5	-	50	MHz
7	D	External square wave pulse width low [4]	t_{EXTL}	9.5	-	-	ns
8	D	External square wave pulse width high [4]	t_{EXTH}	9.5	-	-	ns
9	D	External square wave rise time [4]	t_{EXTR}	-	-	1	ns
10	D	External square wave fall time [4]	t_{EXTF}	-	-	1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}	-	7	-	pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}	-	1.1	-	V
13	P	EXTAL Pin Input High Voltage [4]	$V_{IH,EXTAL}$	0.75*V_{DDPLL}	-	-	V
	T	EXTAL Pin Input High Voltage [4]	$V_{IH,EXTAL}$	-	-	V_{DDPLL} + 0.3	V
14	P	EXTAL Pin Input Low Voltage [4]	$V_{IL,EXTAL}$	-	-	0.25*V_{SSPLL}	V
	T	EXTAL Pin Input Low Voltage [4]	$V_{IL,EXTAL}$	V_{SSPLL} - 0.3	-	-	V
15	C	EXTAL Pin Input Hysteresis [4]	$V_{HYS,EXTAL}$	-	250	-	mV