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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dp512cpve

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.16	31 Mar 2003	31 Mar 2003		- Corrections in App. A 'NVM, Flash and EEPROM': - Number of words per flash row = 64 - Replaced 'burst programming' with 'row programming' - Sector erase size = 1024 bytes - Corrected feature description ECT - Corrected min. bus freq. in table 'Operating Conditions'
V01.17	30 May 2003	30 May 2003		- Replaced references to HCS12 Core Guide with the individual HCS12 Block guides throughout document - Table 'Absolute Maximum Ratings' corrected footnote on clamp of TEST pin
V01.18	23 Jul 2003	23 Jul 2003		- Mentioned 'S12 LRAE' bootloader in Flash section - Document References: corrected S12 CPU document reference
V01.19	24 Jul 2003	24 Jul 2003		- Added part ID for 2L00M maskset.
V01.20	01 Sep 2003	01 Sep 2003		- Added part ID for 3L00M maskset. - Added cycle definition to 'CPU 12 Block Description'. - Diagram 'Clock Connections': Connected Bus Clock to HCS12 Core. - Corrected 'Background Debug Module' to 'HCS12 Breakpoint' at address \$0028 - \$002F in table 1-1. - Corrected 'Blank Check Time Flash' value in table 'NVM Timing Characteristics' - Added EXTAL pin VIH, VIL and EXTAL pin hysteresis value to 'Oscillator Characteristics'. Updated oscillator description and table note.
V01.21	08 Mar 2004	08 Mar 2004		- Added part ID for 4L00M maskset. - Corrected pin name KWP5 in device pinout.
V01.22	23 Aug 2004	23 Aug 2004		- Updated $V_{IH,EXTAL}$ and $V_{IL,EXTAL}$ in table 'Oscillator Characteristics' - Removed item 'Oscillator' from table 'Operating Conditions' as already covered in table 'Oscillator Characteristics'
V01.23	09 Feb 2005	09 Feb 2005		- Corrected Flash Row Programming Time in NVM Timing Characteristics
V01.24	01 Apr 2005	01 Apr 2005		- Changed T_{Javg} and added footnote to data retention time in NVM Reliability Characteristics
V01.25	05 Jul 2005	05 Jul 2005		- Updated NVM Reliability Characteristics

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Section 1 Introduction

1.1 Overview

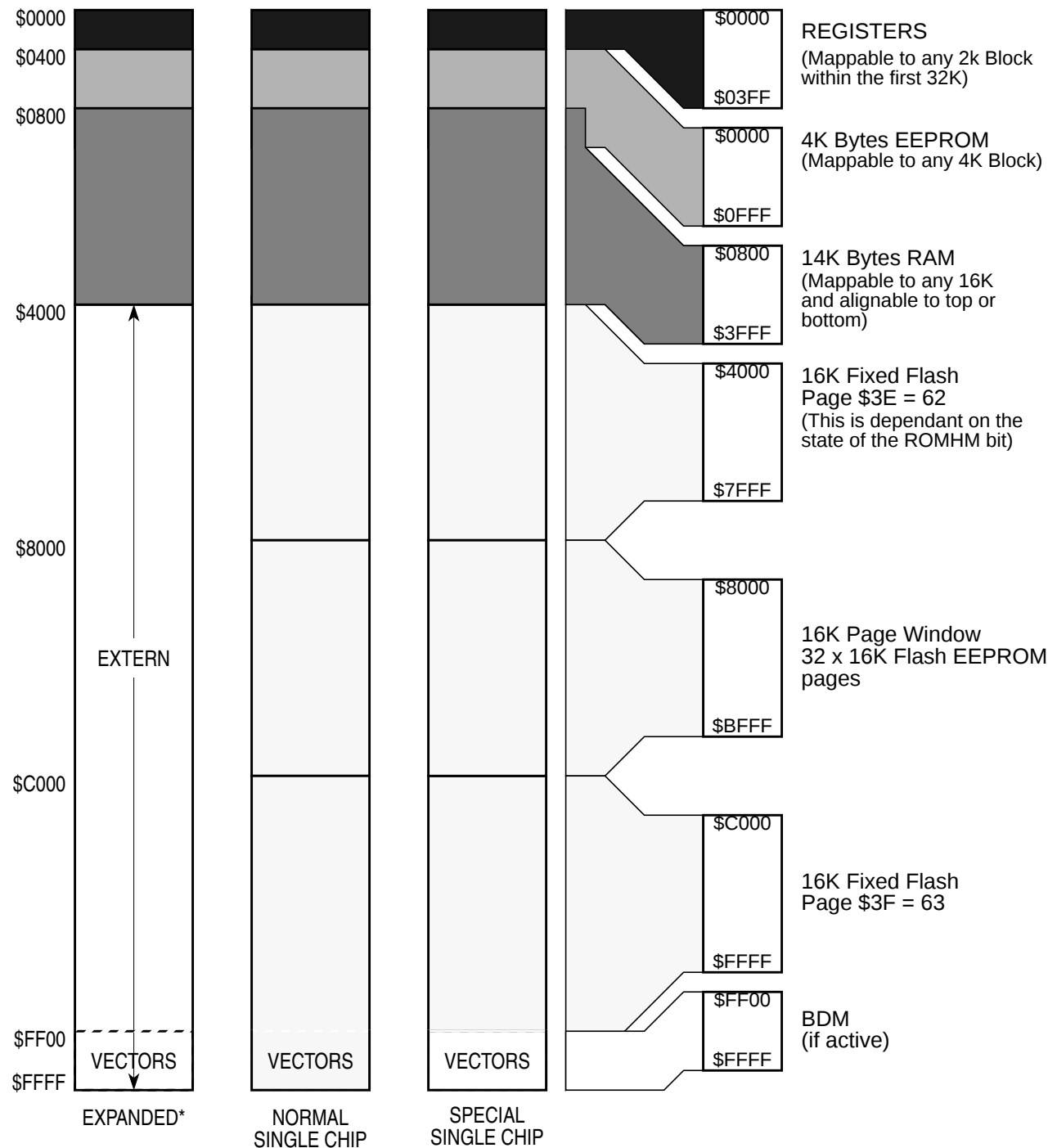
The MC9S12DP512 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 512K bytes of Flash EEPROM, 14K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), three serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wake up capability, five CAN 2.0 A, B software compatible modules (MSCAN12), and an Inter-IC Bus. The MC9S12DP512 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
 - 16-bit HCS12 CPU
 - i. Upward compatible with M68HC11 instruction set
 - ii. Interrupt stacking and programmer's model identical to M68HC11
 - iii. Instruction queue
 - iv. Enhanced indexed addressing
 - MEBI (Multiplexed External Bus Interface)
 - MMC (Module Mapping Control)
 - INT (Interrupt control)
 - BKP (Breakpoints)
 - BDM (Background Debug Mode)
- CRG (Clock and Reset Generation)
 - Low current Colpitts oscillator or
 - Pierce oscillator
 - PLL
 - COP watchdog
 - Real Time Interrupt
 - Clock Monitor
- 8-bit and 4-bit ports with interrupt functionality

- Digital filtering
 - Programmable rising or falling edge trigger
 - Memory
 - 512K Flash EEPROM
 - 4K byte EEPROM
 - 14K byte RAM
 - Two 8-channel Analog-to-Digital Converters
 - 10-bit resolution
 - External conversion trigger capability
 - Five 1M bit per second, CAN 2.0 A, B software compatible modules
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
 - Enhanced Capture Timer
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels
 - Four 8-bit or two 16-bit pulse accumulators
 - 8 PWM channels
 - Programmable period and duty cycle
 - 8-bit 8-channel or 16-bit 4-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
 - Usable as interrupt inputs
 - Serial interfaces
 - Two asynchronous Serial Communications Interfaces (SCI)
 - Three Synchronous Serial Peripheral Interface (SPI)
 - Byte Data Link Controller (BDLC)
 - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
-

Figure 1-2 MC9S12DP512 Memory Map



* Assuming that a '0' was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

\$0015 - \$0016**INT map 1 of 2 (HCS12 Interrupt)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
\$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

\$0017 - \$0019**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0017-\$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$001A - \$001B**Device ID Register (Table 1-3)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
\$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

\$001C - \$001D**MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-4)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
\$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

\$001E - \$001E**MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

\$001F - \$001F**INT map 2 of 2 (HCS12 Interrupt)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

\$0020 - \$0027**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0020 - \$0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

Table 1-2 Detailed FSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
\$xx13	CANxTIDR3	Write:								
	Standard ID	Read:								
		Write:								
\$xx14 - \$xx1B	CANxTDSR0 - CANxTDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
\$xx1C	CANxTDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
\$xx1D	CANxTTBPR	Read:	PRI07	PRI06	PRI05	PRI04	PRI03	PRI02	PRI01	PRI00
		Write:								
\$xx1E	CANxTTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
\$xx1F	CANxTTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

\$0180 - \$01BF**CAN1 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0185	CAN1RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$018C - \$018D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$018E	CAN1RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$018F	CAN1TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0190 - \$0193	CAN1IDAR0 - CAN1IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								

\$0240 - \$027F**PIM (Port Integration Module PIM_9DP256)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$026D	PPSJ	Read:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
		Write:								
\$026E	PIEJ	Read:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
		Write:								
\$026F	PIFJ	Read:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
		Write:								
\$0270 - \$027F	Reserved	Read:								

\$0280 - \$02BF**CAN4 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0280	CAN4CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0281	CAN4CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0282	CAN4BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0283	CAN4BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0284	CAN4RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRI1	RXF
		Write:								
\$0285	CAN4RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0286	CAN4TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0287	CAN4TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0288	CAN4TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0289	CAN4TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$028A	CAN4TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$028B	CAN4IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$028C - \$028D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$028E	CAN4RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$028F	CAN4TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0290 - \$0293	CAN4IDAR0 - CAN4IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0294 - \$0297	CAN4IDMR0 - CAN4IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0298 - \$029B	CAN4IDAR4 - CAN4IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								

\$0280 - \$02BF**CAN4 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$029C -	CAN4IDMR4 -	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
\$029F	CAN4IDMR7	Write:								
\$02A0 -	CAN4RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-2							
\$02AF		Write:								
\$02B0 -	CAN4TXFG	Read:	FOREGROUND TRANSMIT BUFFER see Table 1-2							
\$02BF		Write:								

\$02C0 - \$03FF**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$02C0 -	Reserved	Read:	0	0	0	0	0	0	0	0
\$03FF		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses \$001A and \$001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-3** shows the assigned part ID number.

Table 1-3 Assigned Part ID Numbers

Device	Mask Set Number	Part ID ¹
MC9S12DP512	0L00M	\$0400
MC9S12DP512	1L00M	\$0401
MC9S12DP512	2L00M	\$0402
MC9S12DP512	3L00M	\$0403
MC9S12DP512	4L00M	\$0404

NOTES:

1. The coding is as follows:

Bit 15 - 12: Major family identifier

Bit 11 - 8: Minor family identifier

Bit 7 - 4: Major mask set revision number including FAB transfers

Bit 3 - 0: Minor - non full - mask set revision

1.7 Memory Size Assignments

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses \$001C and \$001D after reset). **Table 1-4** shows the read-only values of these registers. Refer to HCS12 Module Mapping Control (MMC) Block Guide for further details.

Table 1-4 Memory size registers

Register name	Value
MEMSIZ0	\$26
MEMSIZ1	\$82

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PS7	SS0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, $\overline{SS}$ of SPI0
PS6	SCK0	—	—	—				Port S I/O, SCK of SPI0
PS5	MOSI0	—	—	—				Port S I/O, MOSI of SPI0
PS4	MISO0	—	—	—				Port S I/O, MISO of SPI0
PS3	TXD1	—	—	—				Port S I/O, TXD of SCI1
PS2	RXD1	—	—	—				Port S I/O, RXD of SCI1
PS1	TXD0	—	—	—				Port S I/O, TXD of SCI0
PS0	RXD0	—	—	—				Port S I/O, RXD of SCI0
PT[7:0]	IOC[7:0]	—	—	—	VDDX	PERT/ PPST	Disabled	Port T I/O, Timer channels

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{RESET}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: The TEST pin must be tied to VSS in all applications.

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

NOTE: All VSS pins must be connected together in the application.

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: No load allowed except for bypass capacitors.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: No load allowed except for bypass capacitors.

6.5 HCS12 Background Debug (BDM) Block Description

Consult the BDM Block Guide for information on the HCS12 Background Debug module.

6.5.1 Device-specific information

When the BDM Block Guide refers to *alternate clock* this is equivalent to *Oscillator Clock*.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block Guide for information on the HCS12 Breakpoint module.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

The Low Voltage Reset feature of the CRG is not available on this device.

Section 8 Oscillator (OSC) Block Description

8.1 Device-specific information

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 9 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block Guide for information about the Enhanced Capture Timer module.

When the ECT_16B8C Block Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 10 Analog to Digital Converter (ATD) Block Description

Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Freescale and are subject to change without notice.*

This supplement contains the most accurate electrical information for the MC9S12DP512 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification is shown in the column labeled “C” in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12DP512 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator, PLL and internal logic.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply.
The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA} .
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL} .
5. This pin is clamped low to V_{SSX} , but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at $T_A = 125^\circ\text{C}$ positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at $T_A = 27^\circ\text{C}$ positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J . For power dissipation calculations refer to **Section A.1.8 Power Dissipation and Thermal Characteristics**.

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.25	V
Digital Logic Supply Voltage ¹	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage ⁽¹⁾	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	ΔV_{DDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	ΔV_{SSX}	-0.1	0	0.1	V
Bus Frequency (MC9S12DP512C, V, M)	f_{bus}	0.25 ²	-	25	MHz
MC9S12DP512C					
Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range ³	T_A	-40	27	85	°C
MC9S12DP512V					
Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range ⁽³⁾	T_A	-40	27	105	°C
MC9S12DP512M					
Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range ⁽³⁾	T_A	-40	27	125	°C

NOTES:

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J .

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

Table A-6 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input High Voltage	V_{IH}	$0.65 \cdot V_{DD5}$	-	-	V
	T	Input High Voltage	V_{IH}	-	-	$V_{DD5} + 0.3$	V
2	P	Input Low Voltage	V_{IL}	-	-	$0.35 \cdot V_{DD5}$	V
	T	Input Low Voltage	V_{IL}	$V_{SS5} - 0.3$	-	-	V
3	C	Input Hysteresis	V_{HYS}	-	250	-	mV
4	P	Input Leakage Current (pins in high impedance input mode) $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	-1	-	1	μA
5	P	Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2mA$ Full Drive $I_{OH} = -10mA$	V_{OH}	$V_{DD5} - 0.8$	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +2mA$ Full Drive $I_{OL} = +10mA$	V_{OL}	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	-130	μA
8	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	μA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	μA
10	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	μA
11	D	Input Capacitance	C_{in}	-	6	-	pF
12	T	Injection current ¹ Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered ²	t_{PIGN}	-	-	3	μs
14	P	Port H, J, P Interrupt Input Pulse passed ⁽²⁾	t_{PVAL}	10	-	-	μs

NOTES:

1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.7 SPI

This section provides electrical parametrics and ratings for the SPI.

In **Table A-18** the measurement conditions are listed.

Table A-18 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD} , on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) V_{DDX}	V

A.7.1 Master Mode

In **Figure A-6** the timing diagram for master mode with transmission format $CPHA=0$ is depicted.

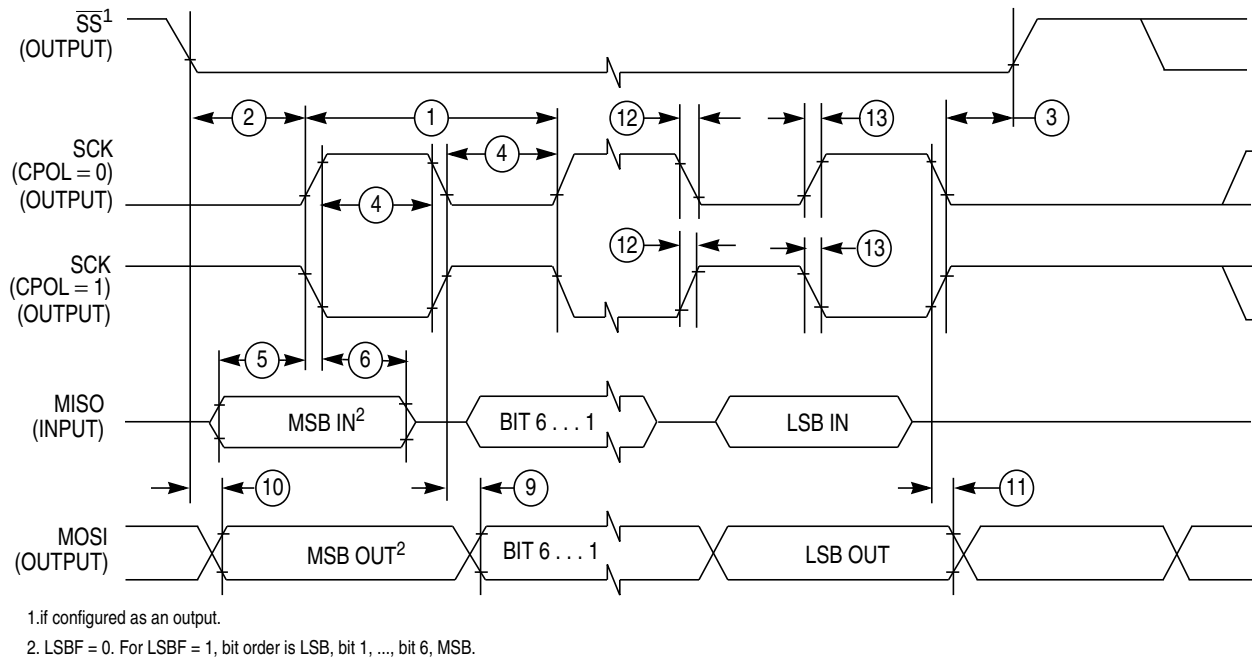


Figure A-6 SPI Master Timing (CPHA=0)

In **Figure A-7** the timing diagram for master mode with transmission format $CPHA=1$ is depicted.

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-10** with the actual timing values shown on table **Table A-21**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

