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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dp512cpver

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	27 Nov 2001	11 Feb 2002		- Initial version based on DP256 V2.09.
V01.01	13 Mar 2002	13 Mar 2002		- Updated document formats. - Removed reference to SIM in overview. - Changed XCLKS to PE7 in signal description. - Removed "Oscillator start-up time from POR or STOP" from Oscillator Characteristics. - Changed VDD and VDDPLL to 2.35V. - Updated C _{INS} . - Updated I _{OL} /I _{OH} values. - Updated input capacitance. - Updated NVM timing characteristics.
V01.02	02 Apr 2002	02 Apr 2002		- Updated document reference (SPI, SCI).
V01.03	15 Apr 2002	15 Apr 2002		- Corrected values in device memory map (RAM start, flash protected sector sizes). - Updated document reference (SCI).
V01.04	06 Jun 2002	06 Jun 2002		- Changed all operating frequency references to 50MHz XTAL and removed references to 80 pin LQFP.
V01.05	05 Jul 2002	05 Jul 2002		- Preface Table "Document References": Changed to full naming for each block. - Table "Interrupt Vector Locations", Column "Local Enable": Corrected several register and bit names. - Table "Signal Properties": Added column "Internal Pull Resistor". - Table "PLL Characteristics": Updated parameters K1 and f1 - Figure "Basic PLL functional diagram": Inserted XFC pin in diagram - Enhanced section "XFC Component Selection" - Added to Sections ATD, ECT and PWM: freeze mode = active BDM mode.

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Figure 1-1 MC9S12DP512 Block Diagram

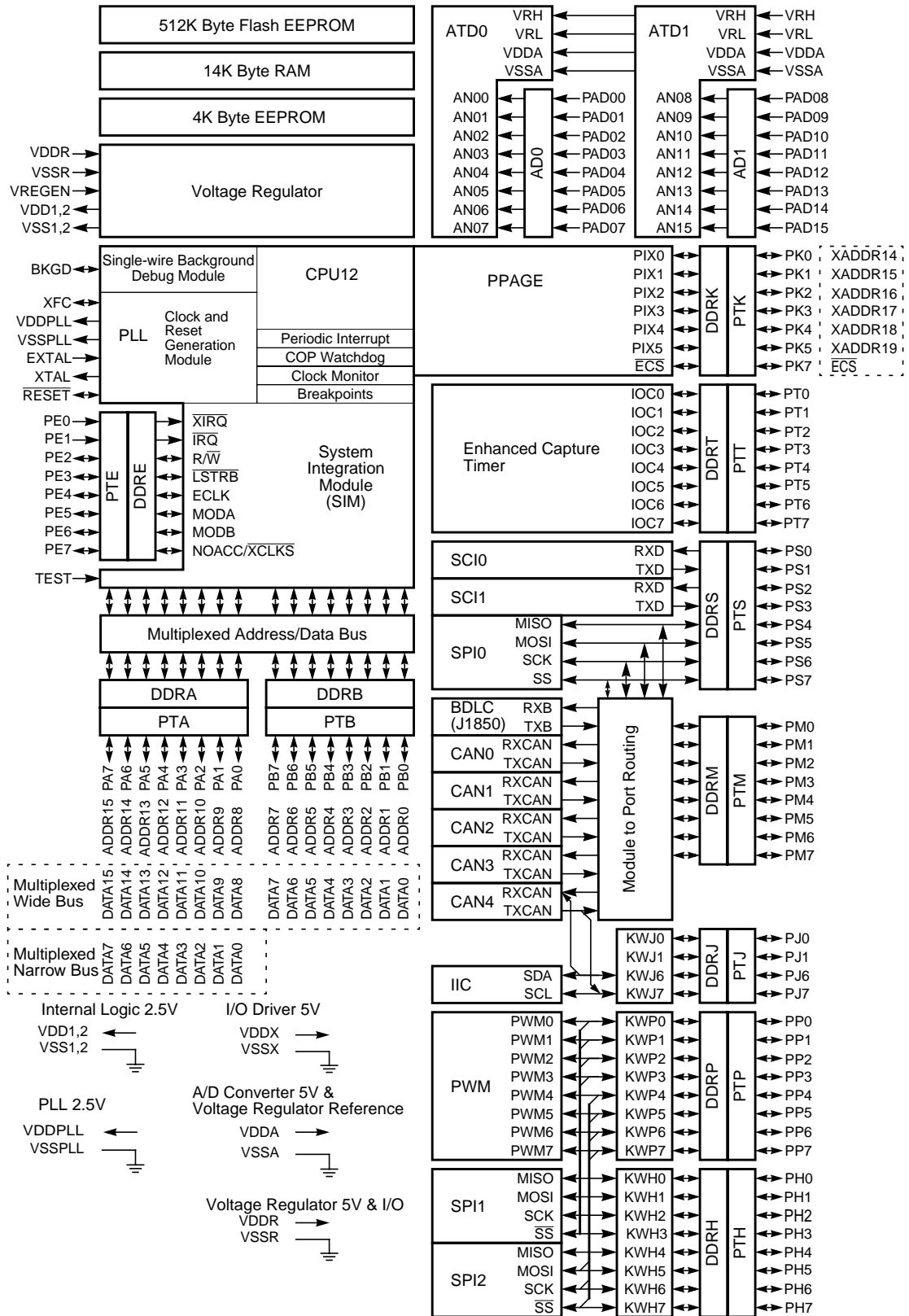


Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
\$8000 - \$BFFF	Flash EEPROM Page Window	16384
\$C000 - \$FFFF	Fixed Flash EEPROM array incl. 2K, 4K, 8K or 16K Protected Sector at end and 256 bytes of Vector Space at \$FF80 - \$FFFF	16384

1.5.1 Detailed Register Map

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0000	PORTA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0001	PORTB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0002	DDRA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0003	DDRB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0004 - \$0007	Reserved	Read: Write:	0	0	0	0	0	0	0	0
\$0008	PORTE	Read: Write:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
\$0009	DDRE	Read: Write:	Bit 7	6	5	4	3	Bit 2	0	0
\$000A	PEAR	Read: Write:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
\$000B	MODE	Read: Write:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
\$000C	PUCR	Read: Write:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
\$000D	RDRIV	Read: Write:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
\$000E	EBICTL	Read: Write:	0	0	0	0	0	0	0	ESTR
\$000F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0010	INITRM	Read: Write:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
\$0011	INITRG	Read: Write:	0	REG14	REG13	REG12	REG11	0	0	0
\$0012	INITEE	Read: Write:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
\$0013	MISC	Read: Write:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
\$0014	Reserved	Read: Write:	0	0	0	0	0	0	0	0

\$0015 - \$0016

INT map 1 of 2 (HCS12 Interrupt)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0015	ITCR	Read: 0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:							
\$0016	ITEST	Read: INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:							

\$0017 - \$0019

Reserved

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0017-\$0019	Reserved	Read: 0	0	0	0	0	0	0	0
		Write:							

\$001A - \$001B

Device ID Register (Table 1-3)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001A	PARTIDH	Read: ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:							
\$001B	PARTIDL	Read: ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:							

\$001C - \$001D

MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-4)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001C	MEMSIZ0	Read: reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:							
\$001D	MEMSIZ1	Read: rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:							

\$001E - \$001E

MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001E	INTCR	Read: IRQE	IRQEN	0	0	0	0	0	0
		Write:							

\$001F - \$001F

INT map 2 of 2 (HCS12 Interrupt)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001F	HPRIO	Read: PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:							

\$0020 - \$0027

Reserved

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0020 - \$0027	Reserved	Read: 0	0	0	0	0	0	0	0
		Write:							

2.3.47 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.48 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.49 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.50 PS7 / \overline{SS} — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin \overline{SS} of the Serial Peripheral Interface 0 (SPI0).

2.3.51 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.52 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.53 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.54 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.55 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.56 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.57 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.58 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12DP512 power and ground pins are described below.

Table 2-2 MC9S12DP512 Power and Ground Connection Summary

Mnemonic	Pin Number	Nominal Voltage	Description
	112-pin QFP		
$V_{DD1,2}$	13, 65	2.5 V	Internal power and ground generated by internal regulator
$V_{SS1,2}$	14, 66	0V	
V_{DDR}	41	5.0 V	External power and ground, supply to pin drivers and internal voltage regulator.
V_{SSR}	40	0 V	
V_{DDX}	107	5.0 V	External power and ground, supply to pin drivers.
V_{SSX}	106	0 V	
V_{DDA}	83	5.0 V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
V_{SSA}	86	0 V	
V_{RL}	85	0 V	Reference voltages for the analog-to-digital converter.
V_{RH}	84	5.0 V	
V_{DDPLL}	43	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
V_{SSPLL}	45	0 V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules.

Figure 3-1 shows the clock connections from the CRG to all modules.

Consult the CRG Block Guide and OSC Block Guide for details on clock generation.

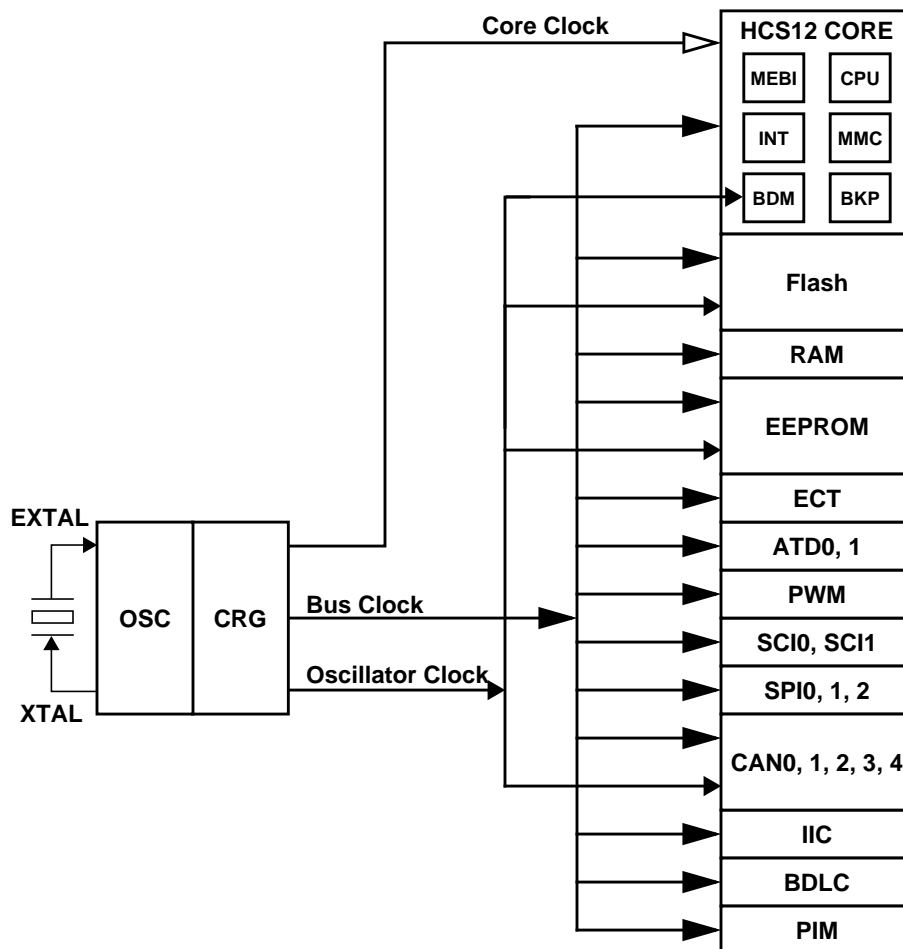


Figure 3-1 Clock Connections

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the CPU12 Reference Manual for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
\$FFFE, \$FFFF	Reset	None	None	–
\$FFFC, \$FFFD	Clock Monitor fail reset	None	PLLCTL (CME, SCME)	–
\$FFFA, \$FFFB	COP failure reset	None	COP rate select	–
\$FFF8, \$FFF9	Unimplemented instruction trap	None	None	–
\$FFF6, \$FFF7	SWI	None	None	–
\$FFF4, \$FFF5	XIRQ	X-Bit	None	–
\$FFF2, \$FFF3	IRQ	I-Bit	IRQCR (IRQEN)	\$F2
\$FFF0, \$FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	\$F0
\$FFEE, \$FFEF	Enhanced Capture Timer channel 0	I-Bit	TIE (C0I)	\$EE
\$FFEC, \$FFED	Enhanced Capture Timer channel 1	I-Bit	TIE (C1I)	\$EC
\$FFEA, \$FFEB	Enhanced Capture Timer channel 2	I-Bit	TIE (C2I)	\$EA
\$FFE8, \$FFE9	Enhanced Capture Timer channel 3	I-Bit	TIE (C3I)	\$E8
\$FFE6, \$FFE7	Enhanced Capture Timer channel 4	I-Bit	TIE (C4I)	\$E6
\$FFE4, \$FFE5	Enhanced Capture Timer channel 5	I-Bit	TIE (C5I)	\$E4
\$FFE2, \$FFE3	Enhanced Capture Timer channel 6	I-Bit	TIE (C6I)	\$E2
\$FFE0, \$FFE1	Enhanced Capture Timer channel 7	I-Bit	TIE (C7I)	\$E0
\$FFDE, \$FFDF	Enhanced Capture Timer overflow	I-Bit	TSRC2 (TOI)	\$DE
\$FFDC, \$FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	\$DC
\$FFDA, \$FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	\$DA
\$FFD8, \$FFD9	SPI0	I-Bit	SPICR1 (SPIE, SPTIE)	\$D8
\$FFD6, \$FFD7	SCI0	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	\$D6
\$FFD4, \$FFD5	SCI1	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	\$D4
\$FFD2, \$FFD3	ATD0	I-Bit	ATDCTL2 (ASCIE)	\$D2
\$FFD0, \$FFD1	ATD1	I-Bit	ATDCTL2 (ASCIE)	\$D0
\$FFCE, \$FFCF	Port J	I-Bit	PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0)	\$CE
\$FFCC, \$FFCD	Port H	I-Bit	PIEH (PIEH7-0)	\$CC

Section 6 HCS12 Core Block Description

6.1 CPU12 Block Description

Consult the HCS12 CPU Reference Manual for information on the CPU.

6.1.1 Device-specific information

When the HCS12 CPU Reference Manual refers to *cycles* this is equivalent to *Bus Clock periods*. So *1 cycle* is equivalent to *1 Bus Clock period*.

6.2 HCS12 Module Mapping Control (MMC) Block Description

Consult the MMC Block Guide for information on the HCS12 Module Mapping Control module.

6.2.1 Device-specific information

- INITEE
 - Reset state: \$01
 - Bits EE11-EE15 are "Write once in Normal and Emulation modes and write anytime in Special modes".
- PPAGE
 - Reset state: \$00
 - Register is "Write anytime in all modes"

6.3 HCS12 Multiplexed External Bus Interface (MEBI) Block Description

Consult the MEBI Block Guide for information on HCS12 Multiplexed External Bus Interface module.

6.3.1 Device-specific information

- PUCR
 - Reset state: \$90

6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins. The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

Table A-6 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input High Voltage	V_{IH}	$0.65 \cdot V_{DD5}$	-	-	V
	T	Input High Voltage	V_{IH}	-	-	$V_{DD5} + 0.3$	V
2	P	Input Low Voltage	V_{IL}	-	-	$0.35 \cdot V_{DD5}$	V
	T	Input Low Voltage	V_{IL}	$V_{SS5} - 0.3$	-	-	V
3	C	Input Hysteresis	V_{HYS}	-	250	-	mV
4	P	Input Leakage Current (pins in high impedance input mode) $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	-1	-	1	μA
5	P	Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2mA$ Full Drive $I_{OH} = -10mA$	V_{OH}	$V_{DD5} - 0.8$	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +2mA$ Full Drive $I_{OL} = +10mA$	V_{OL}	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	-130	μA
8	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	μA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	μA
10	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	μA
11	D	Input Capacitance	C_{in}	-	6	-	pF
12	T	Injection current ¹ Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered ²	t_{PIGN}	-	-	3	μs
14	P	Port H, J, P Interrupt Input Pulse passed ⁽²⁾	t_{PVAL}	10	-	-	μs

NOTES:

1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq 1\text{LSB}$, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of \$3FF (\$FF in 8-bit mode) for analog inputs greater than V_{RH} and \$000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9 ATD Electrical Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Max input Source Resistance	R_S	-	-	1	K Ω
2	T	Total Input Capacitance Non Sampling Sampling	C_{INN} C_{INS}	-	-	10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5	-	2.5	mA
4	C	Coupling Ratio positive current injection	K_p	-	-	10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n	-	-	10^{-2}	A/A

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in Table A-4 unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB	-	5	-	mV
2	P	10-Bit Differential Nonlinearity	DNL	-1	-	1	Counts
3	P	10-Bit Integral Nonlinearity	INL	-2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error ¹	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB	-	20	-	mV
6	P	8-Bit Differential Nonlinearity	DNL	-0.5	-	0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	-1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error ⁽¹⁾	AE	-1.5	±1.0	1.5	Counts

NOTES:

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^n DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

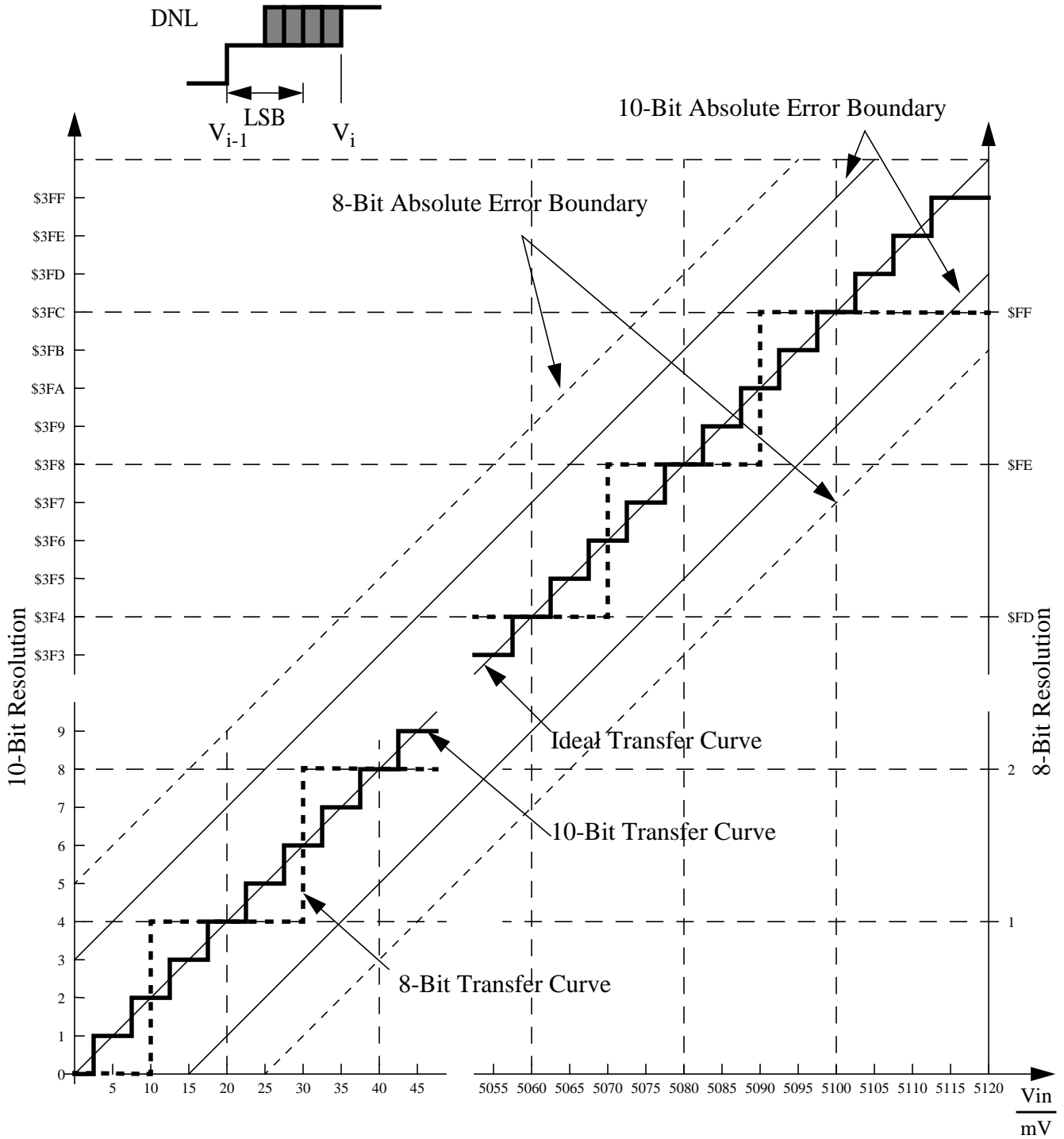


Figure A-1 ATD Accuracy Definitions

NOTE: Figure A-1 shows only definitions, for specification values refer to **Table A-10**.

A.4 Voltage Regulator

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed.

Table A-13 Voltage Regulator Recommended Load Capacitances

Rating	Symbol	Min	Typ	Max	Unit
Load Capacitance on VDD1, 2	C_{LVDD}	-	220	-	nF
Load Capacitance on VDDPLL	$C_{LVDDfcPLL}$	-	220	-	nF

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-16 PLL Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Self Clock Mode frequency	f_{SCM}	1	-	5.5	MHz
2	D	VCO locking range	f_{VCO}	8	-	50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$ \Delta_{trk} $	3	-	4	% ¹
4	D	Lock Detection	$ \Delta_{Lock} $	0	-	1.5	% ⁽¹⁾
5	D	Un-Lock Detection	$ \Delta_{unt} $	0.5	-	2.5	% ⁽¹⁾
6	D	Lock Detector transition from Tracking to Acquisition mode	$ \Delta_{unt} $	6	-	8	% ⁽¹⁾
7	C	PLLON Total Stabilization delay (Auto Mode) ²	t_{stab}	-	0.5	-	ms
8	D	PLLON Acquisition mode stabilization delay ⁽²⁾	t_{acq}	-	0.3	-	ms
9	D	PLLON Tracking mode stabilization delay ⁽²⁾	t_{al}	-	0.2	-	ms
10	D	Fitting parameter VCO loop gain	K_1	-	-100	-	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1	-	60	-	MHz
12	D	Charge pump current acquisition mode	$ i_{ch} $	-	38.5	-	μA
13	D	Charge pump current tracking mode	$ i_{ch} $	-	3.5	-	μA
14	C	Jitter fit parameter 1 ⁽²⁾	j_1	-	-	1.1	%
15	C	Jitter fit parameter 2 ⁽²⁾	j_2	-	-	0.13	%

NOTES:

1. % deviation from target frequency

2. $f_{OSC} = 4\text{MHz}$, $f_{BUS} = 25\text{MHz}$ equivalent $f_{VCO} = 50\text{MHz}$: REFDV = #03, SYNRR = #018, Cs = 4.7nF, Cp = 470pF, Rs = 10K Ω .

