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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dp512mpve

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	27 Nov 2001	11 Feb 2002		- Initial version based on DP256 V2.09.
V01.01	13 Mar 2002	13 Mar 2002		- Updated document formats. - Removed reference to SIM in overview. - Changed XCLKS to PE7 in signal description. - Removed "Oscillator start-up time from POR or STOP" from Oscillator Characterisitcs. - Changed VDD and VDDPLL to 2.35V. - Updated C_{INS}. - Updated I_{OL}/I_{OH} values. - Updated input capacitance. - Updated NVM timing characteristics.
V01.02	02 Apr 2002	02 Apr 2002		- Updated document reference (SPI, SCI).
V01.03	15 Apr 2002	15 Apr 2002		- Corrected values in device memory map (RAM start, flash protected sector sizes). - Updated document reference (SCI).
V01.04	06 Jun 2002	06 Jun 2002		- Changed all operating frequency references to 50MHz EXTAL and removed references to 80 pin LQFP.
V01.05	05 Jul 2002	05 Jul 2002		- Preface Table "Document References": Changed to full naming for each block. - Table "Interrupt Vector Locations", Column "Local Enable": Corrected several register and bit names. - Table "Signal Properties": Added column "Internal Pull Resistor". - Table "PLL Characteristics": Updated parameters K1 and f1 - Figure "Basic Pll functional diagram": Inserted XFC pin in diagram - Enhanced section "XFC Component Selection" - Added to Sections ATD, ECT and PWM: freeze mode = active BDM mode.

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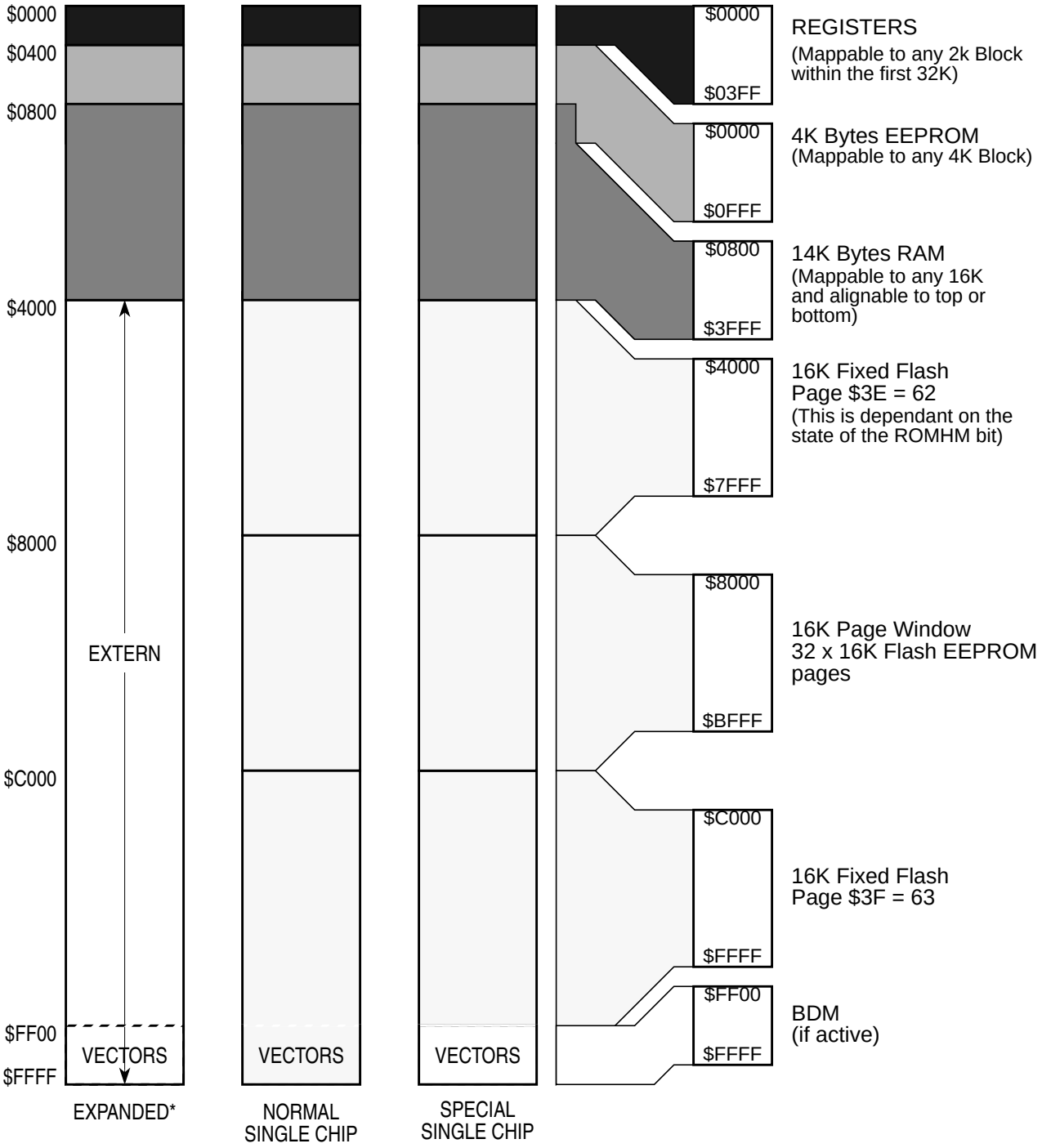
Appendix A Electrical Characteristics

Figure 1-2 MC9S12DP512 Memory Map



* Assuming that a '0' was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	ATD1CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0121	ATD1CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0122	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0123	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0124	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0125	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0126	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0128	ATD1TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0129	ATD1TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$012A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$012C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012D	ATD1DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012F	PORTAD1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0130	ATD1DR0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0131	ATD1DR0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0132	ATD1DR1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0133	ATD1DR1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0134	ATD1DR2H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0135	ATD1DR2L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0136	ATD1DR3H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0137	ATD1DR3L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0138	ATD1DR4H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0180 - $01BF CAN1 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0194 - $0197	CAN1IDMR0 - CAN1IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0198 - $019B	CAN1IDAR4 - CAN1IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019C - $019F	CAN1IDMR4 - CAN1IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01A0 - $01AF	CAN1RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$01B0 - $01BF	CAN1TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

$01C0 - $01FF CAN2 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01C0	CAN2CTL0	Read: Write:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
$01C1	CAN2CTL1	Read: Write:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
$01C2	CAN2BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$01C3	CAN2BTR1	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$01C4	CAN2RFLG	Read: Write:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
$01C5	CAN2RIER	Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$01C6	CAN2TFLG	Read: Write:	0	0	0	0	0	TXE2	TXE1	TXE0
$01C7	CAN2TIER	Read: Write:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
$01C8	CAN2TARQ	Read: Write:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
$01C9	CAN2TAAK	Read: Write:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
$01CA	CAN2TBSEL	Read: Write:	0	0	0	0	0	TX2	TX1	TX0
$01CB	CAN2IDAC	Read: Write:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
$01CC - $01CD	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$01CE	CAN2RXERR	Read: Write:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
$01CF	CAN2TXERR	Read: Write:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
$01D0 - $01D3	CAN2IDAR0 - CAN2IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D4 - $01D7	CAN2IDMR0 - CAN2IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0

$0240 - $027F PIM (Port Integration Module PIM_9DP256)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0257	MODRR	Read:	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		Write:								
$0258	PTP	Read:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$025E	PIEP	Read:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		Write:								
$025F	PIFP	Read:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		Write:								
$0260	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$0263	RDRH	Read:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$0264	PERH	Read:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$0265	PPSH	Read:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$0266	PIEH	Read:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$0267	PIFH	Read:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0268	PTJ	Read:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
		Write:								
$0269	PTIJ	Read:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
		Write:								
$026A	DDRJ	Read:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
		Write:								
$026B	RDRJ	Read:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
		Write:								
$026C	PERJ	Read:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
		Write:								

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block Guides of the individual IP blocks on the device.

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PH7	KWH7	$\overline{SS2}$	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, $\overline{SS}$ of SPI2
PH6	KWH6	SCK2	—	—				Port H I/O, Interrupt, SCK of SPI2
PH5	KWH5	MOSI2	—	—				Port H I/O, Interrupt, MOSI of SPI2
PH4	KWH4	MISO2	—	—				Port H I/O, Interrupt, MISO of SPI2
PH3	KWH3	$\overline{SS1}$	—	—				Port H I/O, Interrupt, $\overline{SS}$ of SPI1
PH2	KWH2	SCK1	—	—				Port H I/O, Interrupt, SCK of SPI1
PH1	KWH1	MOSI1	—	—				Port H I/O, Interrupt, MOSI of SPI1
PH0	KWH0	MISO1	—	—				Port H I/O, Interrupt, MISO of SPI1
PJ7	KWJ7	TXCAN4	SCL	TXCAN0	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC, TX of CAN0
PJ6	KWJ6	RXCAN4	SDA	RXCAN0				Port J I/O, Interrupt, RX of CAN4, SDA of IIC, RX of CAN0
PJ[1:0]	KWJ[1:0]	—	—	—				Port J I/O, Interrupts
PK7	$\overline{ECS}$	ROMCTL	—	—	VDDX	PUCR/ PUPKE	Up	Port K I/O, Emulation Chip Select, ROM Control
PK[5:0]	XADDR [19:14]	—	—	—				Port K I/O, Extended Addresses
PM7	TXCAN3	TXCAN4	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of CAN3, TX of CAN4
PM6	RXCAN3	RXCAN4	—	—				Port M I/O, RX of CAN3, RX of CAN4
PM5	TXCAN2	TXCAN0	TXCAN4	SCK0				Port M I/O, TX of CAN2, CAN0, CAN4, SCK of SPI0
PM4	RXCAN2	RXCAN0	RXCAN4	MOSI0				Port M I/O, RX of CAN2, CAN0, CAN4, MOSI of SPI0
PM3	TXCAN1	TXCAN0	—	$\overline{SS0}$				Port M I/O, TX of CAN1, CAN0, $\overline{SS}$ of SPI0
PM2	RXCAN1	RXCAN0	—	MISO0				Port M I/O, RX of CAN1, CAN0, MISO of SPI0
PM1	TXCAN0	TXB	—	—				Port M I/O, TX of CAN0, RX of BDLC
PM0	RXCAN0	RXB	—	—				Port M I/O, RX of CAN0, RX of BDLC
PP7	KWP7	PWM7	SCK2	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 7 of PWM, SCK of SPI2
PP6	KWP6	PWM6	$\overline{SS2}$	—				Port P I/O, Interrupt, Channel 6 of PWM, $\overline{SS}$ of SPI2
PP5	KWP5	PWM5	MOSI2	—				Port P I/O, Interrupt, Channel 5 of PWM, MOSI of SPI2
PP4	KWP4	PWM4	MISO2	—				Port P I/O, Interrupt, Channel 4 of PWM, MISO2 of SPI2
PP3	KWP3	PWM3	$\overline{SS1}$	—				Port P I/O, Interrupt, Channel 3 of PWM, $\overline{SS}$ of SPI1
PP2	KWP2	PWM2	SCK1	—				Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1
PP1	KWP1	PWM1	MOSI1	—				Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1
PP0	KWP0	PWM0	MISO1	—				Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

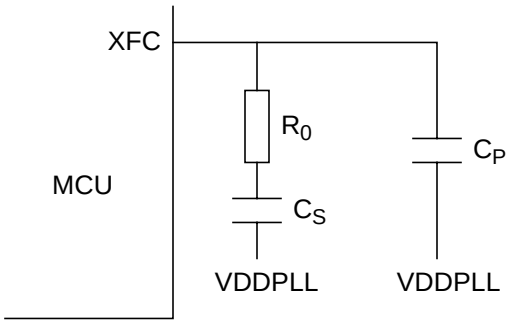


Figure 2-2 PLL Loop Filter Connections

2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin has a permanently enabled pull-up device.

2.3.7 PAD15 / AN15 / ETRIG1 — Port AD Input Pin of ATD1

PAD15 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

2.3.8 PAD[14:08] / AN[14:08] — Port AD Input Pins of ATD1

PAD14 - PAD08 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD1.

2.3.9 PAD7 / AN07 / ETRIG0 — Port AD Input Pin of ATD0

PAD7 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.10 PAD[06:00] / AN[06:00] — Port AD Input Pins of ATD0

PAD06 - PAD00 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD0.

2.3.47 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.48 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.49 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.50 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.51 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.52 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.53 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.54 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the CPU12 Reference Manual for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	Reset	None	None	–
$FFFC, $FFFD	Clock Monitor fail reset	None	PLLCTL (CME, SCME)	–
$FFFA, $FFFB	COP failure reset	None	COP rate select	–
$FFF8, $FFF9	Unimplemented instruction trap	None	None	–
$FFF6, $FFF7	SWI	None	None	–
$FFF4, $FFF5	XIRQ	X-Bit	None	–
$FFF2, $FFF3	IRQ	I-Bit	IRQCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	$F0
$FFEE, $FFEF	Enhanced Capture Timer channel 0	I-Bit	TIE (C0I)	$EE
$FFEC, $FFED	Enhanced Capture Timer channel 1	I-Bit	TIE (C1I)	$EC
$FFEA, $FFEB	Enhanced Capture Timer channel 2	I-Bit	TIE (C2I)	$EA
$FFE8, $FFE9	Enhanced Capture Timer channel 3	I-Bit	TIE (C3I)	$E8
$FFE6, $FFE7	Enhanced Capture Timer channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Enhanced Capture Timer channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Enhanced Capture Timer channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Enhanced Capture Timer channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Enhanced Capture Timer overflow	I-Bit	TSRC2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI0	I-Bit	SPICR1 (SPIE, SPTIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD0	I-Bit	ATDCTL2 (ASCIE)	$D2
$FFD0, $FFD1	ATD1	I-Bit	ATDCTL2 (ASCIE)	$D0
$FFCE, $FFCF	Port J	I-Bit	PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0)	$CE
$FFCC, $FFCD	Port H	I-Bit	PIEH (PIEH7-0)	$CC

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	-	-	54	$^{o}C/W$
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	-	-	41	$^{o}C/W$

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB	-	5	-	mV
2	P	10-Bit Differential Nonlinearity	DNL	–1	-	1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB	-	20	-	mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5	-	0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error(1)	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the $\overline{XCLKS}$ signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC} . The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-15 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5	-	16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5	-	40	MHz
2	P	Startup Current	i_{OSC}	100	-	-	µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}	-	8[2]	100[3]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45	-	2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5	-	50	MHz
7	D	External square wave pulse width low [4]	t_{EXTL}	9.5	-	-	ns
8	D	External square wave pulse width high [4]	t_{EXTH}	9.5	-	-	ns
9	D	External square wave rise time [4]	t_{EXTR}	-	-	1	ns
10	D	External square wave fall time [4]	t_{EXTF}	-	-	1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}	-	7	-	pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}	-	1.1	-	V
13	P	EXTAL Pin Input High Voltage [4]	$V_{IH,EXTAL}$	0.75*V_{DDPLL}	-	-	V
	T	EXTAL Pin Input High Voltage [4]	$V_{IH,EXTAL}$	-	-	V_{DDPLL} + 0.3	V
14	P	EXTAL Pin Input Low Voltage [4]	$V_{IL,EXTAL}$	-	-	0.25*V_{SSPLL}	V
	T	EXTAL Pin Input Low Voltage [4]	$V_{IL,EXTAL}$	V_{SSPLL} - 0.3	-	-	V
15	C	EXTAL Pin Input Hysteresis [4]	$V_{HYS,EXTAL}$	-	250	-	mV

A.6 MSCAN

Table A-17 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}	-	-	2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5	-	-	µs

A.7.2 Slave Mode

In **Figure A-8** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

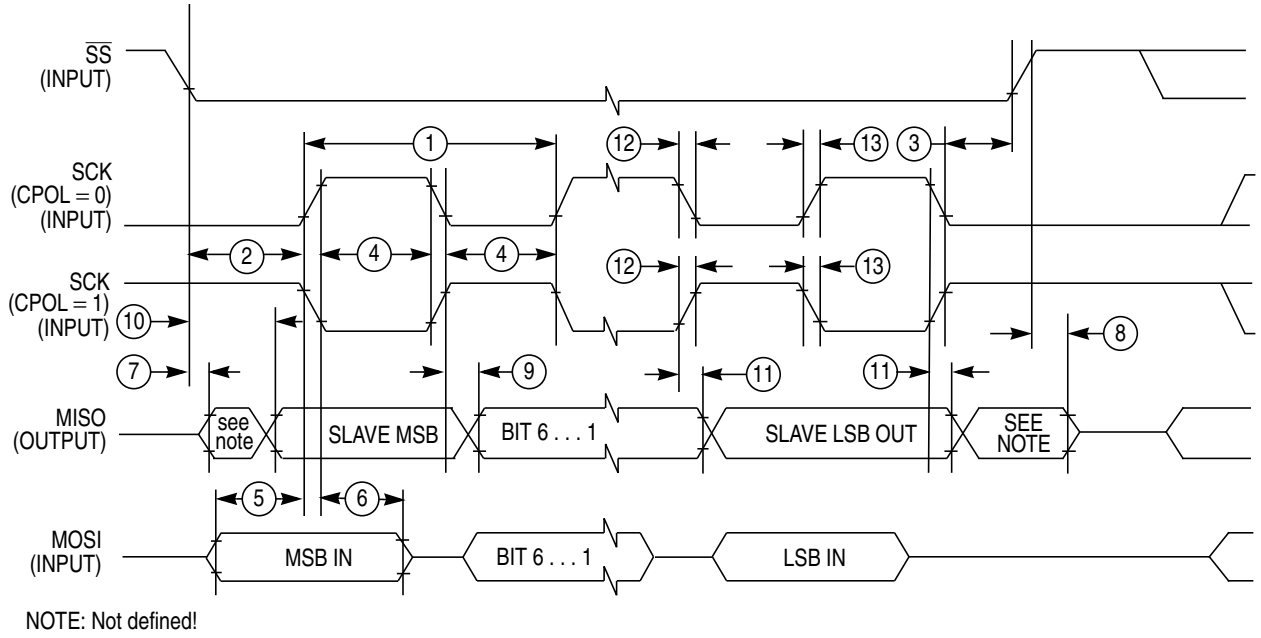


Figure A-8 SPI Slave Timing (CPHA=0)

In **Figure A-9** the timing diagram for slave mode with transmission format CPHA=1 is depicted.