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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dp512vpve

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	27 Nov 2001	11 Feb 2002		- Initial version based on DP256 V2.09.
V01.01	13 Mar 2002	13 Mar 2002		- Updated document formats. - Removed reference to SIM in overview. - Changed XCLKS to PE7 in signal description. - Removed "Oscillator start-up time from POR or STOP" from Oscillator Characterisitcs. - Changed VDD and VDDPLL to 2.35V. - Updated C_{INS}. - Updated I_{OL}/I_{OH} values. - Updated input capacitance. - Updated NVM timing characteristics.
V01.02	02 Apr 2002	02 Apr 2002		- Updated document reference (SPI, SCI).
V01.03	15 Apr 2002	15 Apr 2002		- Corrected values in device memory map (RAM start, flash protected sector sizes). - Updated document reference (SCI).
V01.04	06 Jun 2002	06 Jun 2002		- Changed all operating frequency references to 50MHz EXTAL and removed references to 80 pin LQFP.
V01.05	05 Jul 2002	05 Jul 2002		- Preface Table "Document References": Changed to full naming for each block. - Table "Interrupt Vector Locations", Column "Local Enable": Corrected several register and bit names. - Table "Signal Properties": Added column "Internal Pull Resistor". - Table "PLL Characteristics": Updated parameters K1 and f1 - Figure "Basic Pll functional diagram": Inserted XFC pin in diagram - Enhanced section "XFC Component Selection" - Added to Sections ATD, ECT and PWM: freeze mode = active BDM mode.

Figure 1-1 MC9S12DP512 Block Diagram

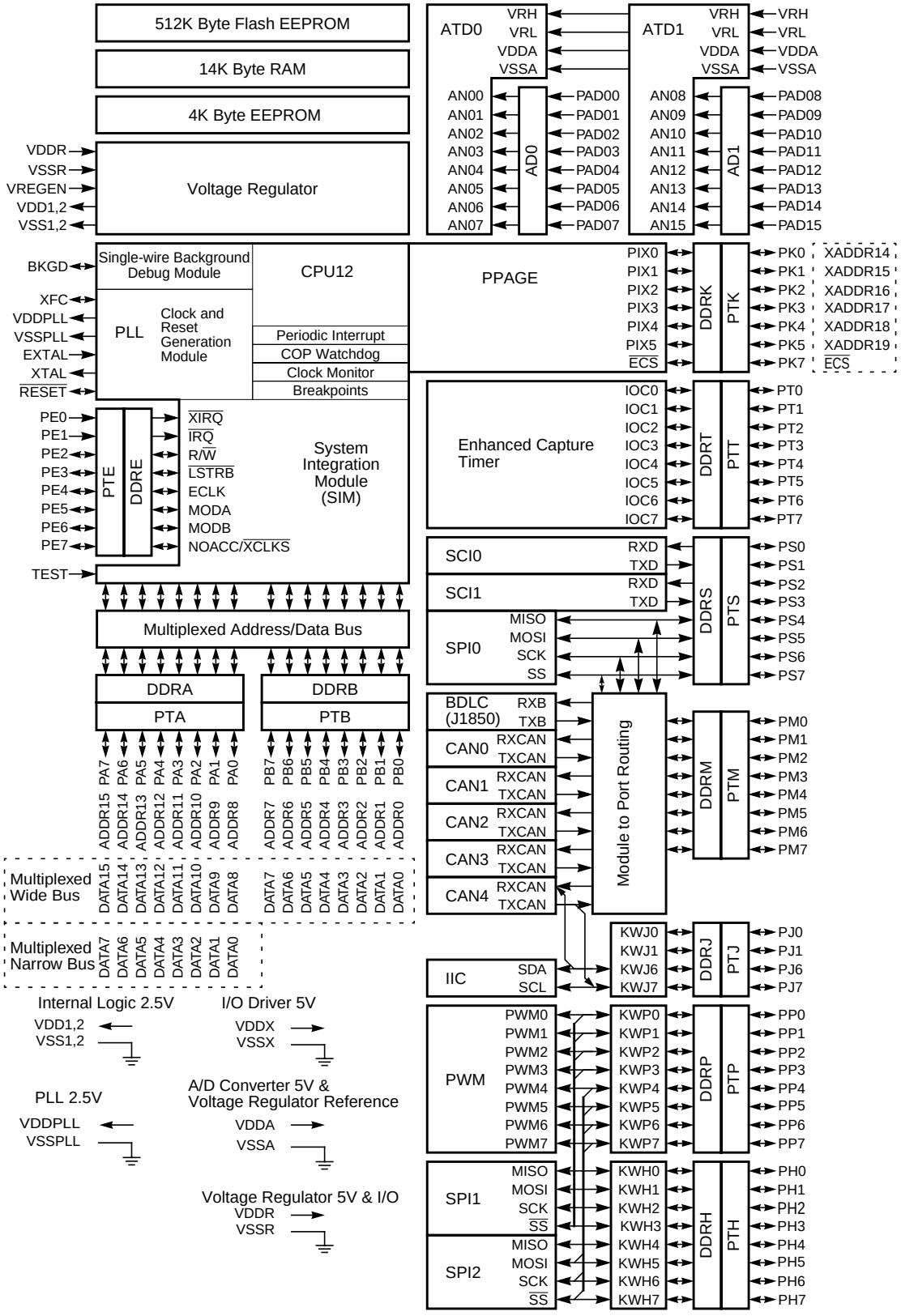
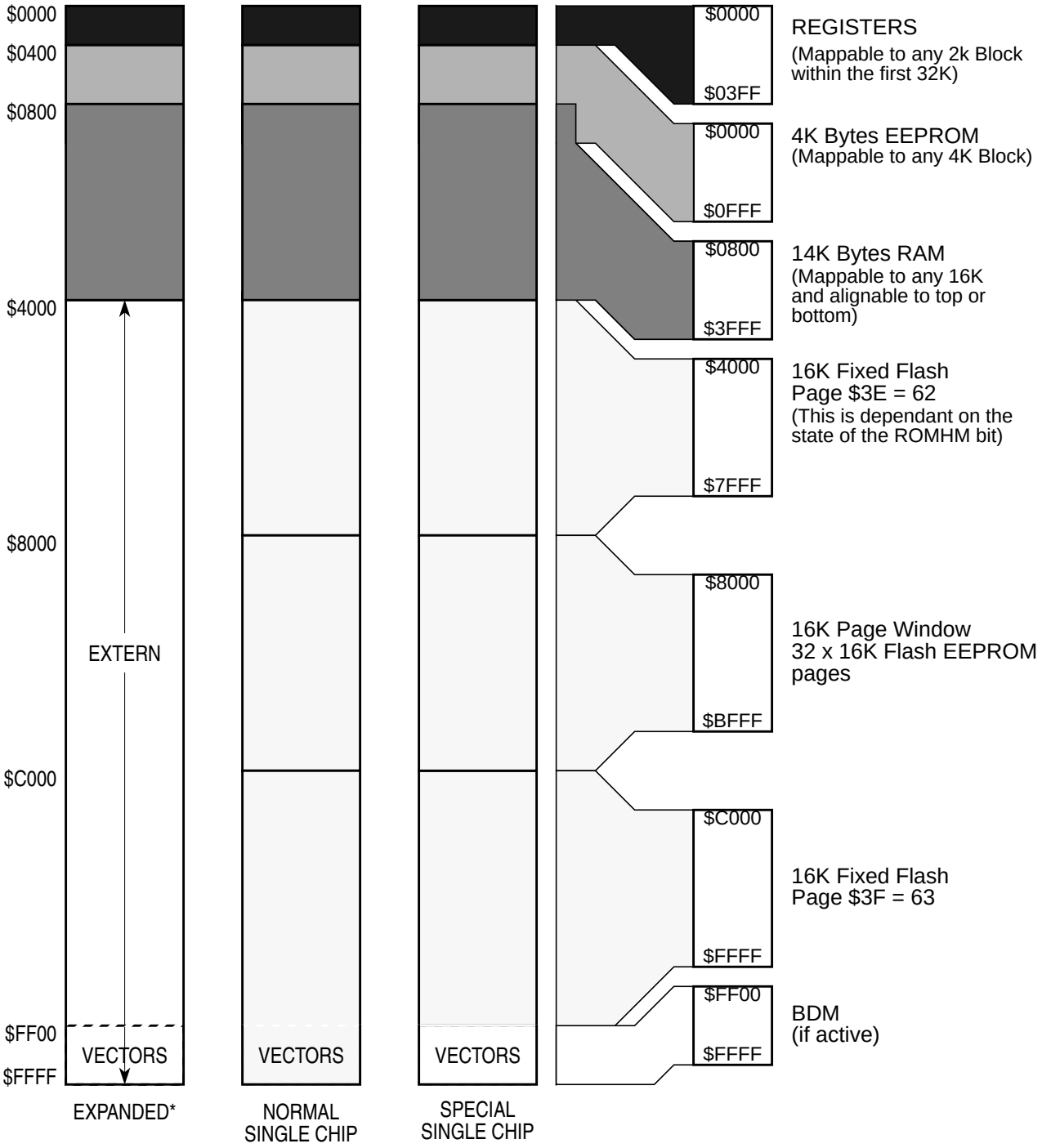


Figure 1-2 MC9S12DP512 Memory Map



* Assuming that a '0' was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
$006C	Reserved	Read:								
		Write:								
$006D	TIMTST Test Only	Read:	0	0	0	0	0	0	TCBYP	0
		Write:								
$006E - $006F	Reserved	Read:								
		Write:								
$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATD0CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATD0CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATD0CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATD0CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATD0STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATD0TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATD0TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008B	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008D	ATD0DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$008E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008F	PORTAD0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0090	ATD0DR0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0091	ATD0DR0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0092	ATD0DR1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0093	ATD0DR1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0094	ATD0DR2H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0095	ATD0DR2L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0096	ATD0DR3H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0097	ATD0DR3L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0098	ATD0DR4H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$00D8 - $00DF SPI0 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPI0DR	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00DE - $00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								
$00E5 - $00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E8 - $00EF BDLC (Bytelevel Data Link Controller J1850)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E8	DLCBCR1	Read:	IMSG	CLKS	0	0	0	0	IE	WCM
		Write:								
$00E9	DLCBSVR	Read:	0	0	I3	I2	I1	I0	0	0
		Write:								
$00EA	DLCBCR2	Read:	SMRST	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
		Write:								
$00EB	DLCBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$00EC	DLCBARD	Read:	0	RXPOL	0	0	BO3	BO2	BO1	BO0
		Write:								
$00ED	DLCBRSR	Read:	0	0	R5	R4	R3	R2	R1	R0
		Write:								
$00EE	DLCSCR	Read:	0	0	0	BDLCE	0	0	0	0
		Write:								
$00EF	DLCBSTAT	Read:	0	0	0	0	0	0	0	IDLE
		Write:								

$0100 - $010F Flash Control Register (fts512k4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	FADDRHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010C - $010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets4k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111 - $0112	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	10	9	Bit 8
		Write:								
$0119	EADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$011A	EDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$011B	EDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$011C - $011F Reserved for RAM Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C - $011F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0139	ATD1DR4L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$013A	ATD1DR5H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$013B	ATD1DR5L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$013C	ATD1DR6H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$013D	ATD1DR6L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$013E	ATD1DR7H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$013F	ATD1DR7L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0140 - $017F CAN0 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$014C - $014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0150 - $0153	CAN0IDAR0 - CAN0IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								

$0140 - $017F CAN0 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0154 - $0157	CAN0IDMR0 - CAN0IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0158 - $015B	CAN0IDAR4 - CAN0IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$015C - $015F	CAN0IDMR4 - CAN0IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0160 - $016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$0170 - $017F	CAN0TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$xxx0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CANxRIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$xxx1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CANxRIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$xxx2	Standard ID	Read:								
	CANxRIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$xxx3	Standard ID	Read:								
	CANxRIDR3	Write:								
$xxx4 - $xxxB	CANxRDSR0 - CANxRDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
$xxxC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$xxxD	Reserved	Read: Write:								
$xxxE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$xxxF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$xx10	Extended ID CANxTIDR0	Read: Write:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	Read: Write:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
$xx11	Extended ID CANxTIDR1	Read: Write:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
	Standard ID	Read: Write:	ID2	ID1	ID0	RTR	IDE=0			
$xx12	Extended ID CANxTIDR2	Read: Write:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read: Write:								

$0180 - $01BF CAN1 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0194 - $0197	CAN1IDMR0 - CAN1IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0198 - $019B	CAN1IDAR4 - CAN1IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019C - $019F	CAN1IDMR4 - CAN1IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01A0 - $01AF	CAN1RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$01B0 - $01BF	CAN1TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

$01C0 - $01FF CAN2 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01C0	CAN2CTL0	Read: Write:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
$01C1	CAN2CTL1	Read: Write:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
$01C2	CAN2BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$01C3	CAN2BTR1	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$01C4	CAN2RFLG	Read: Write:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
$01C5	CAN2RIER	Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$01C6	CAN2TFLG	Read: Write:	0	0	0	0	0	TXE2	TXE1	TXE0
$01C7	CAN2TIER	Read: Write:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
$01C8	CAN2TARQ	Read: Write:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
$01C9	CAN2TAAK	Read: Write:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
$01CA	CAN2TBSEL	Read: Write:	0	0	0	0	0	TX2	TX1	TX0
$01CB	CAN2IDAC	Read: Write:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
$01CC - $01CD	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$01CE	CAN2RXERR	Read: Write:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
$01CF	CAN2TXERR	Read: Write:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
$01D0 - $01D3	CAN2IDAR0 - CAN2IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D4 - $01D7	CAN2IDMR0 - CAN2IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0

$0200 - $023F CAN3 (Freescale Scalable CAN - FSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$021C - $021F	CAN3IDMR4 - CAN3IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0220 - $022F	CAN3RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$0230 - $023F	CAN3TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

$0240 - $027F PIM (Port Integration Module PIM_9DP256)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0240	PTT	Read: Write:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0242	DDRT	Read: Write:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
$0243	RDRT	Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
$0244	PERT	Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
$0245	PPST	Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
$0246 - $0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTS	Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$024A	DDRS	Read: Write:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
$024B	RDRS	Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
$024C	PERS	Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
$024D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block Guides of the individual IP blocks on the device.

2.3.40 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

2.3.41 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

2.3.42 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output or an input for the PWM emergency shutdown. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.43 PP6 / KWP6 / PWM6 / $\overline{\text{SS2}}$ — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.44 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.45 PP4 / KWP4 / PWM4 / MISO2 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.46 PP3 / KWP3 / PWM3 / $\overline{\text{SS1}}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 1 (SPI1).

NOTE: *All VSS pins must be connected together in the application.*

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.
VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.
IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}	-	-	65	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled (1)	I_{DDW}	-	-	40 5	mA
3	C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) 1, 2 -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}	-	370 400 450 550 600 650 800 850 1200	500 1600 2100 5000	µA
4	C C C C C C C	Pseudo Stop Current (RTI and COP enabled) (1), (2) -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}	-	570 600 650 750 850 1200 1500	-	µA
5	C P C C P C P C P	Stop Current (2) -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}	-	12 25 100 130 160 200 350 400 600	100 1200 1700 5000	µA

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5	-	50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1	-	-	MHz
3	D	Operating Frequency	f_{NVMOP}	150	-	200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]	-	74.5 [3]	µs
5	D	Flash Row Programming consecutive word [4]	t_{bwpgm}	20.4 (2)	-	31 (3)	µs
6	D	Flash Row Programming Time for 64 Words (4)	t_{brpgm}	1331.2 (2)	-	2027.5 (3)	µs
7	P	Sector Erase Time	t_{era}	20 [5]	-	26.7 (3)	ms
8	P	Mass Erase Time	t_{mass}	100 (5)	-	133 (3)	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]	-	65546 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 (6)	-	2058 (7)	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **Section A.3.1.1 Single Word Programming- Section A.3.1.4 Mass Erase**for guidance.
4. Row Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. f_{osc} = 4MHz, C = 22pF.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. Only valid if Pierce oscillator/external clock mode is selected

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

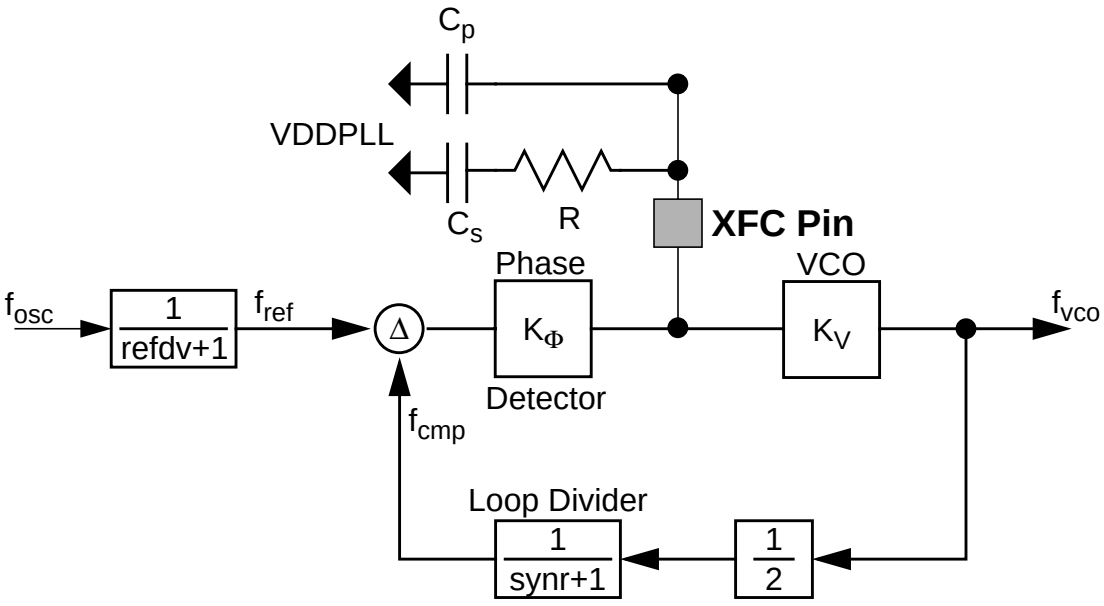


Figure A-3 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-16**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-16 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1	-	5.5	MHz
2	D	VCO locking range	f_{VCO}	8	-	50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3	-	4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0	-	1.5	%(1)
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5	-	2.5	%(1)
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6	-	8	%(1)
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}	-	0.5	-	ms
8	D	PLLON Acquisition mode stabilization delay (2)	t_{acq}	-	0.3	-	ms
9	D	PLLON Tracking mode stabilization delay (2)	t_{al}	-	0.2	-	ms
10	D	Fitting parameter VCO loop gain	K_1	-	-100	-	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1	-	60	-	MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$	-	38.5	-	µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$	-	3.5	-	µA
14	C	Jitter fit parameter 1(2)	j_1	-	-	1.1	%
15	C	Jitter fit parameter 2(2)	j_2	-	-	0.13	%

NOTES:
1. % deviation from target frequency
2. f_{OSC} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DP512 packages.