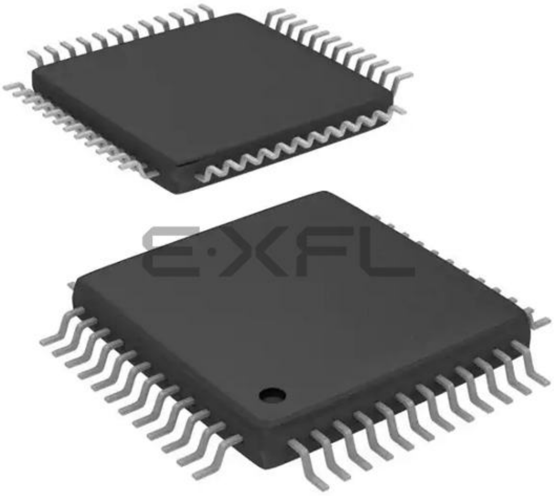
# Silicon Labs - EFM32HG322F32G-B-QFP48 Datasheet



## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

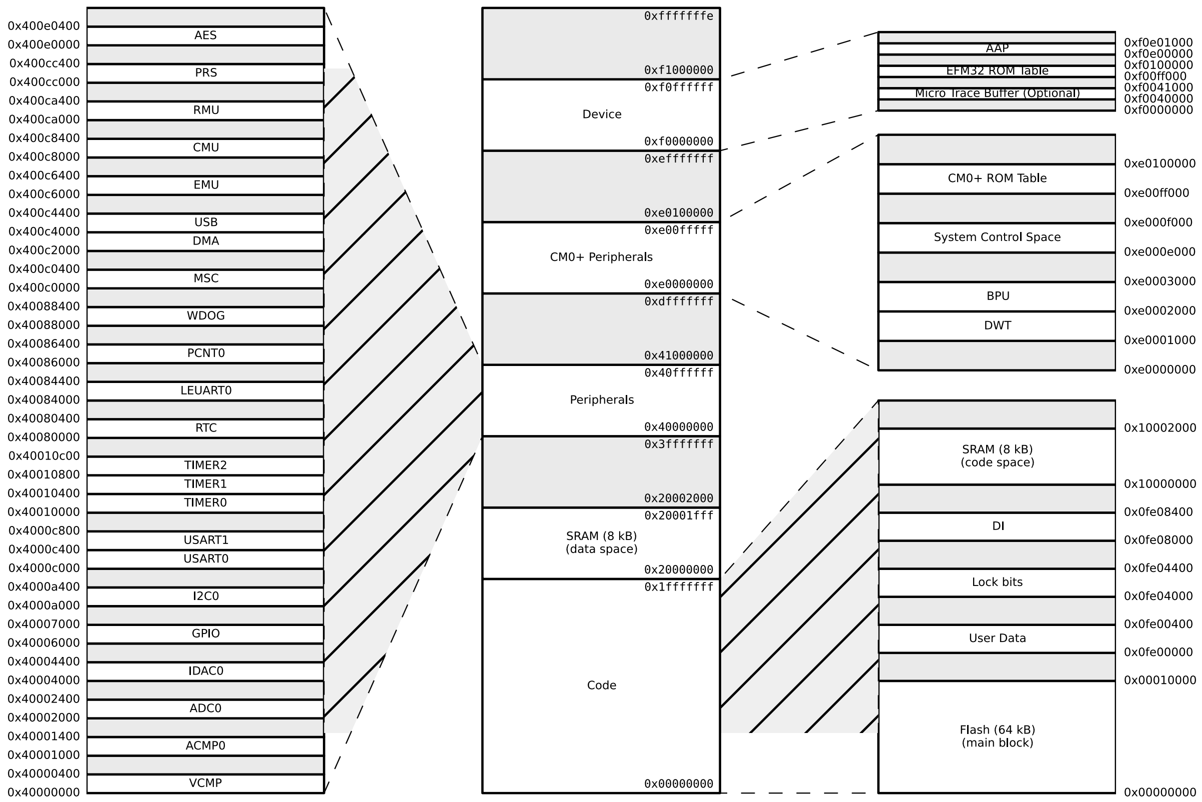
| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32hg322f32g-b-qfp48 |

| Module | Configuration | Pin Connections |
|---|---|---|
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 35 pins | Available pins are shown in Table 4.3 (p. 57) |

## 2.3 Memory Map

The *EFM32HG322* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

*Figure 2.2. EFM32HG322 Memory Map with largest RAM and Flash sizes*



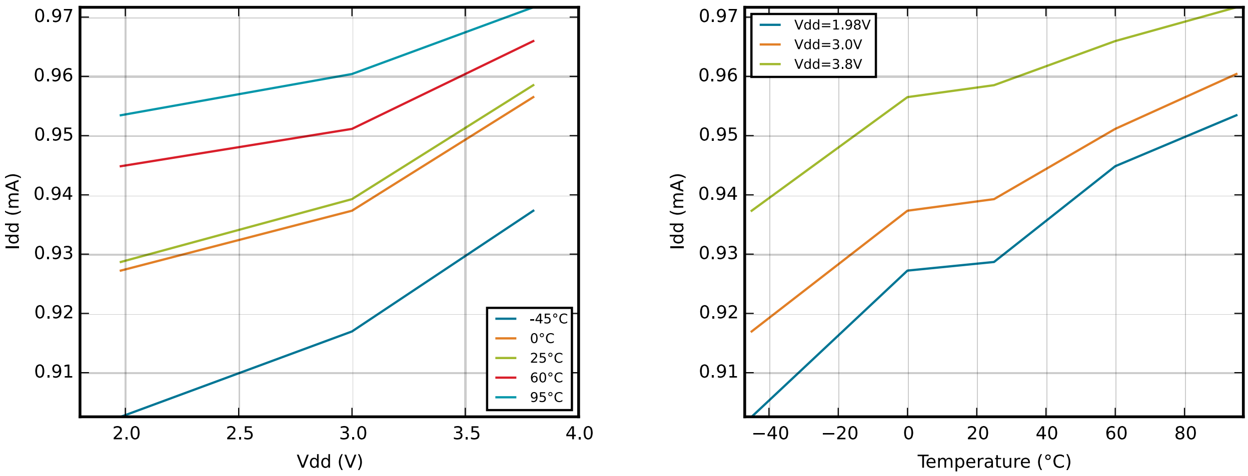
## 3.4 Current Consumption

### *Table 3.3. Current Consumption*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from Flash. | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 148 | 158 | µA/ MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 153 | 163 | µA/ MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 161 | 172 | µA/ MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 163 | 174 | µA/ MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 127 | 137 | µA/ MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 129 | 139 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 131 | 140 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 134 | 143 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 134 | 143 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 137 | 145 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 136 | 144 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 139 | 148 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 142 | 150 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 146 | 154 | µA/ MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 184 | 196 | µA/ MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 194 | 208 | µA/ MHz |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM1}$ | EM1 current | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 68 | µA/MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 67 | 71 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 85 | 91 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 86 | 92 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 51 | 55 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 52 | 56 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 53 | 57 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 54 | 58 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 56 | 59 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 57 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 58 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 59 | 63 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 68 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 67 | 71 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 106 | 114 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 114 | 126 | µA/MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.9 | 1.35 | µA |

*Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz*



## 3.4.2 EM1 Current Consumption

*Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz*

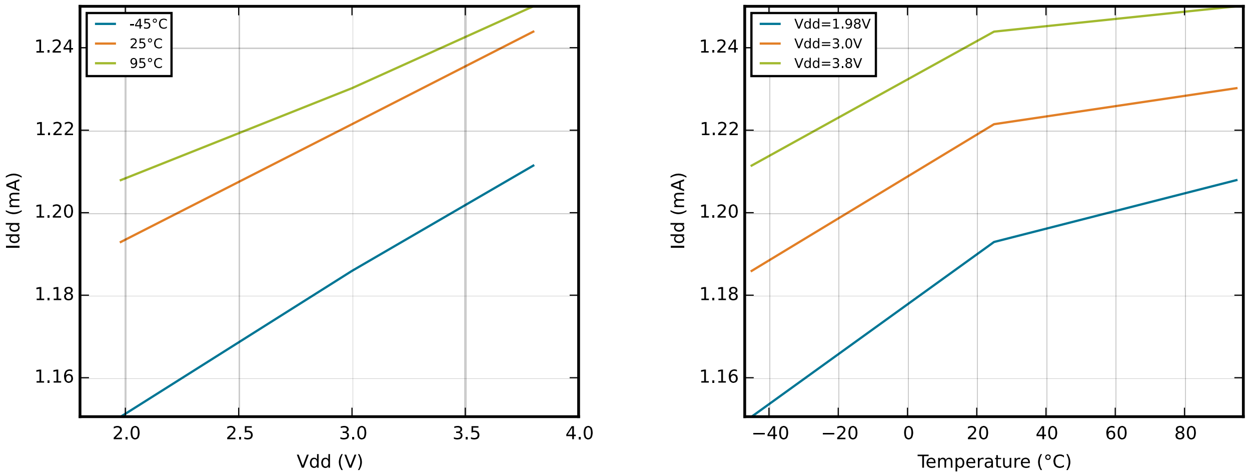


**Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz**

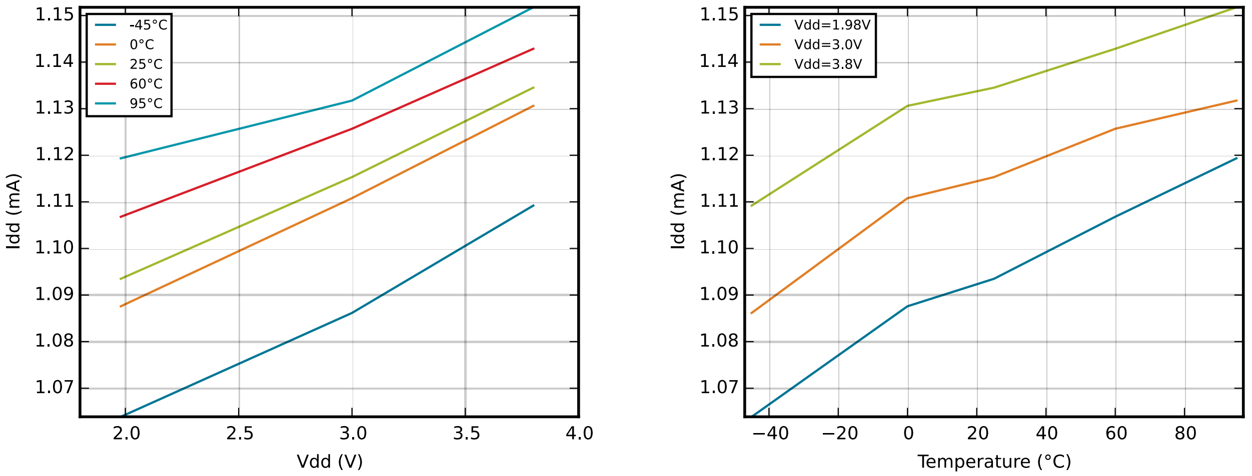
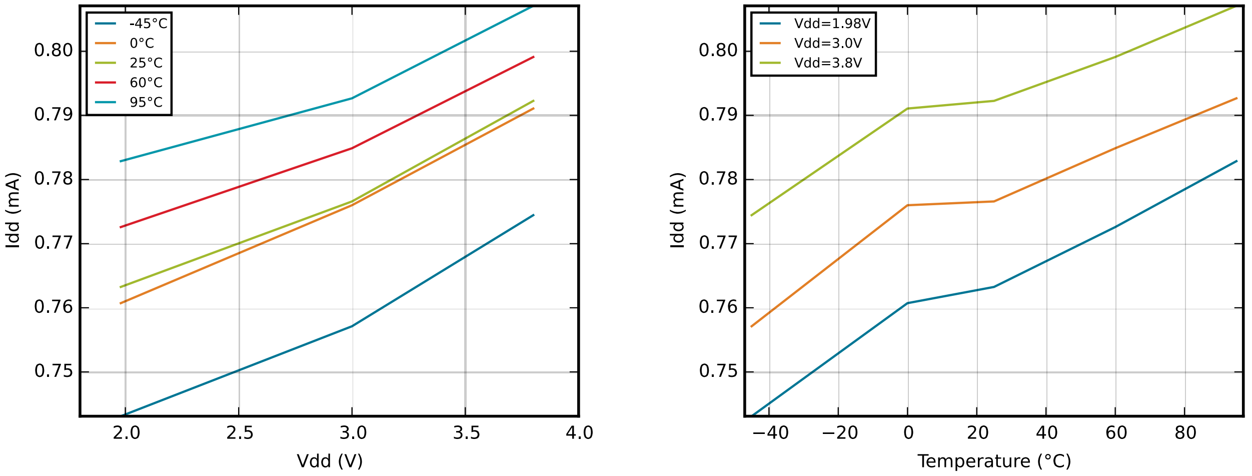
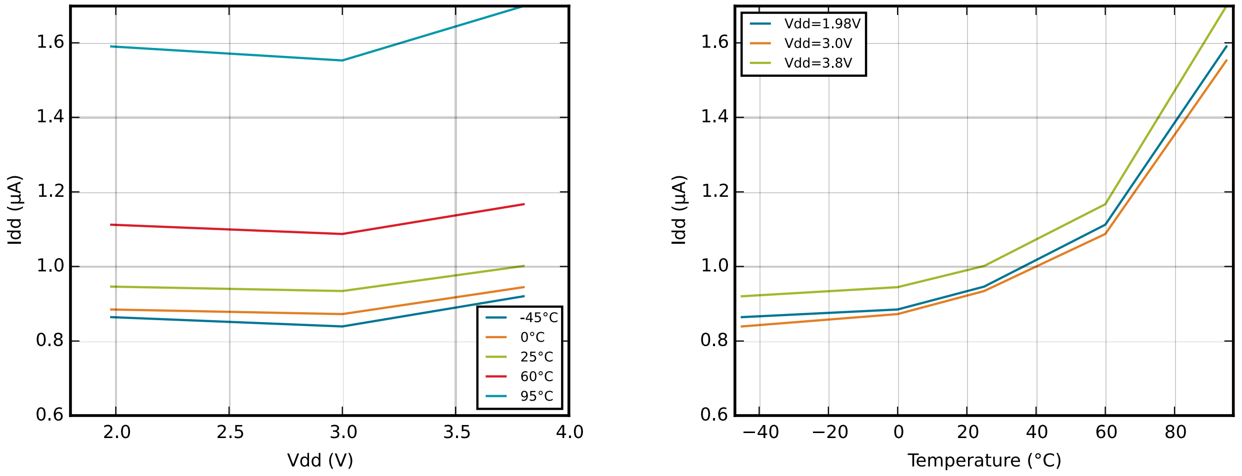


**Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**



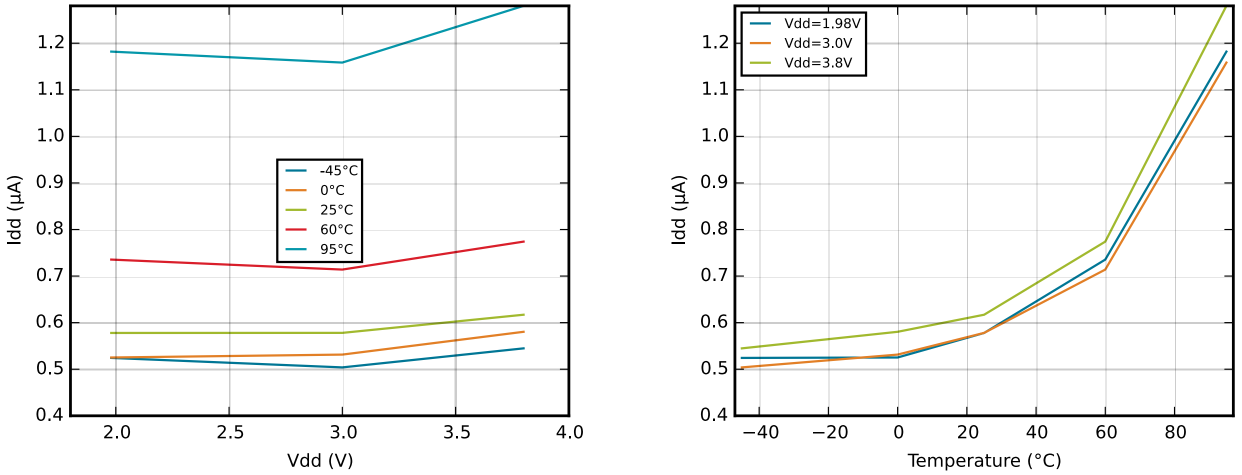
## 3.4.3 EM2 Current Consumption

*Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.*



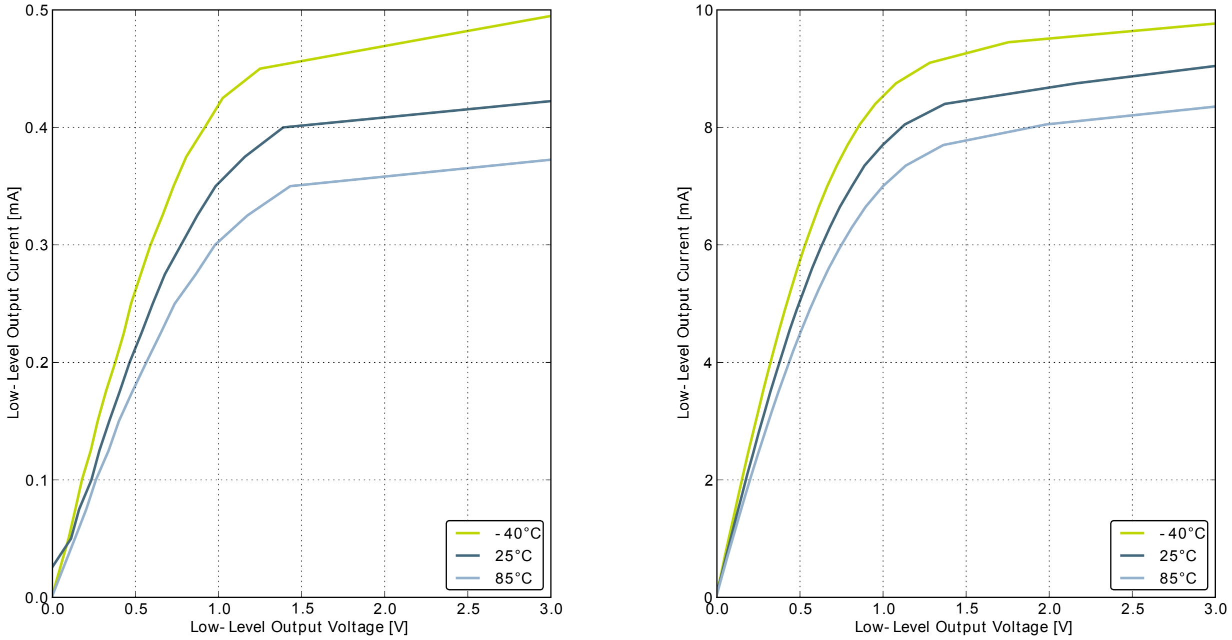
## 3.4.4 EM3 Current Consumption

*Figure 3.12. EM3 current consumption.*



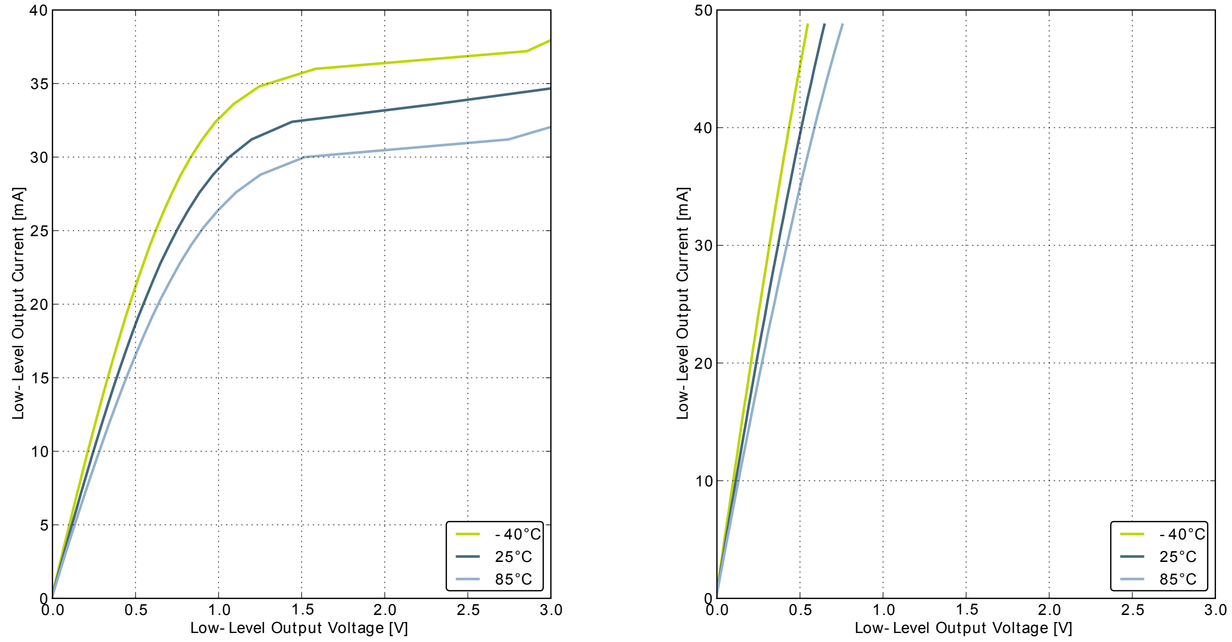
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PD}$ | I/O pin pull-down resistor | | | 40 | | kOhm |
| $R_{IOESD}$ | Internal ESD series resistor | | | 200 | | Ohm |
| $t_{IOGLITCH}$ | Pulse width of pulses to be removed by the glitch suppression filter | | 10 | | 50 | ns |
| $t_{IOOF}$ | Output fall time | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L$=12.5-25pF. | 20+0.1$C_L$ | | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L$=350-600pF | 20+0.1$C_L$ | | 250 | ns |
| $V_{IOHYST}$ | I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{DD}$ = 1.98 - 3.8 V | 0.1$V_{DD}$ | | | V |

*Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

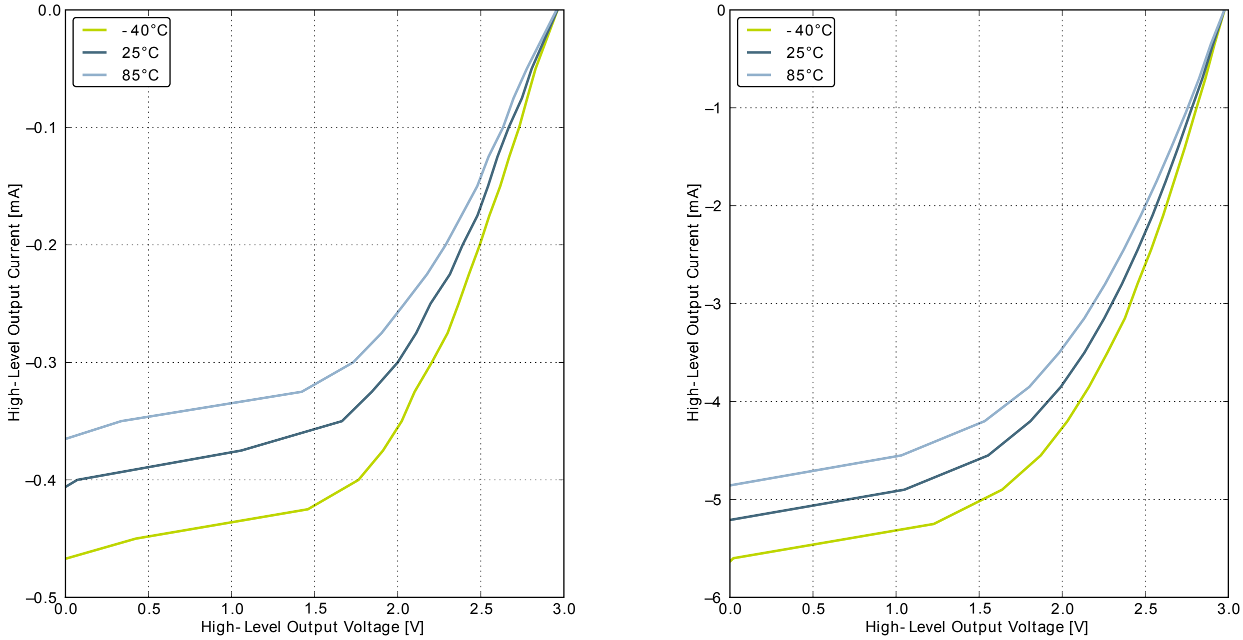
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

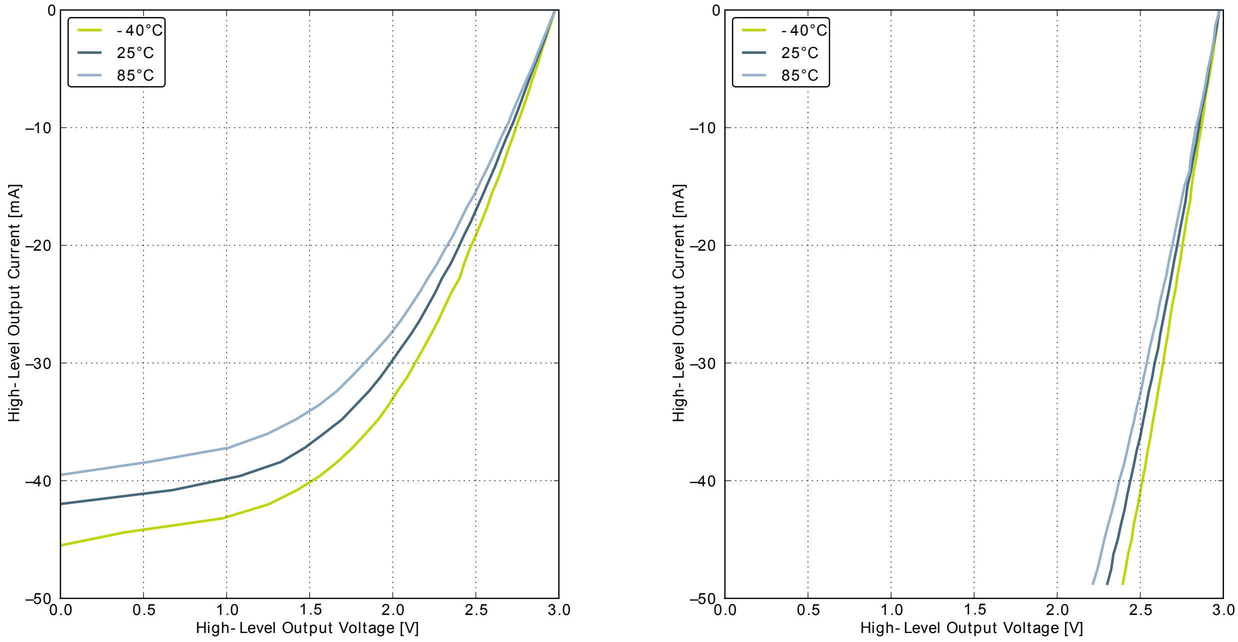
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



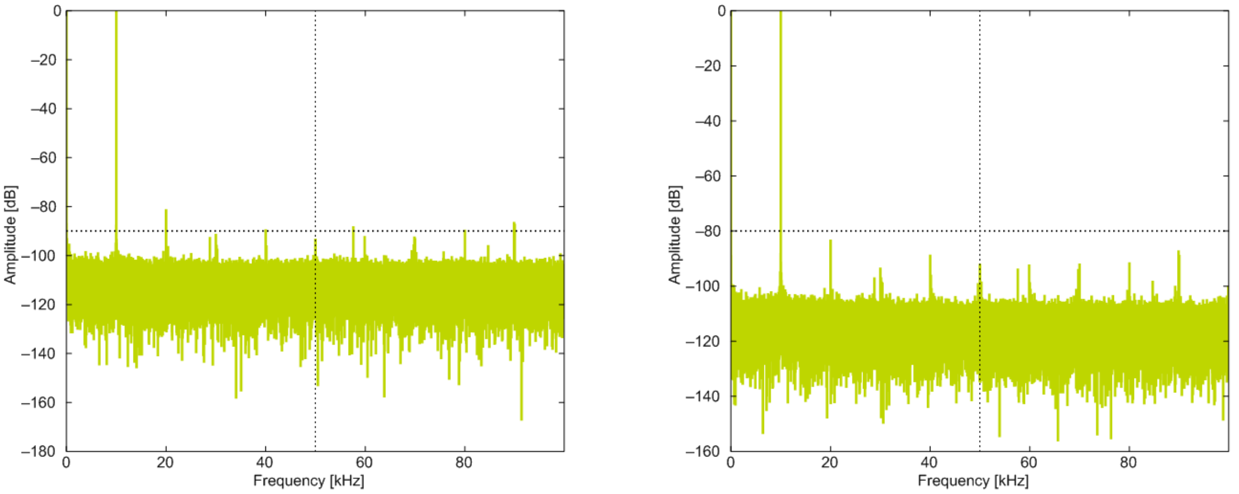
GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 392 | 510 | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11 | | 244 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADC-CLK Cycles |
| | | 8 bit | 11 | | | ADC-CLK Cycles |
| | | 12 bit | 13 | | | ADC-CLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADC-CLK Cycles |

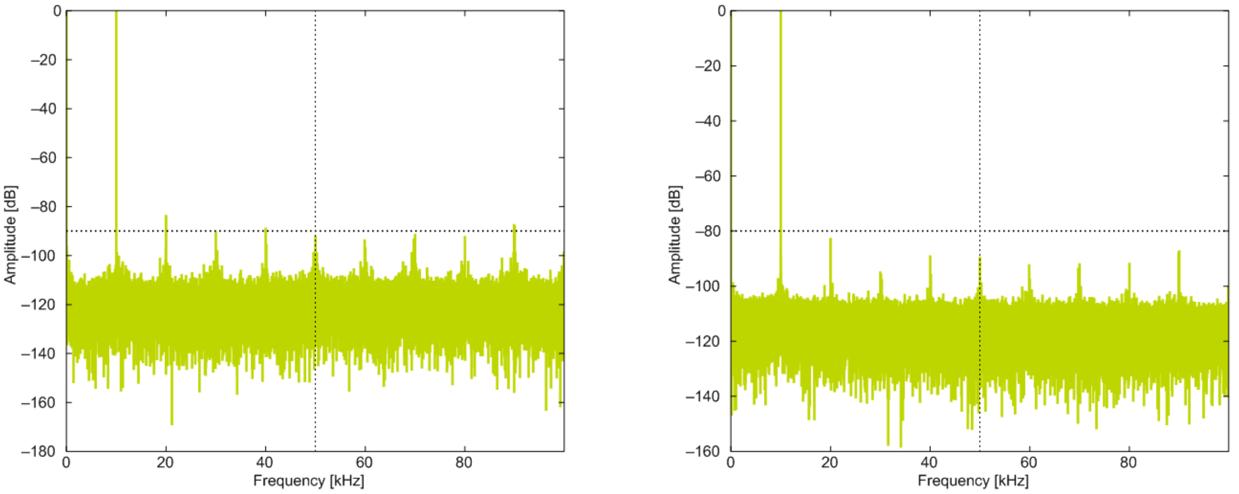
### 3.10.1 Typical performance

*Figure 3.28.  ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C*



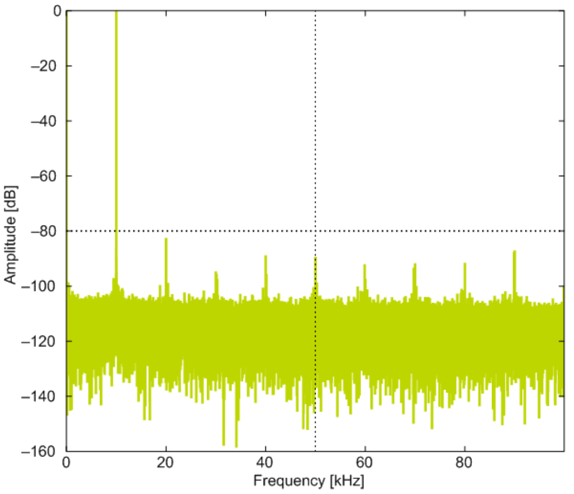
1.25V Reference

2.5V Reference



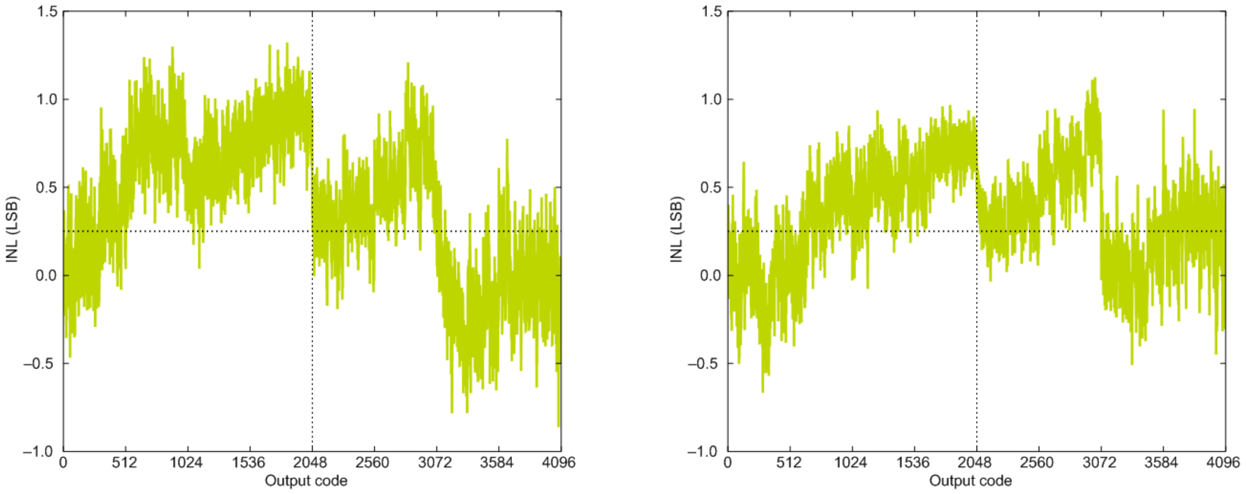
2XVDDVSS Reference

5VDIFF Reference



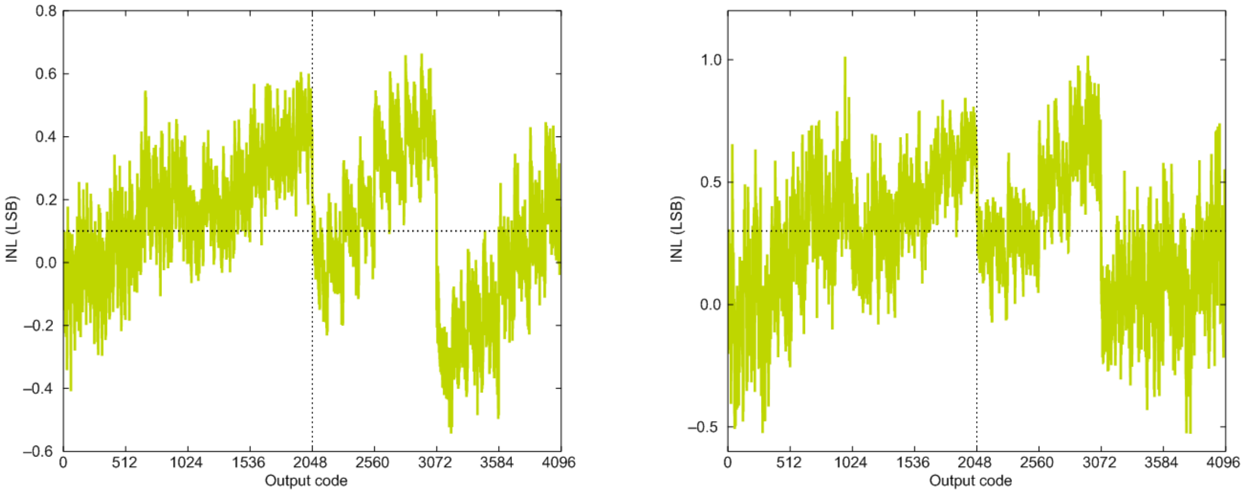
VDD Reference

*Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C*



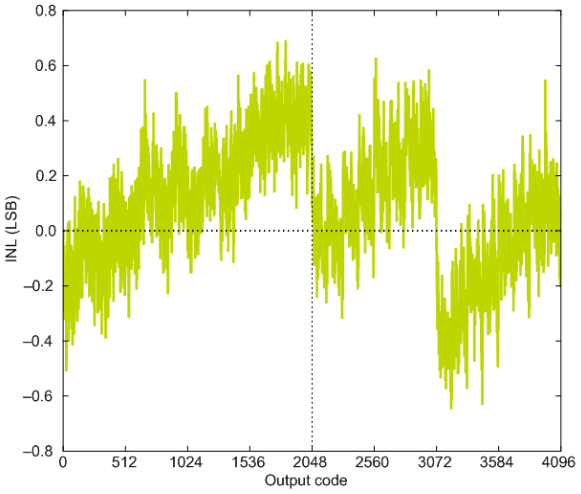
1.25V Reference

2.5V Reference



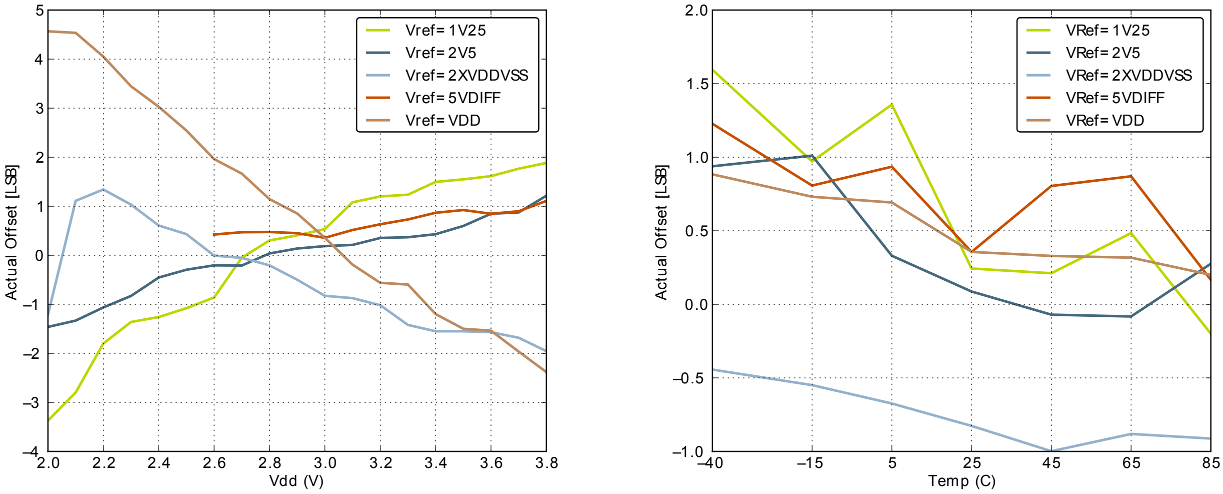
2XVDDVSS Reference

5VDIFF Reference



VDD Reference

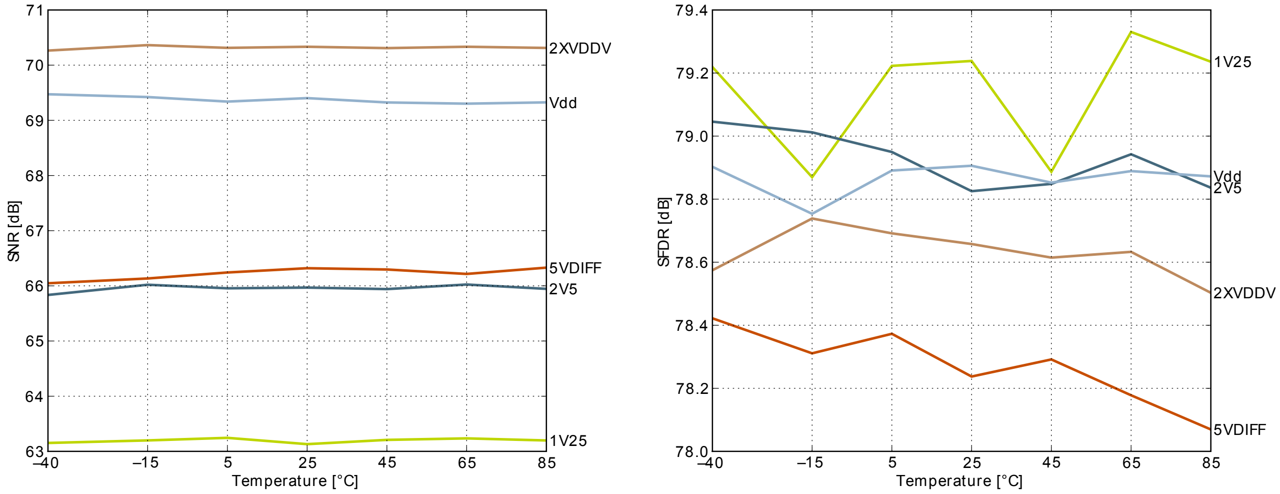
### Figure 3.31. ADC Absolute Offset, Common Mode = Vdd /2



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

### Figure 3.32. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)

Spurious-Free Dynamic Range (SFDR)

### Table 3.18. IDAC Range 1 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 14.4 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.2 | | µA |
| $I_{STEP}$ | Step size | | | 0.1 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT} = V_{DD}$ - 100mV | | 0.75 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 38.4 | | nA/V |

### Table 3.19. IDAC Range 1 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 19.4 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.2 | | µA |
| $I_{STEP}$ | Step size | | | 0.1 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.32 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 40.9 | | nA/V |

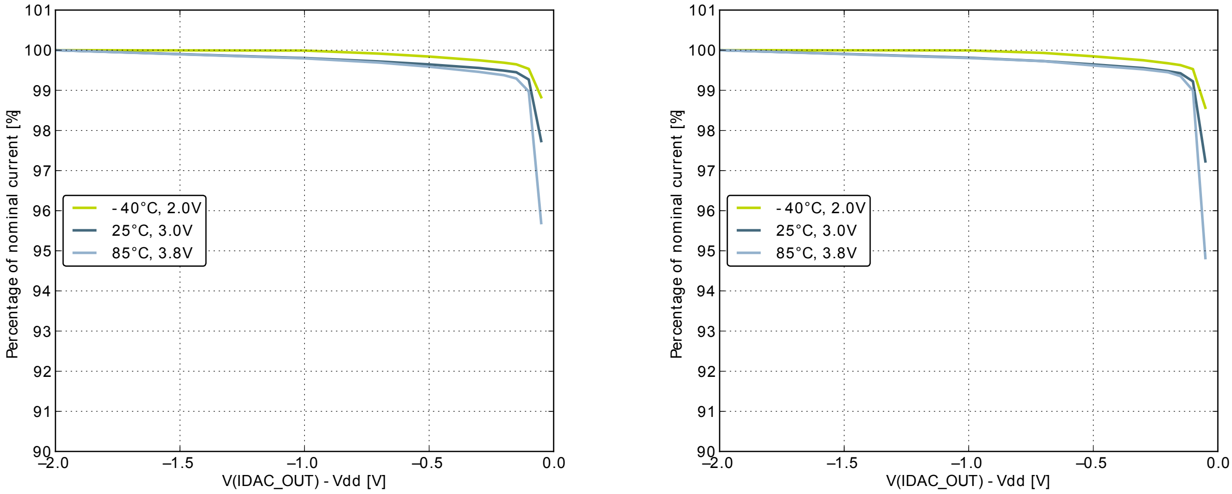
### Table 3.20. IDAC Range 2 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 17.3 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.5 | | µA |
| $I_{STEP}$ | Step size | | | 0.5 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT} = V_{DD}$ - 100mV | | 1.22 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 96.6 | | nA/V |

### Table 3.21. IDAC Range 2 Sink

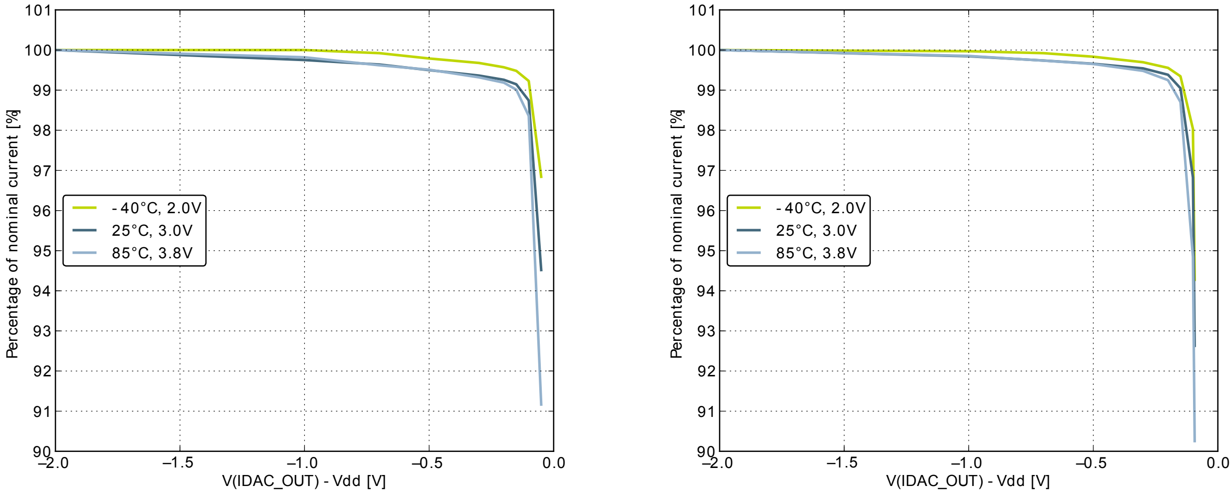
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 29.3 | | µA |

### Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT



Range 0

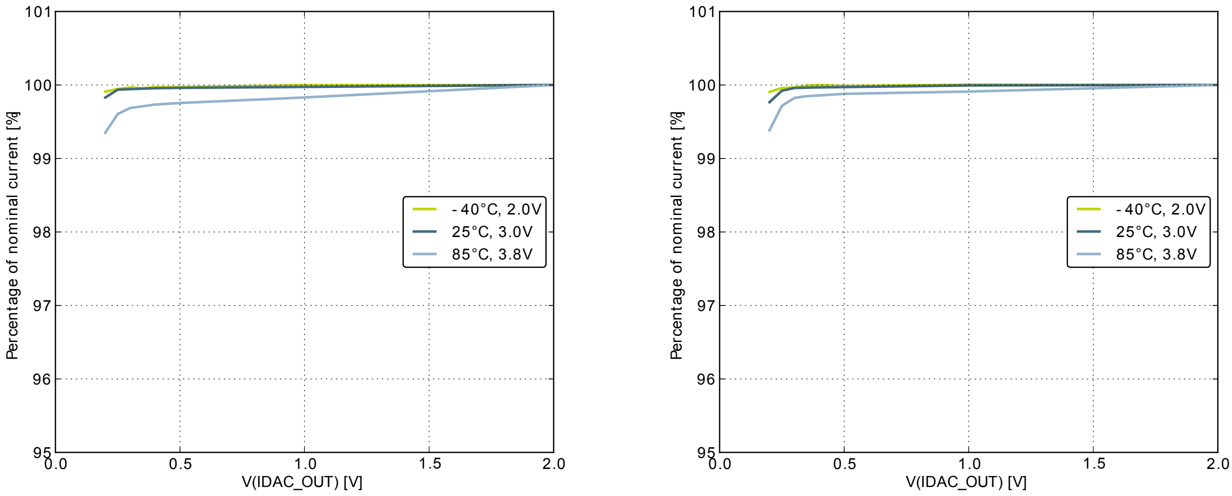
Range 1



Range 2

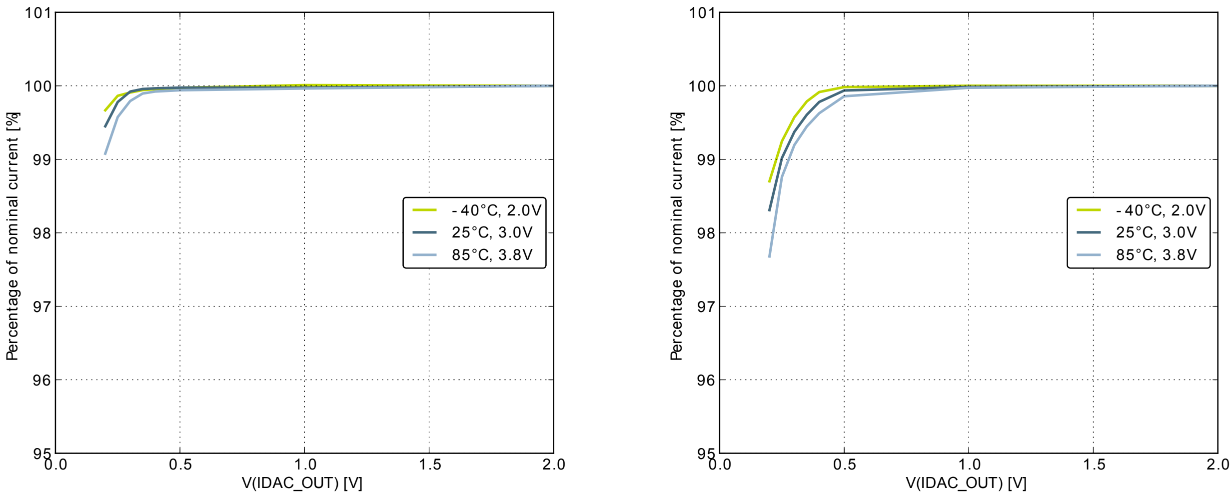
Range 3

## *Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT*



Range 0

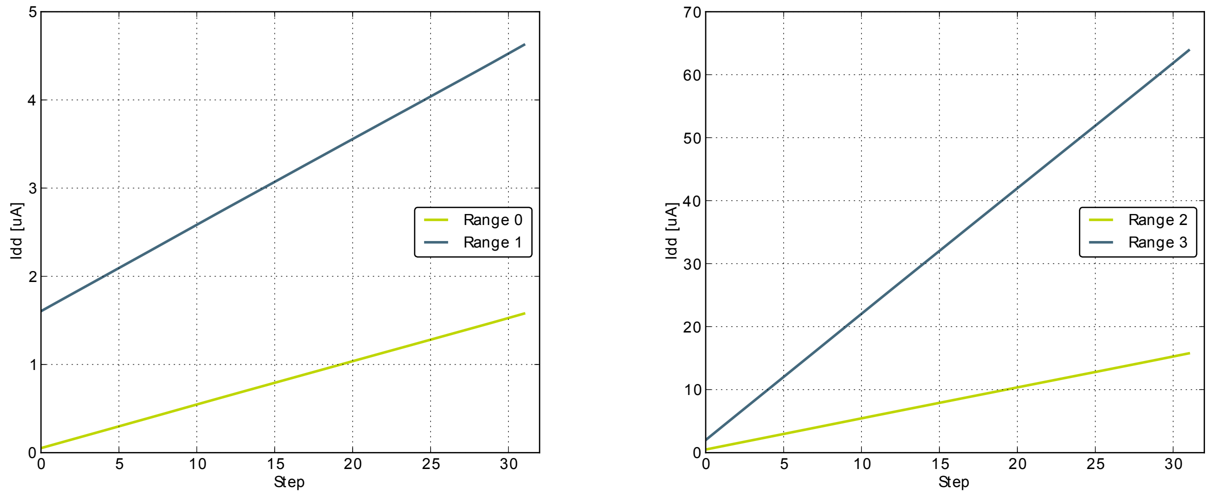
Range 1



Range 2

Range 3

## *Figure 3.36. IDAC linearity*



| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Functionality** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **Description** |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU6 | PC4 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | PE10 | PE13 | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | PE11 | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Functionality** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **Description** |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | | | | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | | PC3 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | PC4 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | PC3 | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | PC2 | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

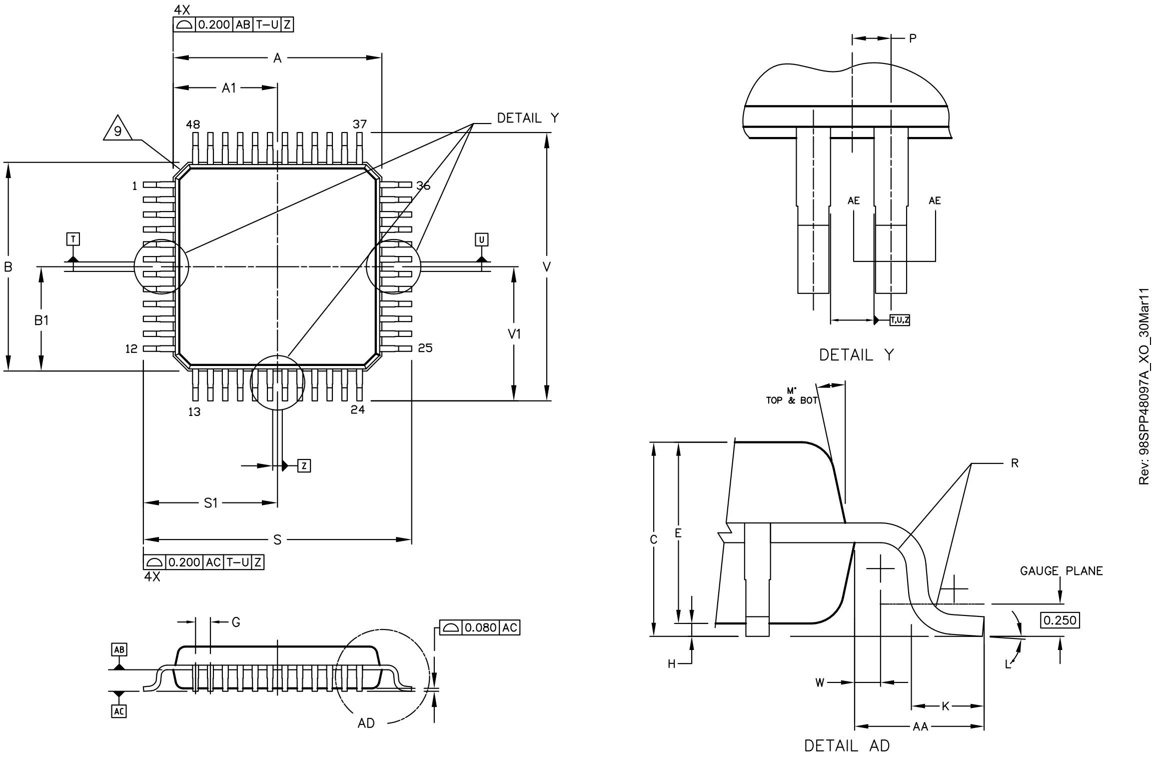
The specific GPIO pins available in *EFM32HG322* is shown in Table 4.3 (p. 57) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

*Table 4.3. GPIO Pinout*

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

## 4.4 TQFP48 Package

*Figure 4.2. TQFP48*



Note:

1. Dimensions and tolerance per ASME Y14.5M-1994
2. Control dimension: Millimeter.
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.

9. Exact shape of each corner is optional.

*Table 4.4. QFP48 (Dimensions in mm)*

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| A | - | 7.000 BSC | - | M | - | 12DEG REF | - |
| A1 | - | 3.500 BSC | - | N | 0.090 | - | 0.160 |
| B | - | 7.000 BSC | - | P | - | 0.250 BSC | - |
| B1 | - | 3.500 BSC | - | R | 0.150 | - | 0.250 |
| C | 1.000 | - | 1.200 | S | - | 9.000 BSC | - |
| D | 0.170 | - | 0.270 | S1 | - | 4.500 BSC | - |
| E | 0.950 | - | 1.050 | V | - | 9.000 BSC | - |
| F | 0.170 | - | 0.230 | V1 | - | 4.500 BSC | - |
| G | - | 0.500 BSC | - | W | - | 0.200 BSC | - |
| H | 0.050 | - | 0.150 | AA | - | 1.000 BSC | - |
| J | 0.090 | - | 0.200 | | | | |
| K | 0.500 | - | 0.700 | | | | |
| L | 0DEG | - | 7DEG | | | | |

The TQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx