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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg322f64g-a-qfp48

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG322 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG322F32G-B-QFP48	32	8	25	1.98 - 3.8	-40 - 85	TQFP48
EFM32HG322F64G-B-QFP48	64	8	25	1.98 - 3.8	-40 - 85	TQFP48

Adding the suffix 'R' to the part number (e.g. EFM32HG322F32G-B-QFP48R) denotes tape and reel.

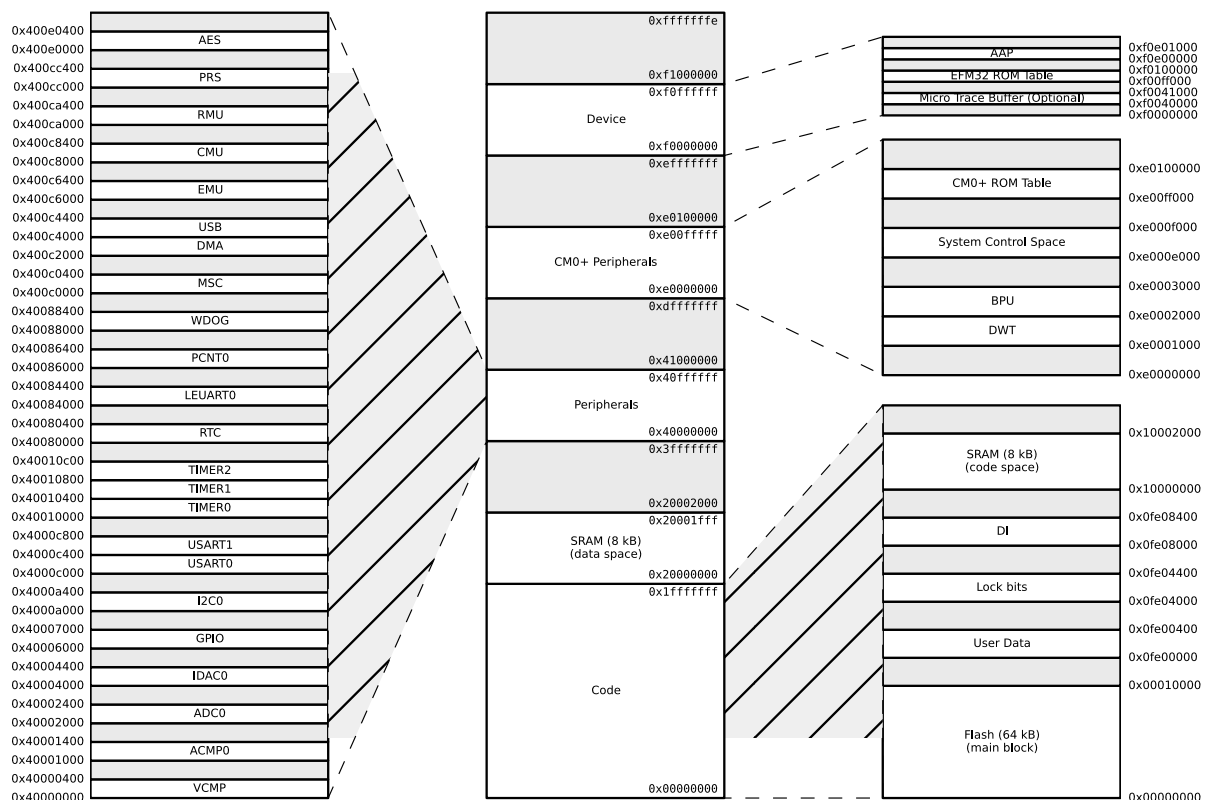
Visit **www.silabs.com** for information on global distributors and representatives.

Module	Configuration	Pin Connections
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[4:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	35 pins	Available pins are shown in Table 4.3 (p. 57)

2.3 Memory Map

The EFM32HG322 memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32HG322 Memory Map with largest RAM and Flash sizes



3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		148	158	$\mu\text{A}/\text{MHz}$
		24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		153	163	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		161	172	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		163	174	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		127	137	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		129	139	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		131	140	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		137	145	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		136	144	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		139	148	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		142	150	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		146	154	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		184	196	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		194	208	$\mu\text{A}/\text{MHz}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		85	91	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		86	92	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		51	55	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		52	56	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		53	57	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		54	58	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		56	59	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		57	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		58	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		59	63	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		106	114	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		114	126	µA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9	1.35	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		1.6	3.50	μA
I_{EM3}	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.6	0.90	μA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		1.2	2.65	μA
I_{EM4}	EM4 current	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.02	0.035	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		0.18	0.480	μA

3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz

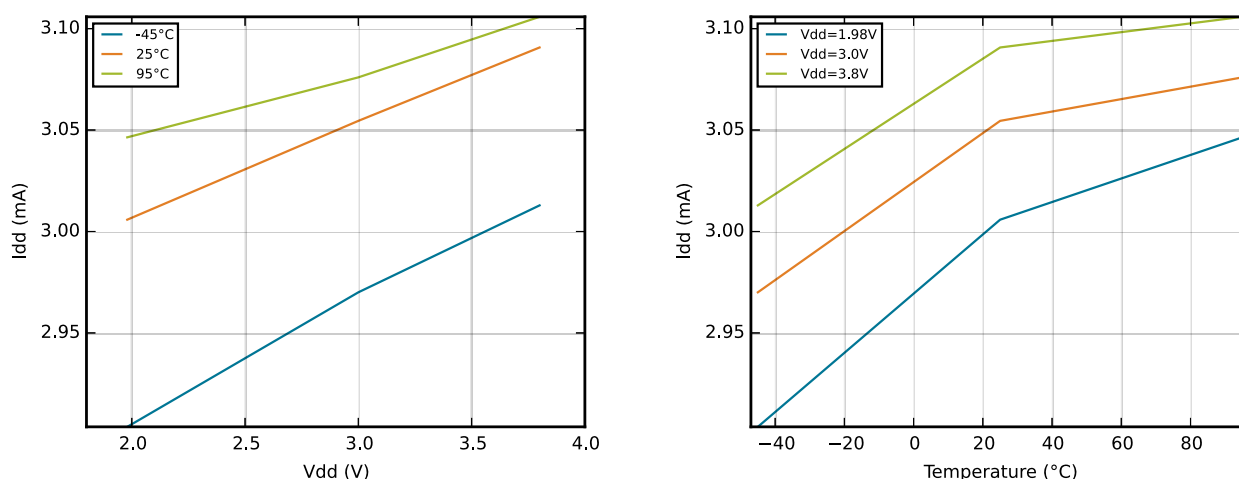


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

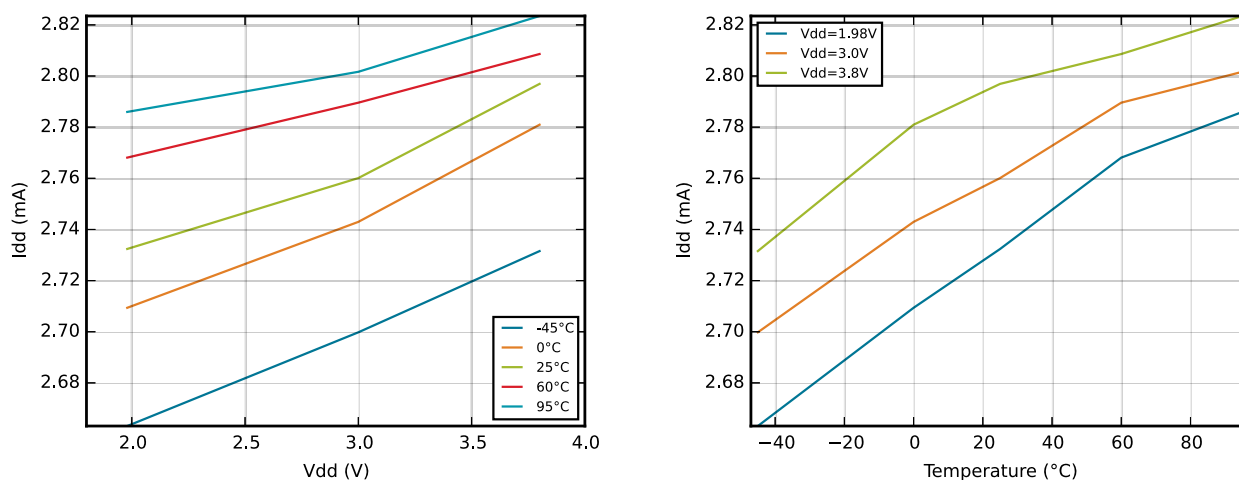


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

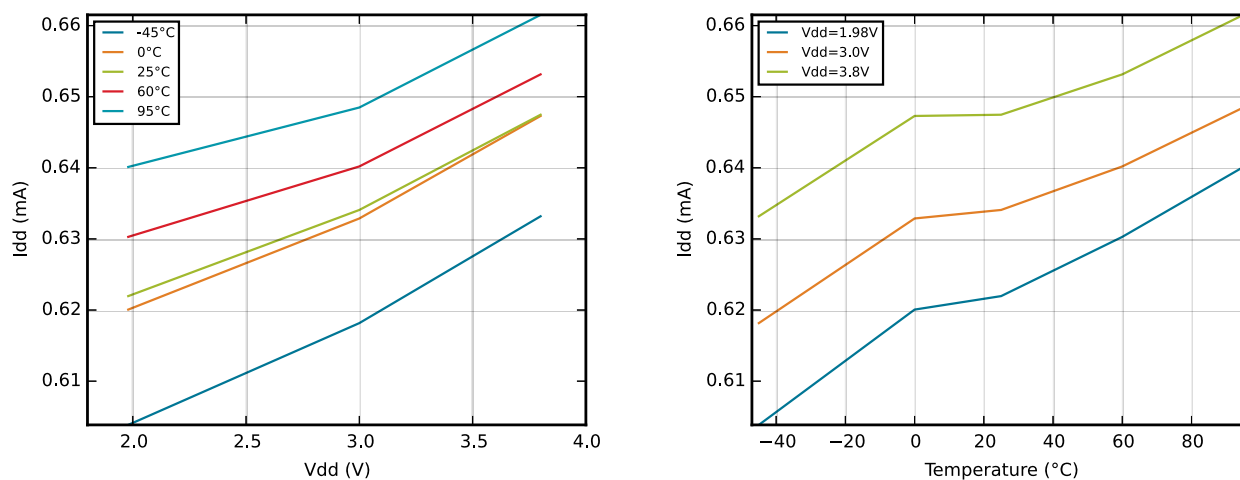


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz

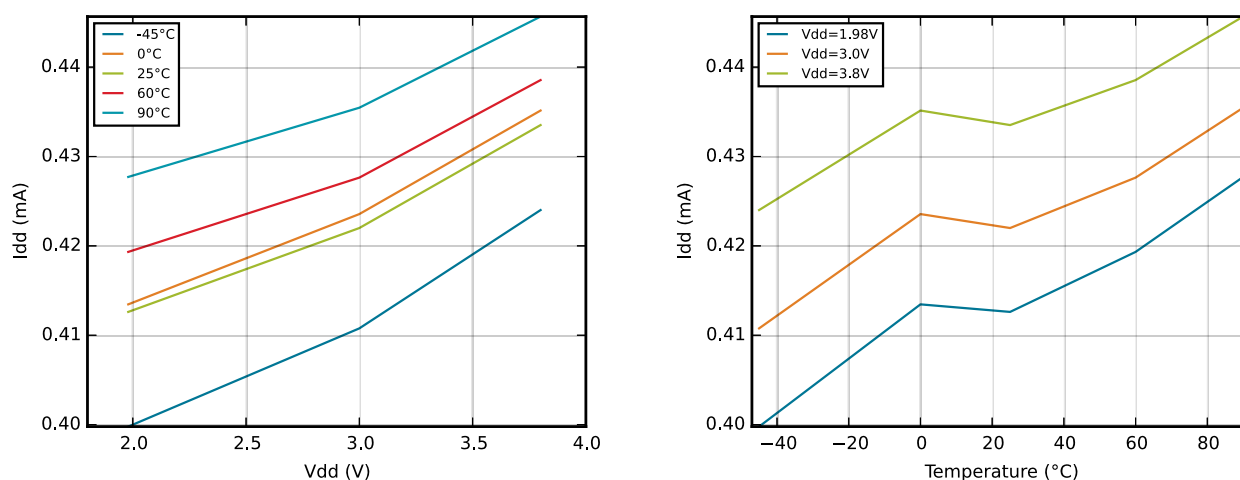


Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

3.7 Flash

Table 3.6. Flash

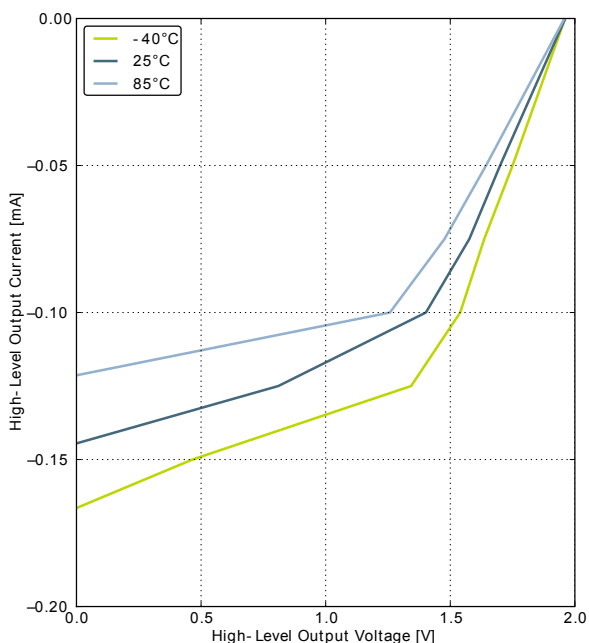
Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹ Measured at 25°C

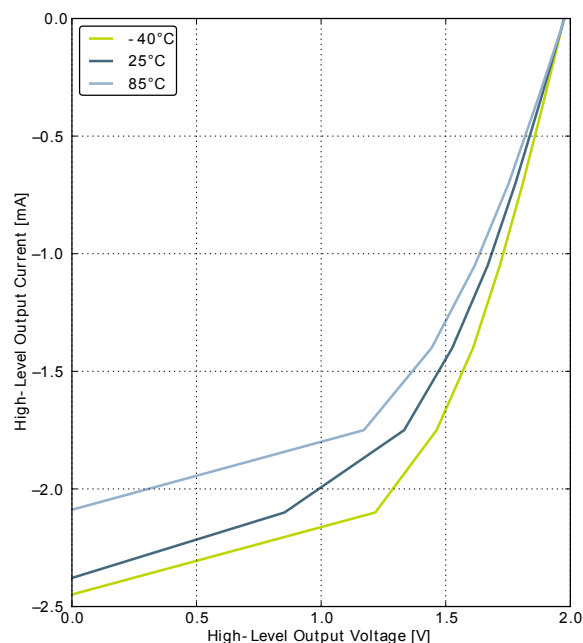
3.8 General Purpose Input Output

Table 3.7. GPIO

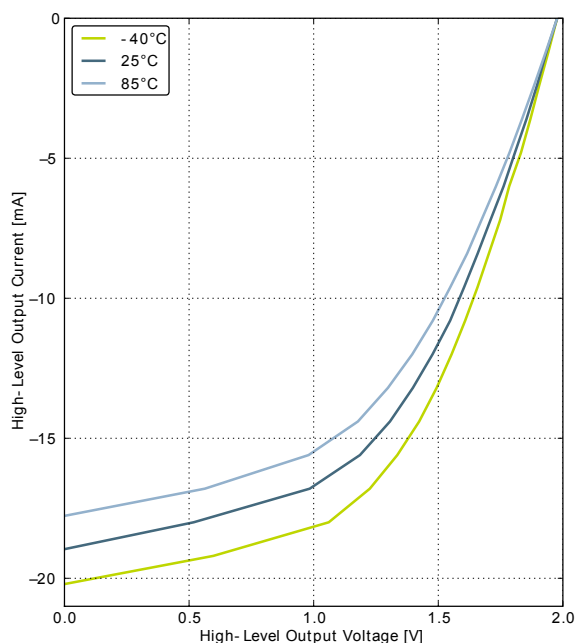
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V

Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage

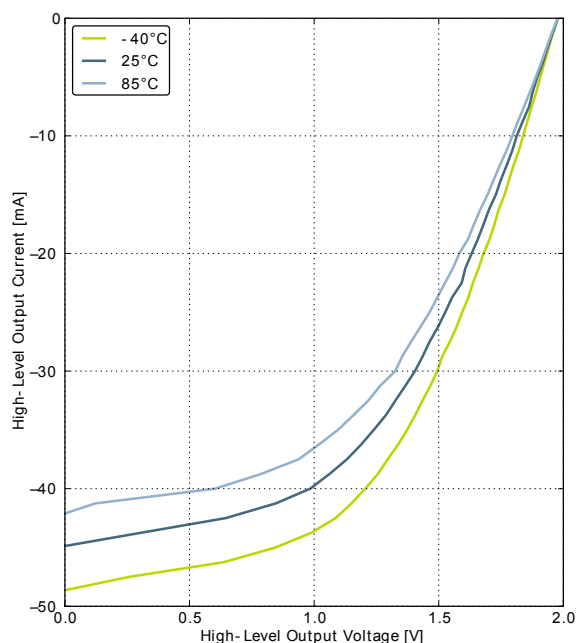
GPIO_Px_CTRL DRIVEMODE = LOWEST



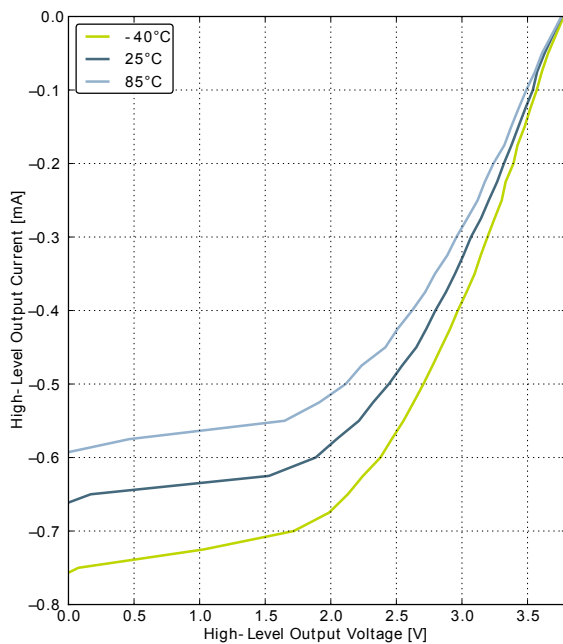
GPIO_Px_CTRL DRIVEMODE = LOW



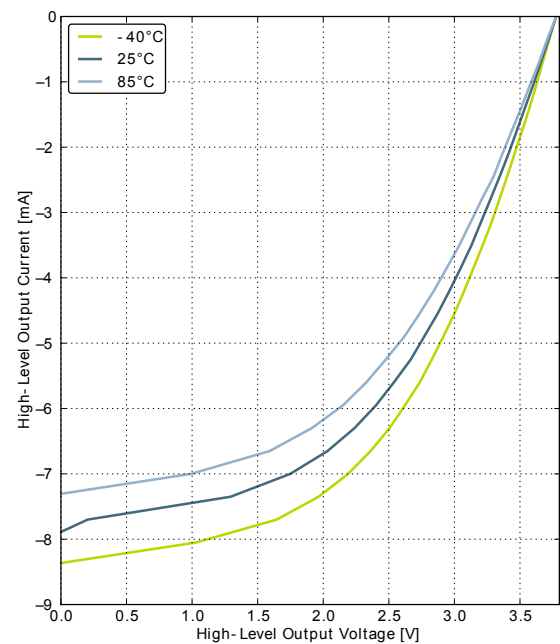
GPIO_Px_CTRL DRIVEMODE = STANDARD



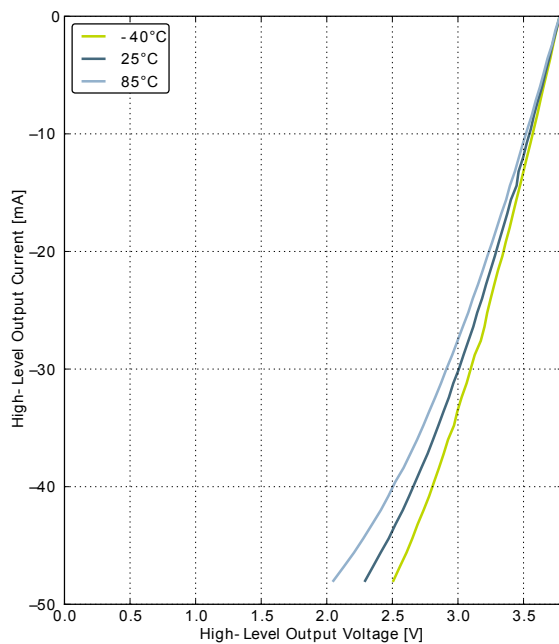
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage

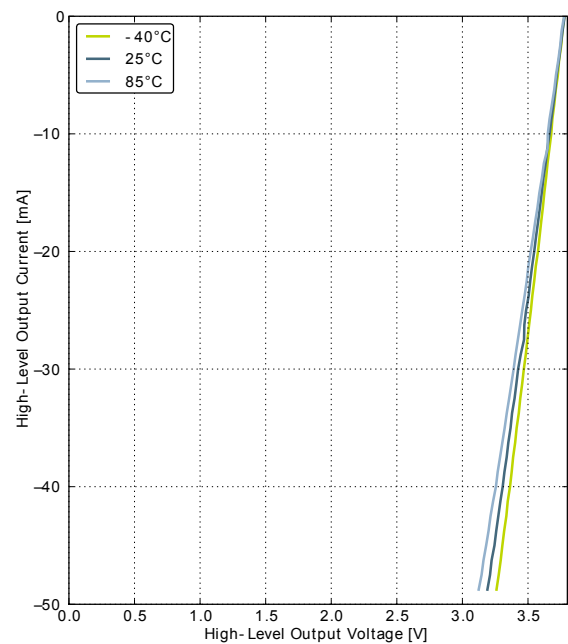
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

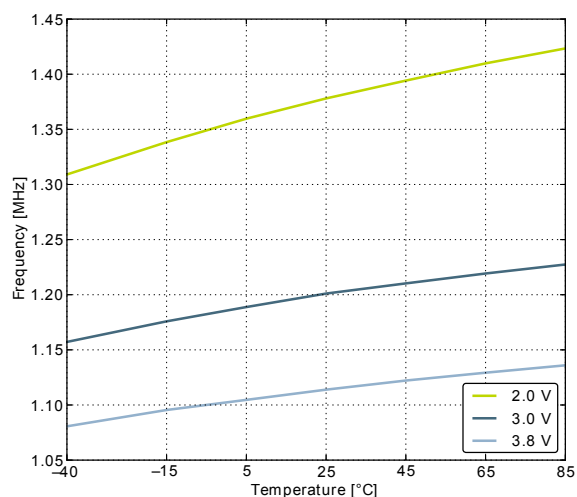
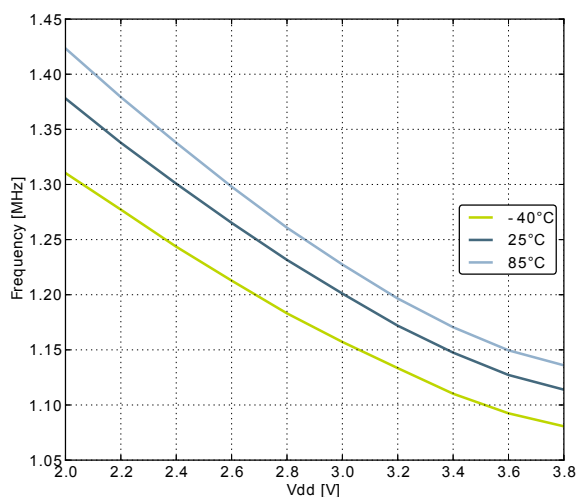
3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	24 MHz frequency band	23.28	24.0	24.72	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{\text{HFRCO_settling}}$	Settling time after start-up	$f_{\text{HFRCO}} = 14 \text{ MHz}$		0.6		Cycles
I_{HFRCO}	Current consumption	$f_{\text{HFRCO}} = 24 \text{ MHz}$		158	184	μA
		$f_{\text{HFRCO}} = 21 \text{ MHz}$		143	175	μA
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		113	140	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		101	125	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		84	105	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		27	40	μA
$\text{TUNESTEP}_{\text{HFRCO}}$	Frequency step for LSB change in TUNING value	24 MHz frequency band		66.8 ¹		kHz
		21 MHz frequency band		52.8 ¹		kHz
		14 MHz frequency band		36.9 ¹		kHz
		11 MHz frequency band		30.1 ¹		kHz
		7 MHz frequency band		18.0 ¹		kHz
		1 MHz frequency band		3.4		kHz

¹The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCREFIN_CH6}	Input range of external positive reference voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
V _{ADCCMIN}	Common mode input range		0		V _{DD}	V
I _{ADCIN}	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input common mode rejection ratio			65		dB
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		392	510	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		μA
I _{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MΩ
R _{ADCFILT}	Input RC filter resistance			10		kΩ
C _{ADCFILT}	Input RC filter/de-coupling capacitance			250		fF
f _{ADCCLK}	ADC Clock Frequency				13	MHz
t _{ADCCONV}	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{ADCACQVDD3}}$	Required acquisition time for VDD/3 reference		2			μs
t_{ADCSTART}	Startup time of reference generator and ADC core in NORMAL mode			5		μs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference		70		dB
$\text{SINAD}_{\text{ADC}}$	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc

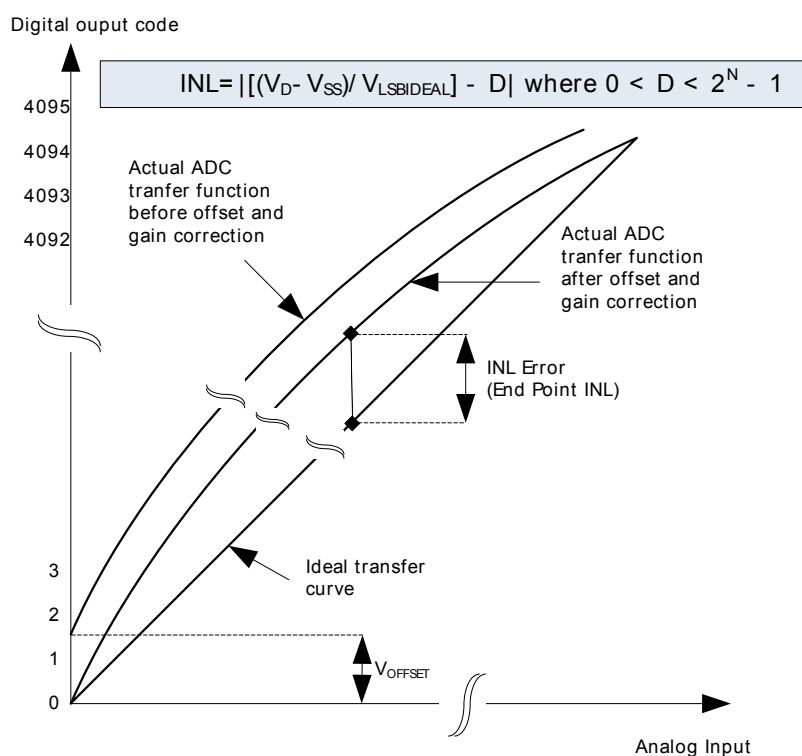
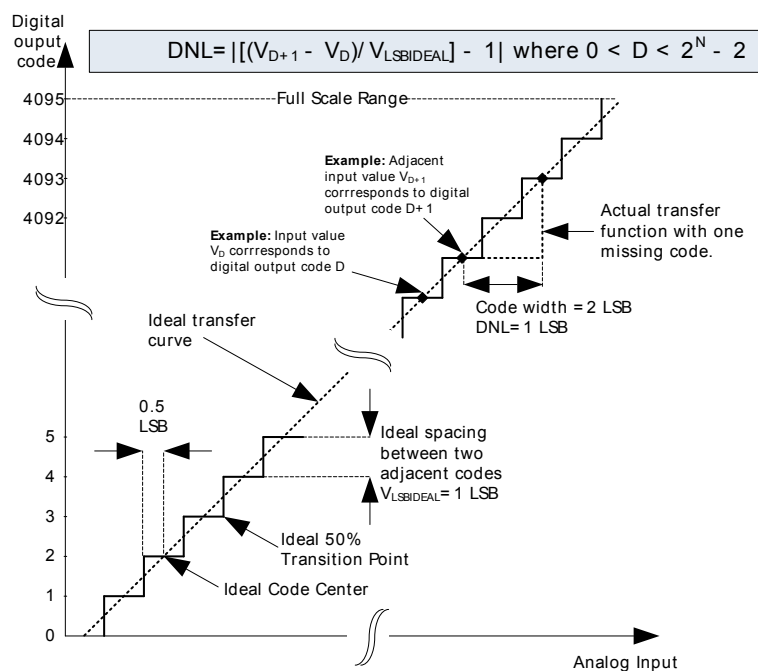
Figure 3.26. Integral Non-Linearity (INL)**Figure 3.27. Differential Non-Linearity (DNL)**

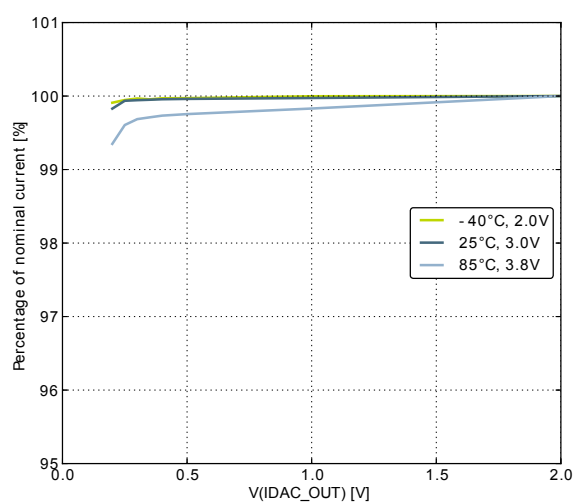
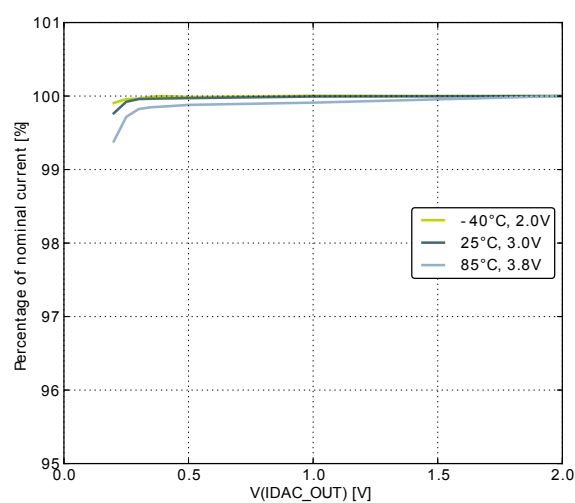
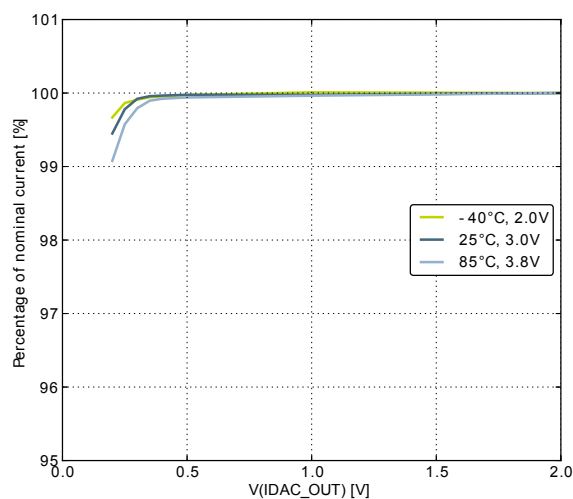
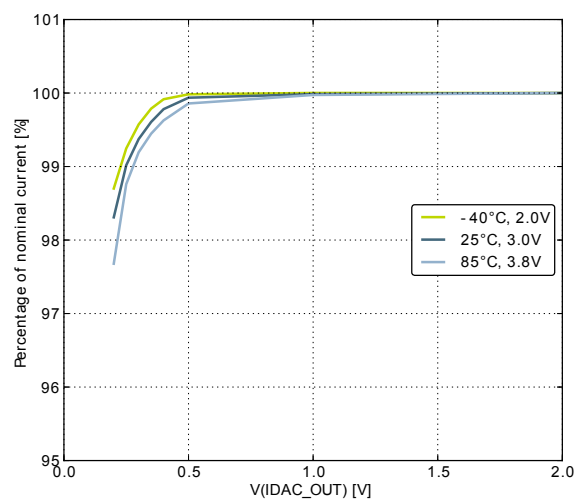
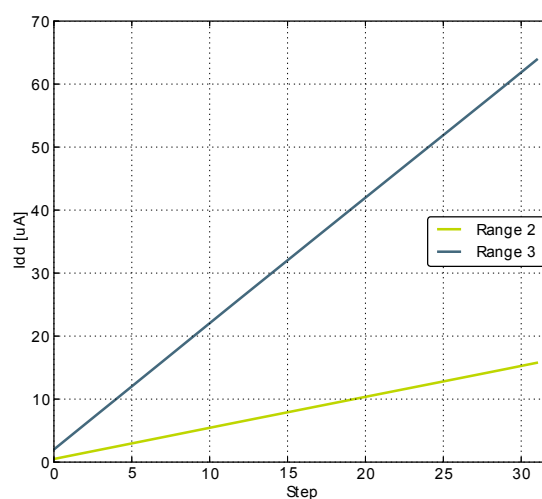
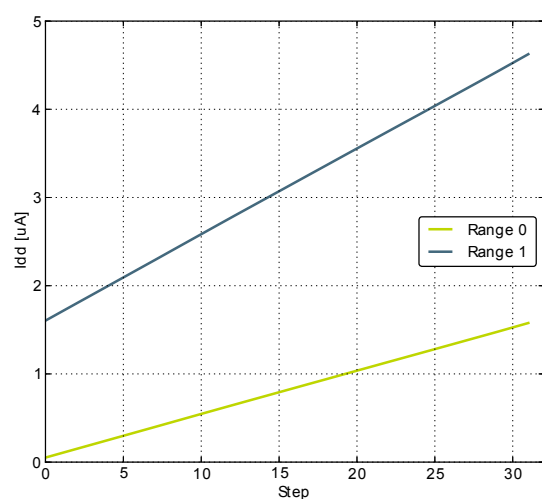
Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT**Range 0****Range 1****Range 2****Range 3****Figure 3.36. IDAC linearity**

Table 3.28. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HPPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 5)$.

Table 3.29. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{HIGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

¹For the minimum HPPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

3.15 USB

The USB hardware in the EFM32HG322 passes all tests for USB 2.0 Full Speed certification. The test report will be distributed with application note "AN0046 - USB Hardware Design Guide" when ready.

Table 3.30. USB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{USBOUT}	USB regulator output voltage		3.1	3.4	3.7	V
I _{USBOUT}	USB regulator output current	BIASPROG=0, T _{AMB} =25°C	55.7	79.4	104.1	mA
		BIASPROG=1, T _{AMB} =25°C	66.0	95.9	126.4	mA
		BIASPROG=2, T _{AMB} =25°C	94.6	146.5	188.1	mA
		BIASPROG=3, T _{AMB} =25°C	80.4	128.3	176.0	mA

3.16 Digital Peripherals

Table 3.31. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		7.5		μA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.25		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		μA/ MHz
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I _{AES}	AES current	AES idle current, clock enabled		2.5		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		μA/ MHz
I _{PRS}	PRS current	PRS idle current		2.81		μA/ MHz
I _{DMA}	DMA current	Clock enable		8.12		μA/ MHz

7 Revision History

7.1 Revision 1.00

December 4th, 2015

Updated all specs with results of full characterization.

Updated part number to revision B.

Added the USB electrical specifications table.

7.2 Revision 0.91

May 6th, 2015

Updated current consumption table for energy modes.

Updated GPIO max leakage current.

Updated startup time for HFXO and LFXO.

Updated current consumption for HFRCO and LFRCO.

Updated ADC current consumption.

Updated IDAC characteristics tables.

Updated ACMP internal resistance.

Updated VCMP current consumption.

7.3 Revision 0.90

March 16th, 2015

Note

This datasheet revision applies to a product under development. It's characteristics and specifications are subject to change without notice.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Updated GPIO electrical characteristics.

Updated Max ESR_{HFXO} value for Crystal Frequency of 25 MHz.

Updated LFRCO plots.

Updated HFRCO table and plots.

Updated ADC table and temp sensor plot.

Added DMA current in Digital Peripherals section.

Updated block diagram.

Corrected leadframe type to matte-Sn.

List of Equations

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