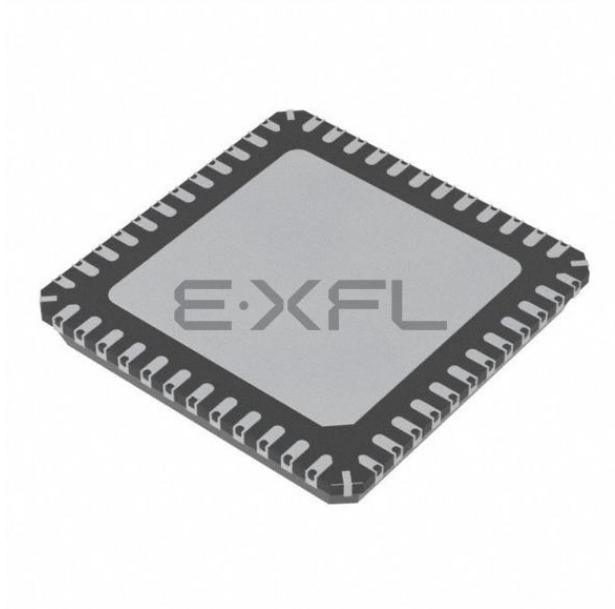

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qvxuma1

1.2 Abbreviations

The following acronyms and terms are used within this document. List see in Table 2.

Table 2 Acronyms

Acronyms	Name
ALU	Arithmetic Logic Unit
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
DAP	Device Access Port
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
FSR	Full Scale Range
ICU	Interrupt Control Unit
IRAM	Internal Random Access Memory - Internal Data Memory
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
MCU	Micro Controller Unit
MDU	Multiplication Division Unit
MMC	Monitor Mode Control
MSB	Most Significant Bit
NMI	Non Maskable Interrupt
OCDS	On Chip Debug Support
OTP	One Time Programmable
OSC	Oscillator
PC	Program Counter
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PMU	Power Management Unit
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit

Table 4 Power mode configurations

Module/function	Active Mode	Stop Mode	Sleep Mode	Comment
CYCLIC Modes	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ cyclic sense/OFF	cyclic sense with HS, VDDEXT; wake-up from cyclic wake needs MC for entering Sleep Mode / Stop Mode again
Measurement Unit	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/HALT	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (20 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON	ON	ON	for cyclic wake-up

1) Cannot not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, the LIN and MON inputs are activated after power-on reset only. GPIO ports as wake-up sources are disabled by default after power-on reset. The application software can reconfigure the wake-up sources according to the application needs.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor and GPIO input individually.

3.1 Power Management Unit (PMU)

The purpose of the power management unit is to ensure the fail safe behavior of embedded automotive systems. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external sensor supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities, especially the reset behavior of the embedded MCU, including the test hardware. All these functions are controlled by finite state machines. The system master functionality of the PMU forces the generation of an independent logic supply (Power Down Supply) and system clock (LP_CLK). Therefore the PMU needs a module internal logic supply and system clock which works independently of the MCU clock.

The following state diagram shows the available modes of the device.

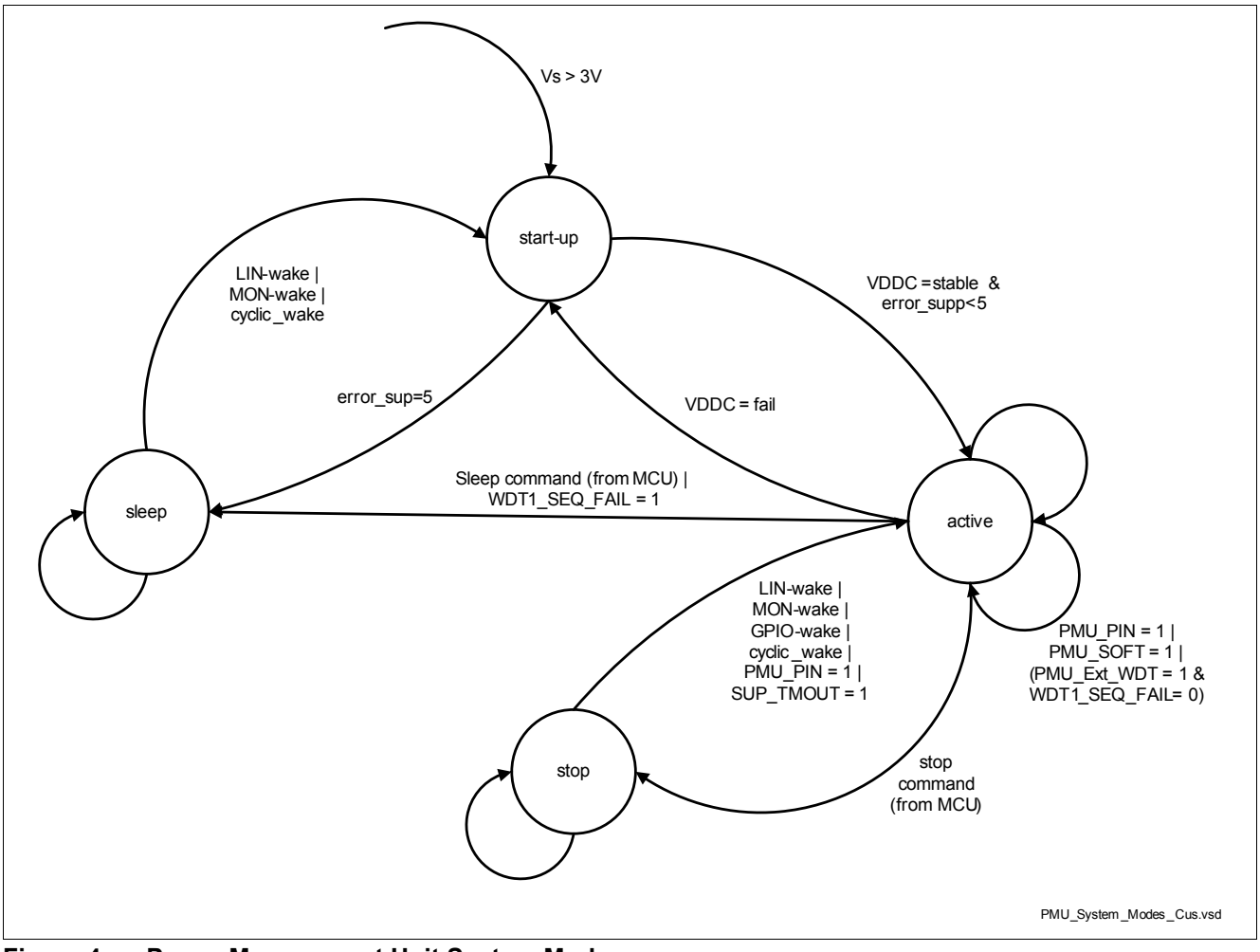


Figure 4 Power Management Unit System Modes

Table 5 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent Supply Voltage Generation for PMU	This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC).
LP_CLK (= 20 MHz)	- Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1
LP_CLK2 (= 100 kHz)	Clock Source for PMU	This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features
VDDEXT (Hall Sensor Supply)	Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor)
PMU-XSFR	All PMU relevant Extended Special Function Registers	This module contains all PMU relevant registers, which are needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module.
PMU-WMU	Wake-up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CYCMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions within cyclic mode.
PMU-CMU	Clock Management Unit of the PMU	This block is responsible for controlling all clocking actions within the PMU.
PMU-RMU	Reset Management Unit of the PMU	This block is responsible for generating all system required resets.

3.2 System Control Unit

3.2.1 System Control Unit - Power Modules

The System Control Unit of the power modules consists of the following sub-modules:

- Reset Control Unit (RCU): generation of all required subsystem resets
- Clock Generation Unit (CGU): providing all required clocks to the analog subsystem
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags
- Power Control Unit (PCU): takes over control when device enters and exits Sleep Mode and Stop Mode
- System Status Unit (SSU): controls mode changes due to system failures
- External Watchdog (WDT1): independent system watchdog to monitor system activity

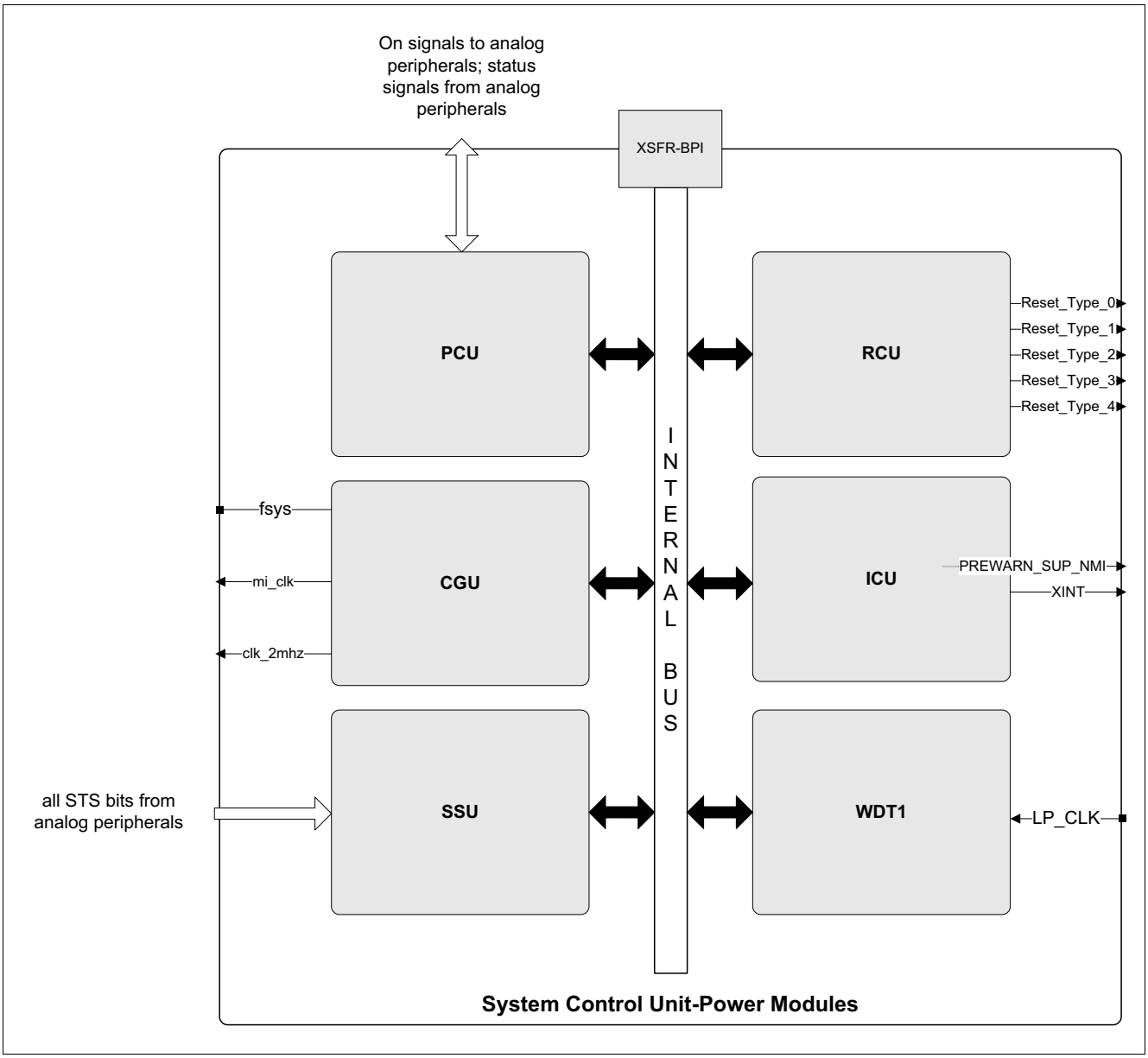


Figure 9 Block Diagram of System Control Unit - Power Modules

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

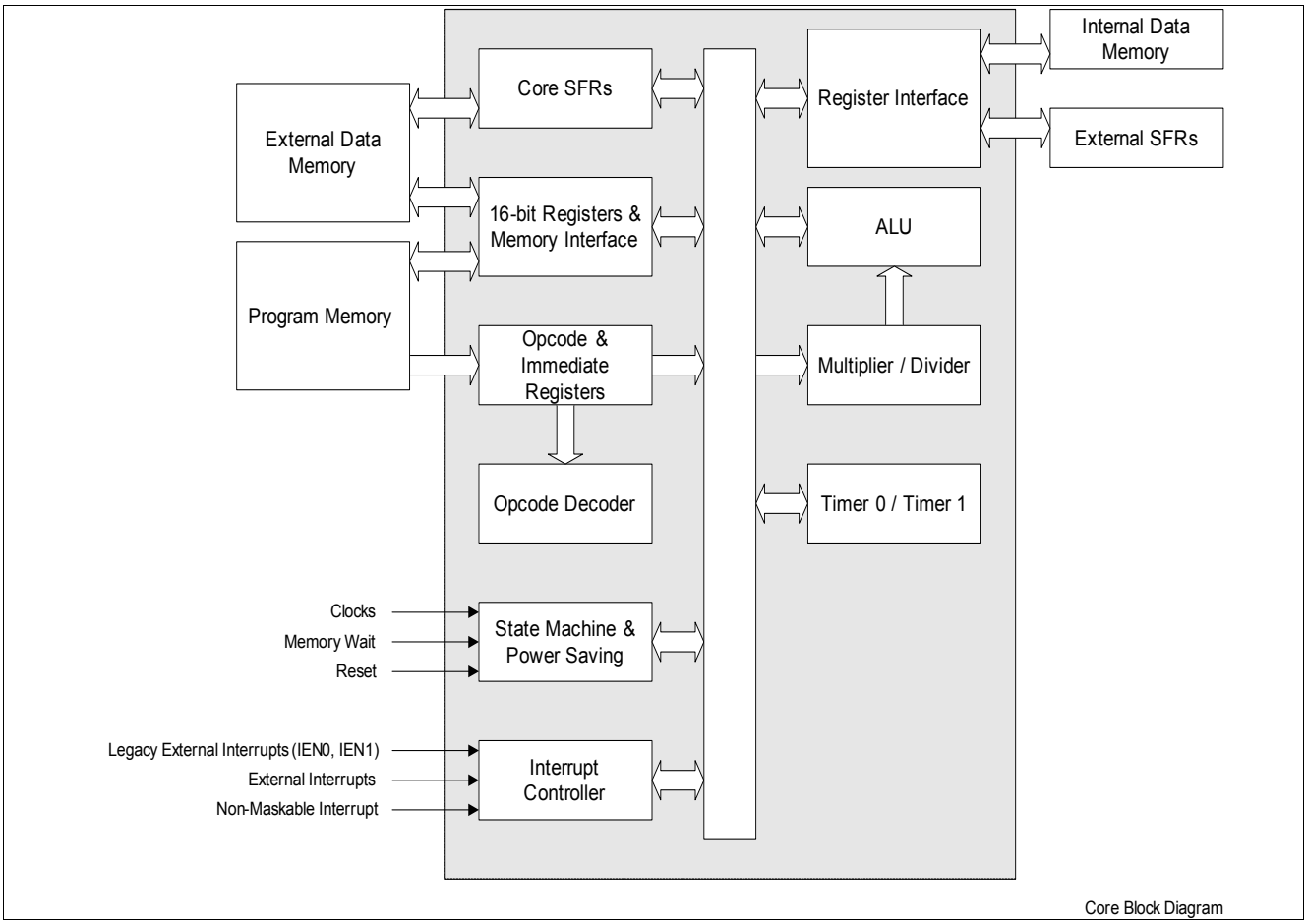


Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

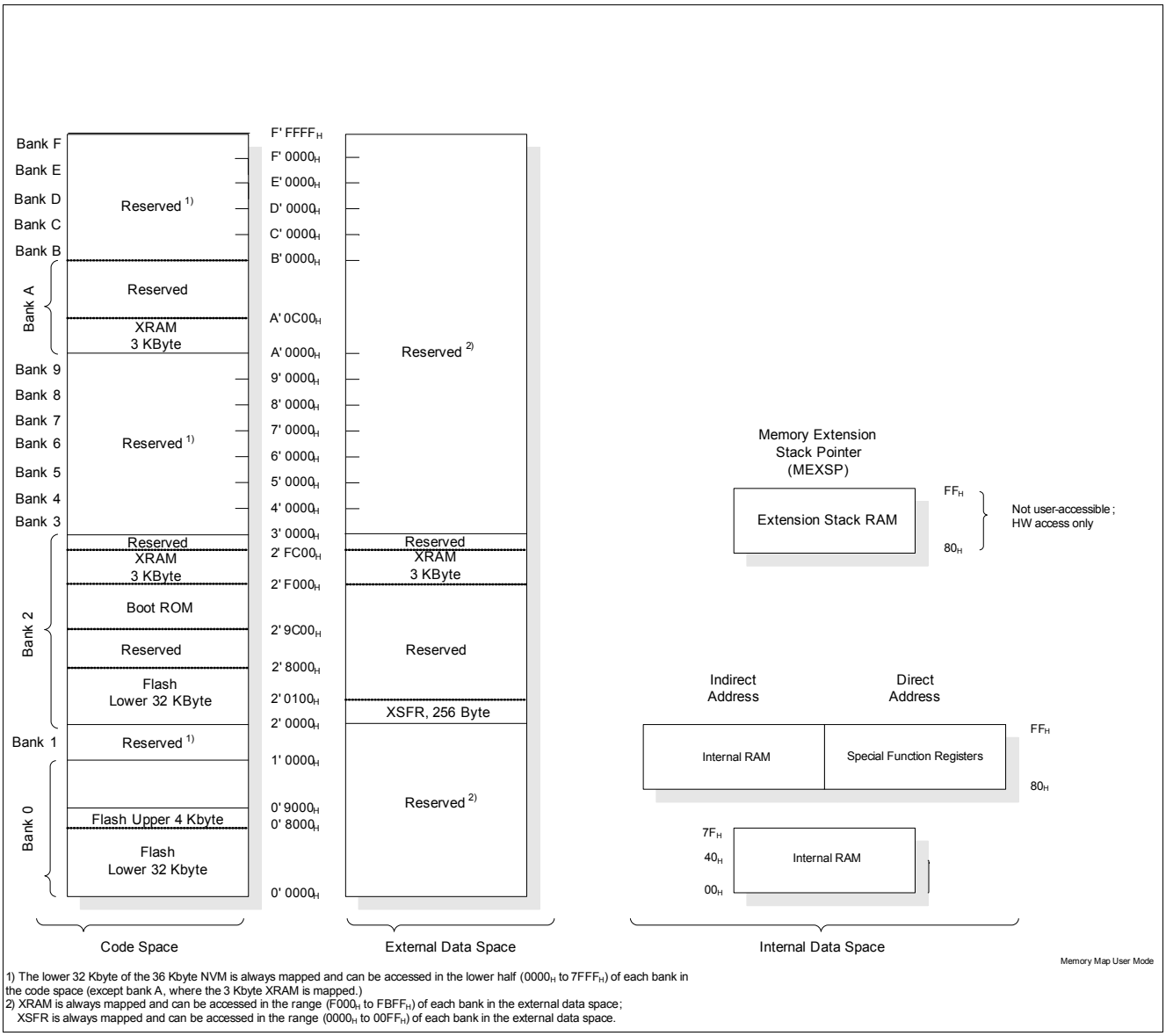
The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.4 Memory Architecture

The TLE9832 CPU manipulates operands in the following memory spaces:

- 36 kByte of Flash memory in code space
- BootROM memory in code space
- 256 Byte of internal RAM data memory in internal data space
- 3 kByte of XRAM memory in code space and external data space (XRAM can be read/written as program memory or external data memory)
- 128 Byte of special function registers SFR in internal data space
- 256 Byte of special function registers XSFR in external data space.

Figure 11 illustrates the memory address spaces of the TLE9832.



1) The lower 32 Kbyte of the 36 Kbyte NVM is always mapped and can be accessed in the lower half (0000_H to $7FFF_H$) of each bank in the code space (except bank A, where the 3 Kbyte XRAM is mapped.)
2) XRAM is always mapped and can be accessed in the range ($F000_H$ to $FBFF_H$) of each bank in the external data space; XSFR is always mapped and can be accessed in the range (0000_H to $00FF_H$) of each bank in the external data space.

Figure 11 TLE9832 Memory Map

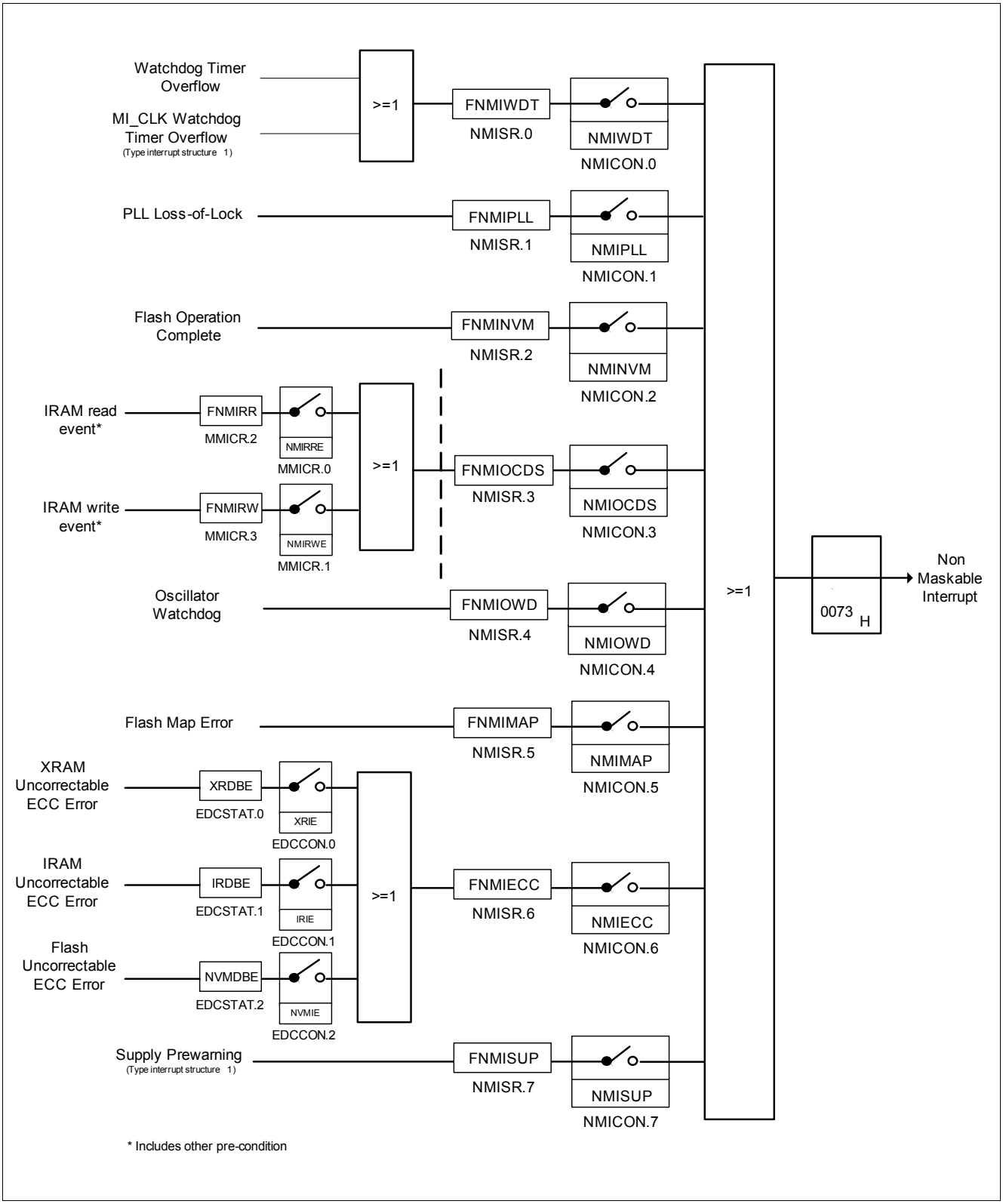


Figure 19 Non-Maskable Interrupt Request Source

3.13 Timer 3

Timer 3 can function as timer or counter. When functioning as a timer, Timer 3 is incremented in periods based on the system clock. When functioning as a counter, Timer 3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer 3 can be configured in four different operating modes to use in a variety of applications, see **Table 8**.

Table 8 Timer 3 Modes

Mode	Sub-Mode	Operation
0	**-**	**13-Bit Timer** The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**a**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter.
1	**b**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable a single shot measurement on a preset channel with the measurement unit.
1	**c**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable the LIN Baudrate Measurement.
2	**-**	**8-Bit Timer with Auto-reload** The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow.
3	**a**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters.
3	**b**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters. In this mode the 100 kHz Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as an counter which counts the time between the edges.

3.14 Capture/Compare Unit 6 (CCU6)

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status Bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and Low Side Switches)
- 16-Bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-Bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

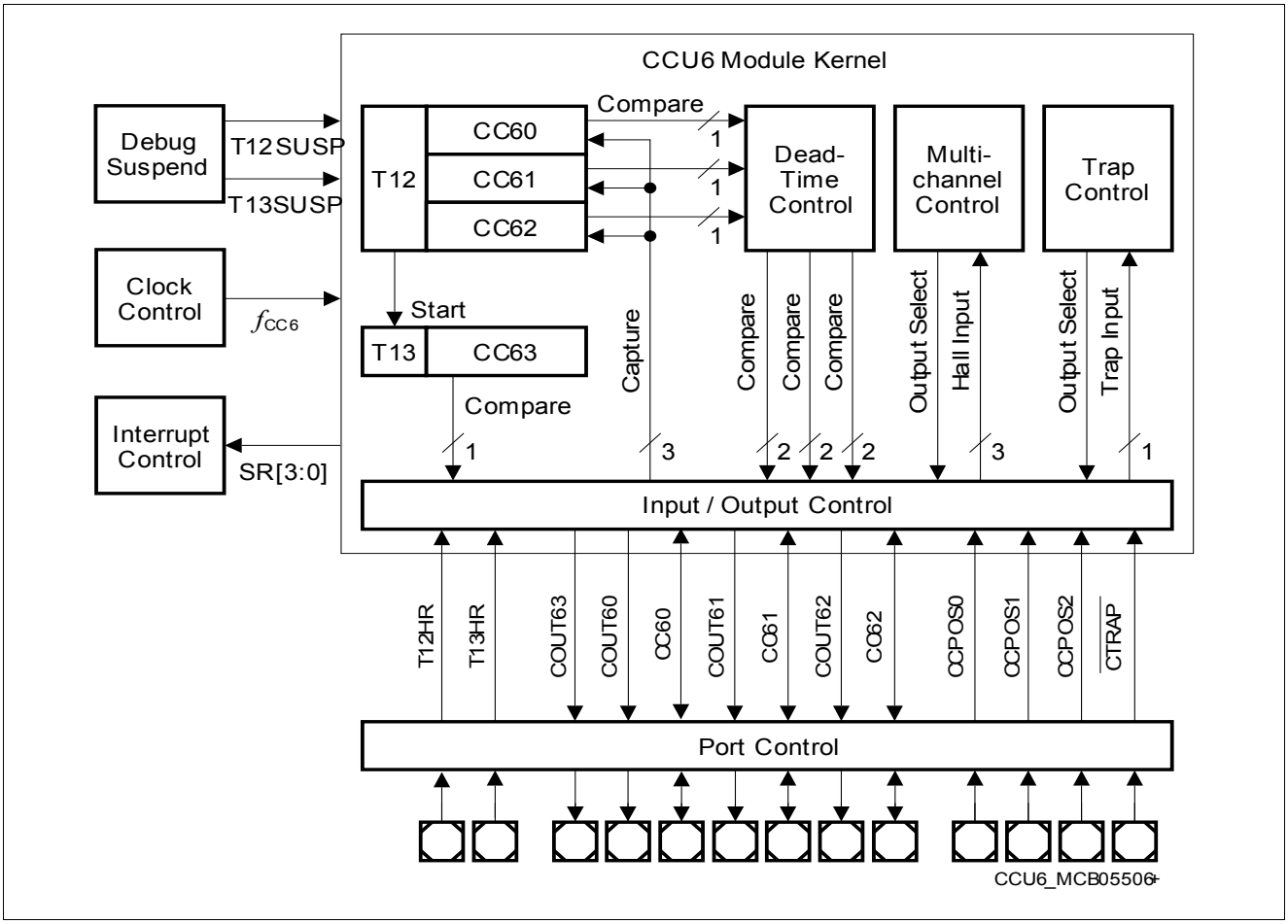


Figure 22 CCU6 Block Diagram

3.20 Analog Digital Converter (ADC1)

The TLE9832 includes a high-performance 10-Bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN1, AN3 - AN5, AN7.

Features

- Successive approximation
- 8-Bit or 10-Bit resolution
- 8 analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21 High Voltage Monitor Input

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at each high-voltage MON_IN pin in low-power mode. Each input is sensitive to an input level monitoring. It is available when the module is switched to Active Mode via the MON_int (internal signal name) output with a small filter delay of typical 2 µs.

Features

- High-voltage input with V_S/2 threshold voltage
- Edge sensitive wake capability for power saving modes
- Level sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC1 in Active Mode, using adjustable threshold values (see also **Chapter 3.20**).

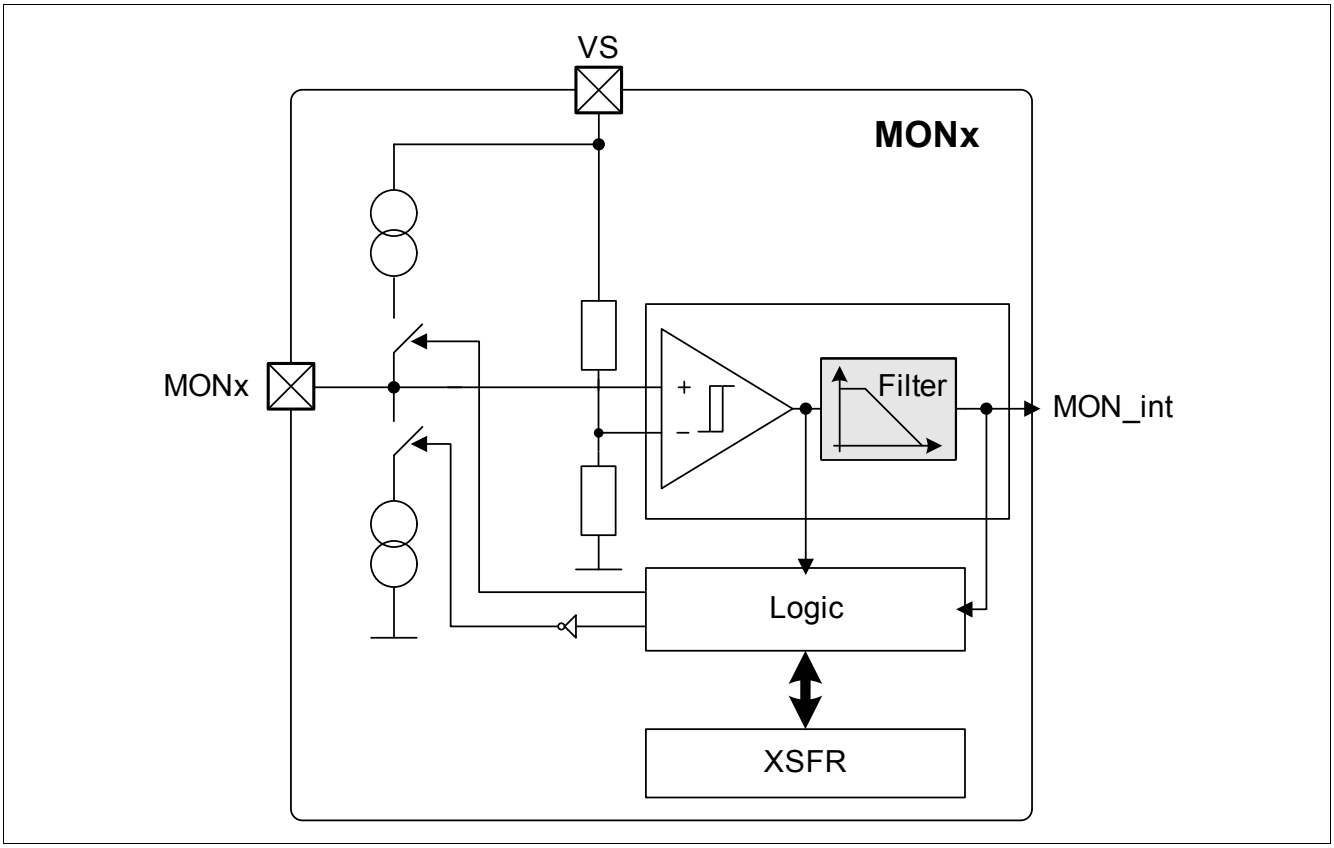


Figure 27 Monitoring Input Block Diagram

3.23 Low Side Switches

The general purpose Low Side Switches are intended to control an on-board relay. They include an over-current detection function.The module is designed for on-board connections.

Features

- Multi purpose Low Side Switch
  - configurable over-current protection with automatic shutdown
  - configurable over-temperature protection with automatic shutdown
- Intended for relay driver
  - PWM relay driver
  - simple relay driver
- Integrated clamping
- PWM capability up to 25 kHz
- Selectable PWM source: PWM-Unit or CCU6

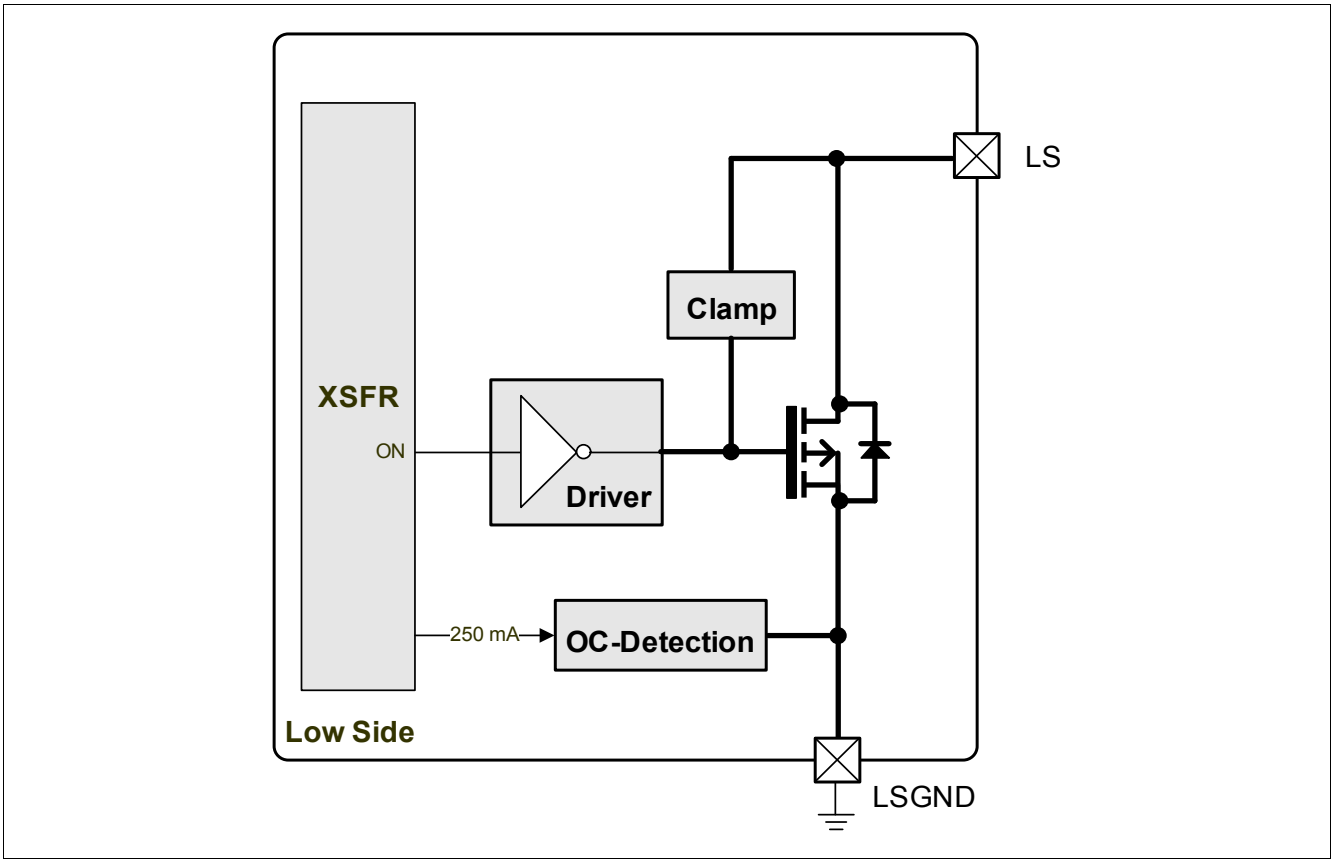


Figure 29 Module Block Diagram

4.7 ESD Tests

Note: Test for ESD robustness to IEC61000-4-2 “gun test” (150pF, 330Ω) will be performed. The result and test condition can be provided in a test report

Table 13 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND	> 6	kV	1)positive pulse
ESD at pin LIN, versus GND	< -6	kV	1)negative pulse

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau).

5 Electrical Characteristics

This chapter includes all relevant Electrical Characteristics of the product TLE9832.

5.1 General Characteristics

5.1.1 Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings [1)]

T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages Supply Pins							
Supply voltage VS	V_S	-0.3	–	40	V	–	P_5.1.1
Voltage VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_5.1.2
Voltage VDDP	V_{DDP}	-0.3	–	6.0	V	t < 100ms, in Stop Mode only	P_5.1.50
Output voltage VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_5.1.3
Voltage VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_5.1.4
Voltages High Voltage Pins							
Battery Voltage VBAT_SENSE	V_{BAT_SENSE}	-27	–	40	V	–	P_5.1.5
Output voltage HS	V_{HS}	-0.3	–	40	V	–	P_5.1.6
Input voltage at LIN	V_{LIN}	-27	–	40	V	–	P_5.1.7
Input voltage MON_x	$V_{MON\_X\_maxrate}$	-40	–	40	V	–	P_5.1.8
Input voltage LS	V_{LS}	-0.3	–	40	V	–	P_5.1.9
Voltages GPIOs							
Voltage on any port pin	V_{in}	-0.3	–	V_{DDP} +0.3	V	V_{IN} < 5.4V	P_5.1.10
Voltages Others							
Input voltage VAREF	V_{AREF}	-0.3	–	5.3	V	–	P_5.1.11
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_5.1.12
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_5.1.13
ESD Resistivity							
ESD Resistivity **HBM** all pins	V_{ESD1}	-2	–	2	kV	EIA/JESD 22-A114B (1.5kΩ, 100pF)	P_5.1.14

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;(LIN Spec 2.1; Param. 31)	P_5.6.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kBit/s)	t_{duty1}	0.396	–	–		[5] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 27)	P_5.6.19
Duty cycle D2 Normal Slope Mode (for worst case at 20 kBit/s)	t_{duty2}	–	–	0.581		[6] duty cycle 2 TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)	P_5.6.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN Spec 2.1; Param. 32)	P_5.6.23

5.7 High-Speed Synchronous Serial Interface

The table below provides the SSC timing in the TLE9832.

Table 29 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		–	P_5.7.1
MTSR delay from SCLK	t_1	10	–	–	ns	–	P_5.7.2
MRST setup to SCLK	t_2	10	–	–	ns	–	P_5.7.3
MRST hold from SCLK	t_3	15	–	–	ns	–	P_5.7.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.

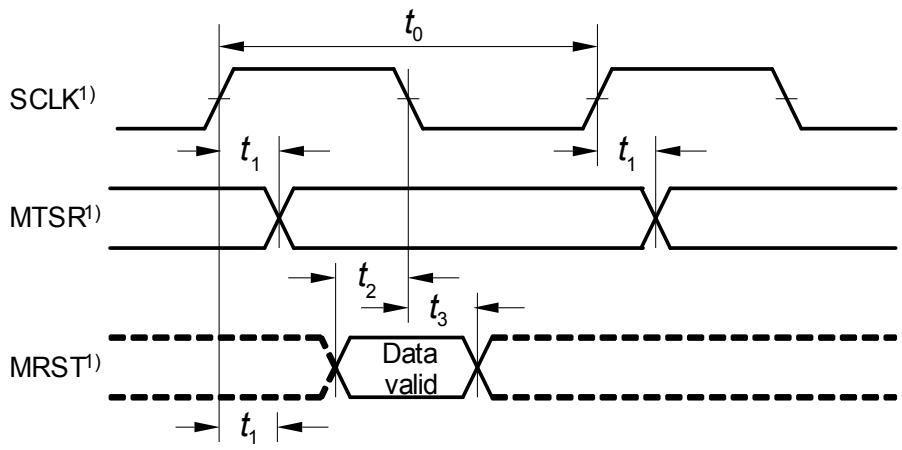


Figure 32 SSC Master Mode Timing

5.8 Measurement Unit

5.8.1 Analog Digital Converter 8-Bit

Table 30 DC Specifications ADC 8 Bit

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resolution	–	–	8	–	Bit	–	P_5.8.1
Offset error	–	-10	4	+10	mV	–	P_5.8.2
Gain single-ended input mode	GSE	–	1	–		–	P_5.8.3
Input voltage single-ended mode	V_{ainp},V_{ainn}	0	–	V_{DD1V5_A}	V	–	P_5.8.4
Gain differential input mode	GDF		1.24	–	–	–	P_5.8.5
Common input voltage in differential mode	V_{icm}	0.5	0.6	V_{DDP}/2 +0.1	–	V_{icm}=(V_{ainp} + V_{ainn})/2	P_5.8.6
Gain error	–	-5	1.5	+5	%FSR	–	P_5.8.7
Differential nonlinearity (DNL)	–	-1.5	0.5	+1.5	LSB	–	P_5.8.8
Integral Nonlinearity (INL)	–	-3	±1.5	3	LSB	–	P_5.8.9

5.8.2 Measurement Unit (VBAT_SENSE - Supply Voltage Attenuator)

Table 31 Supply voltage signal conditioning

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Battery Voltage Measurement V_{BAT_SENSE}							
Nominal operating input voltage range[1)]	V_{S/BAT_SENSE}	3	–	20	V	Max. value corresponds to typ. ADC full scale input	P_5.8.10
Measurement input resistance	$R_{in,VS/VBAT\_SENSE}$	200	289	380	kΩ	PD_N=1 (on-state)	P_5.8.11
Measurement input leakage current	I_{leak}	0	–	1.0	µA	PD_N=0 (off-state), V_{BAT_SENSE}=13.5V	P_5.8.12
Overall (calibrated) measurement accuracy after A/D-conversion[2)]							
V_{BAT_SENSE} / V_s 8-bit ADC	$\Delta V_{BATADC8B}$	-250	–	250	mV	V_s= 5.5V to 18V, T_j = 40..85°C	P_5.8.13
V_{BAT_SENSE} / V_s 10-bit ADC	$\Delta V_{BATADC10B}$	-200	–	200	mV	V_s= 5.5V to 18V, T_j = 40..85°C	P_5.8.14

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis	$I_{OLONhys}$	1	–	4	mA	[1] OL_EN = 1; HS_ON = 1	P_5.11.26
Off-state open load detection							
Open load voltage threshold	V_{OLth1}	0.5* V_S	0.67 *V_S	0.85* V_S	V	I_{OL_test}; open load activated; OLTH_SEL = 1	P_5.11.27
Hysteresis	V_{OLhys}	0.1* V_S	–	0.3* V_S	V	IOL_SEL = 1	P_5.11.28
Open load output current	I_{OL_test}	-150	–	-25	µA	IOL_SEL = 0	P_5.11.29
Open load output current	I_{OL_test}	-1.5	–	-0.5	mA	IOL_SEL = 1	P_5.11.30
Cyclic sense mode							
ON-State Resistance	$R_{ON,static}$	–	–	40	Ω	Definition: differential resistance or resistance at 40 mA	P_5.11.31
Output Slew Rate (rising)	SR_{rise} [1]	1	–	–	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω [1]	P_5.11.32
Output Slew Rate (falling)	SR_{fall} [1]	–	–	-1	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω	P_5.11.33
Delay Time CYCLIC_ON-HS	t_{IN-CYC}	–	–	2	µs	ON =1 to 10% of V_S RL=300Ω	P_5.11.34
Turn-ON time	t_{ON}	–	–	15	µs	V_S =13.5V ON=1 to 90% R_L =300Ω	P_5.11.35
Turn-OFF time	t_{OFF}	–	–	15	µs	V_S =13.5V ON=0 to 10% of V_S R_L =300Ω; T_j=25°C	P_5.11.36

1) Not subject to production test, specified by design.