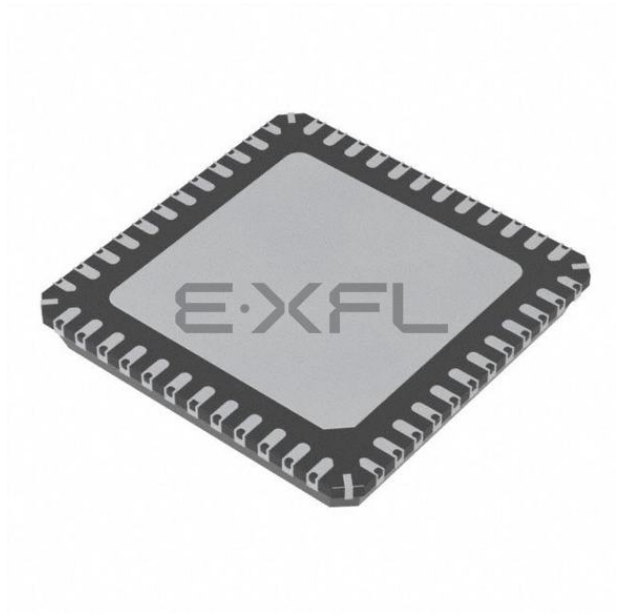

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Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qvxuma2

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1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832 device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9832QV	40 MHz	1	5	36 kByte	11	no
TLE9832QX	40 MHz	1	5	36 kByte	11	no

1.2 Abbreviations

The following acronyms and terms are used within this document. List see in Table 2.

Table 2 Acronyms

Acronyms	Name
ALU	Arithmetic Logic Unit
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
DAP	Device Access Port
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
FSR	Full Scale Range
ICU	Interrupt Control Unit
IRAM	Internal Random Access Memory - Internal Data Memory
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
MCU	Micro Controller Unit
MDU	Multiplication Division Unit
MMC	Monitor Mode Control
MSB	Most Significant Bit
NMI	Non Maskable Interrupt
OCDS	On Chip Debug Support
OTP	One Time Programmable
OSC	Oscillator
PC	Program Counter
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PMU	Power Management Unit
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit

Table 2 Acronyms

Acronyms	Name
ROM	Read Only Memory
SCK	SSC Clock
SFR	Special Function Register
SOW	Short Open Window (for WDT1)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
SSU	System Status Unit
TMS	Test Mode Select
UART	Universal Asynchronous Receiver Transmitter
UDIG	Universal Digital Controller for ADC1
VBG	Voltage reference Band Gap
WDT	Watchdog timer
WMU	Wake-up Management Unit
XRAM	On-Chip eXternal Data Memory
XSFR	On-Chip eXternal Special Function Register

Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately. For cyclic sense in Stop Mode VDDEXT can be switched on periodically. Furthermore cyclic sense allows to sense dedicated GPIO port states and transitions when in Stop Mode.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 4 Power mode configurations

Module/function	Active Mode	Stop Mode	Sleep Mode	Comment
VDD1V5PD	ON	ON	ON	Power Down Supply
VPRE, VDDP, VDDC	ON	ON (no dynamic load)	OFF	–
VDDEXT	ON/OFF	ON (no dynamic load)/OFF cyclic ON/OFF	OFF	–
HS	ON/OFF	cyclic ON/OFF	cyclic ON/OFF	cyclic sense
LSx	ON/OFF	OFF	OFF	–
PWM GEN.	ON/OFF	OFF	OFF	–
LIN TRx	ON/OFF	wake-up only/ OFF	wake-up only/ OFF	–
MON1 - MON5 (wake-up)	n.a.	disabled/static/cyclic	disabled/static/ cyclic	cyclic: combined with HS=on
MON1 - MON5 (measurement)	ON/OFF	OFF	OFF	available on four channels
VS sense	ON/OFF brownout detection	brownout detection	brownout detection	brownout detection done in PCU
VBAT_SENSE	ON/OFF	OFF	OFF	–
GPIO 5V (wake-up)	n.a.	disabled/static/cyclic	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	OFF	OFF	–

3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

Features

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/µs max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 µA)
- Cyclic sense option together with GPIOs

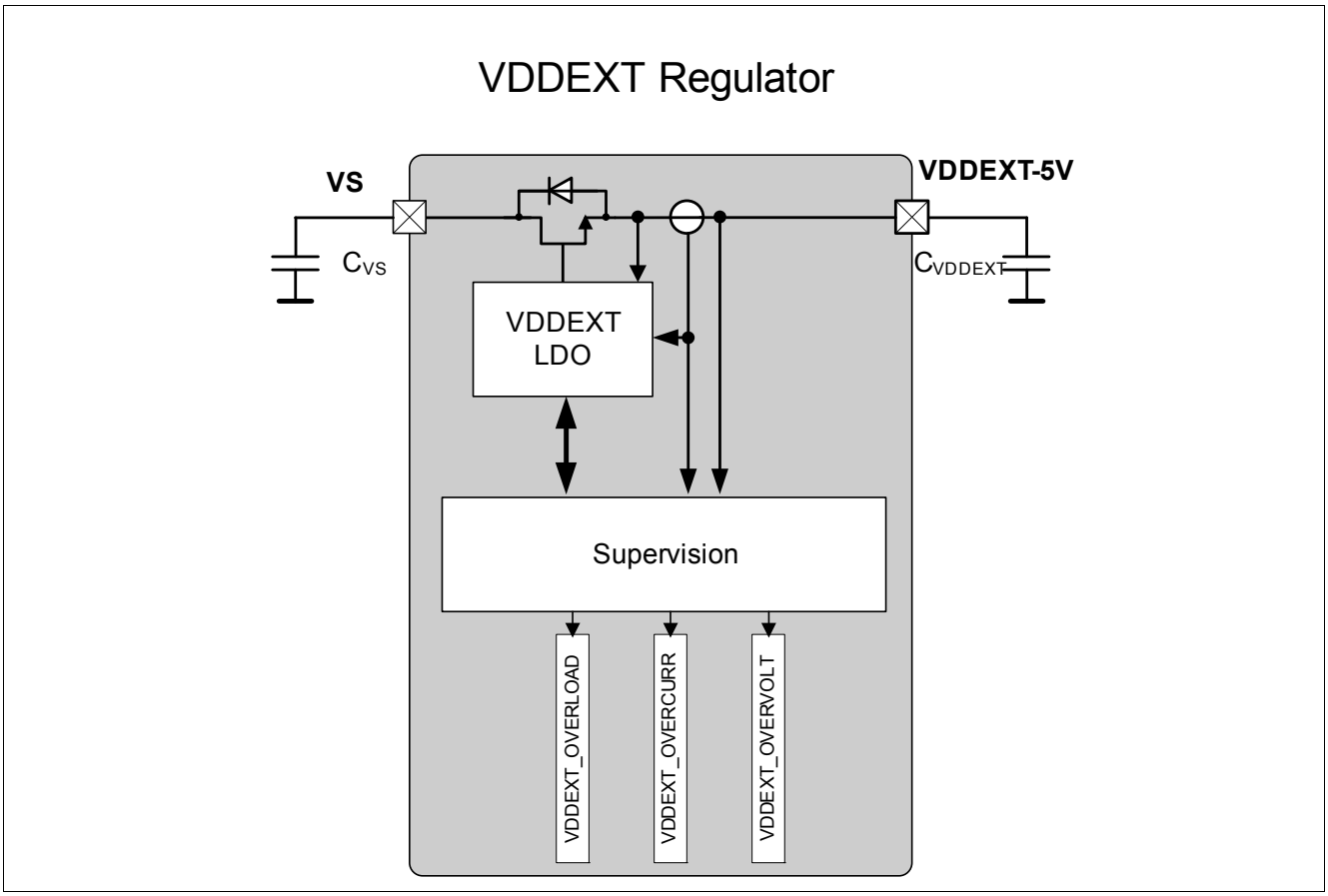

Figure 8 Module Block Diagram

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

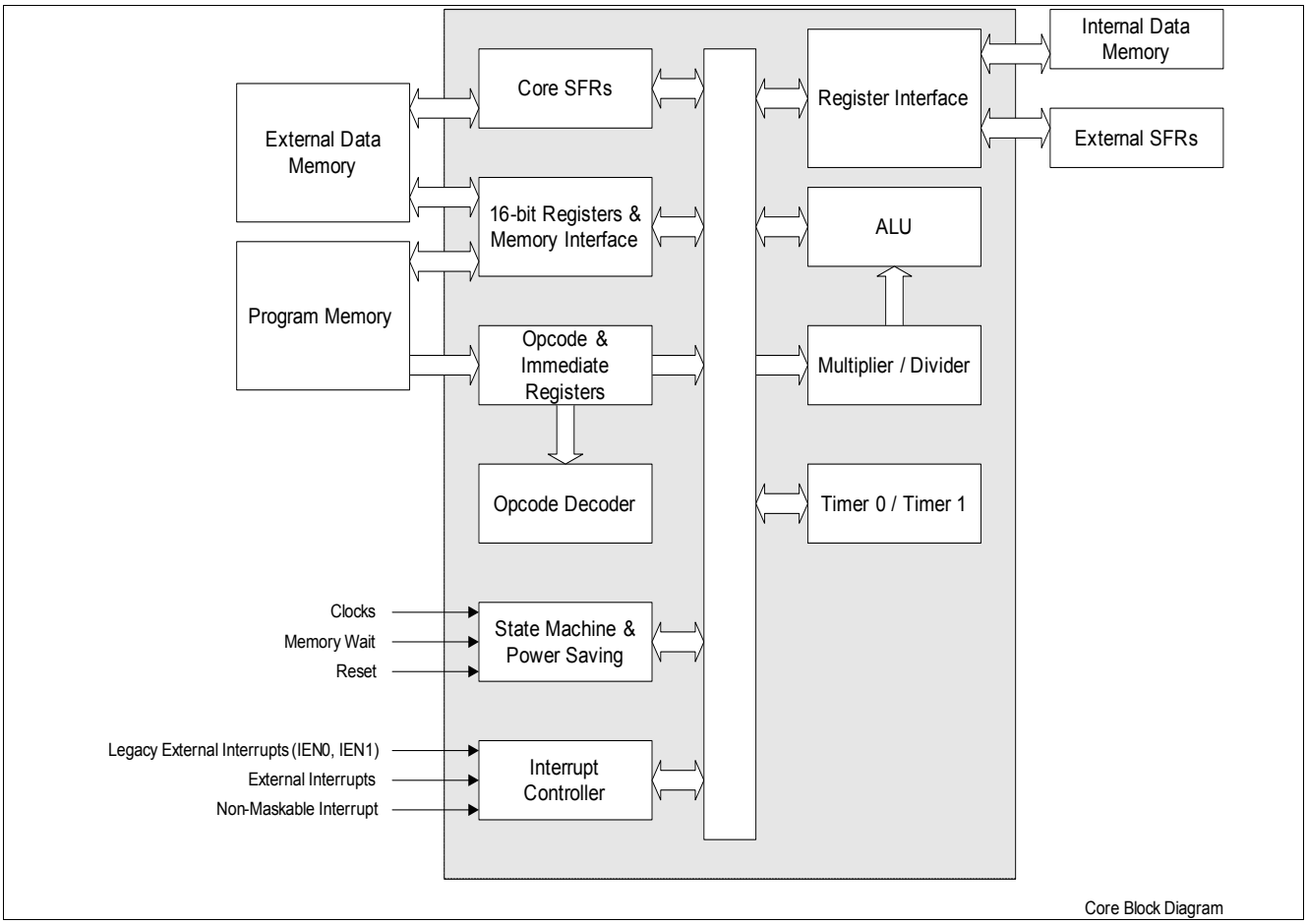

Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a sub-module in the System Control Unit (SCU). The Watchdog Timer provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT helps to abort an accidental malfunction of the TLE9832 in a user-specified time period. When enabled, the WDT will cause the TLE9832 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing an TLE9832 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

The WDT is disabled by default.

In debug mode, the WDT is suspended by default and stops counting (its debug suspend Bit is set by default i.e. MODSUSP.WDTSUSP = 1). Therefore during debugging, there is no need to refresh the WDT.

Features

- 16-Bit Watchdog Timer
- Programmable reload value for upper 8 Bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$

The Watchdog Timer is a 16-Bit timer, which is incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-Bit timer is realized as two concatenated 8-Bit timers. The upper 8 Bits of the Watchdog Timer can be preset to a user-programmable value via a watchdog service access in order to vary the watchdog expiring time. The lower 8 Bits are reset on each service access. **Figure 13** shows the block diagram of the watchdog timer unit.

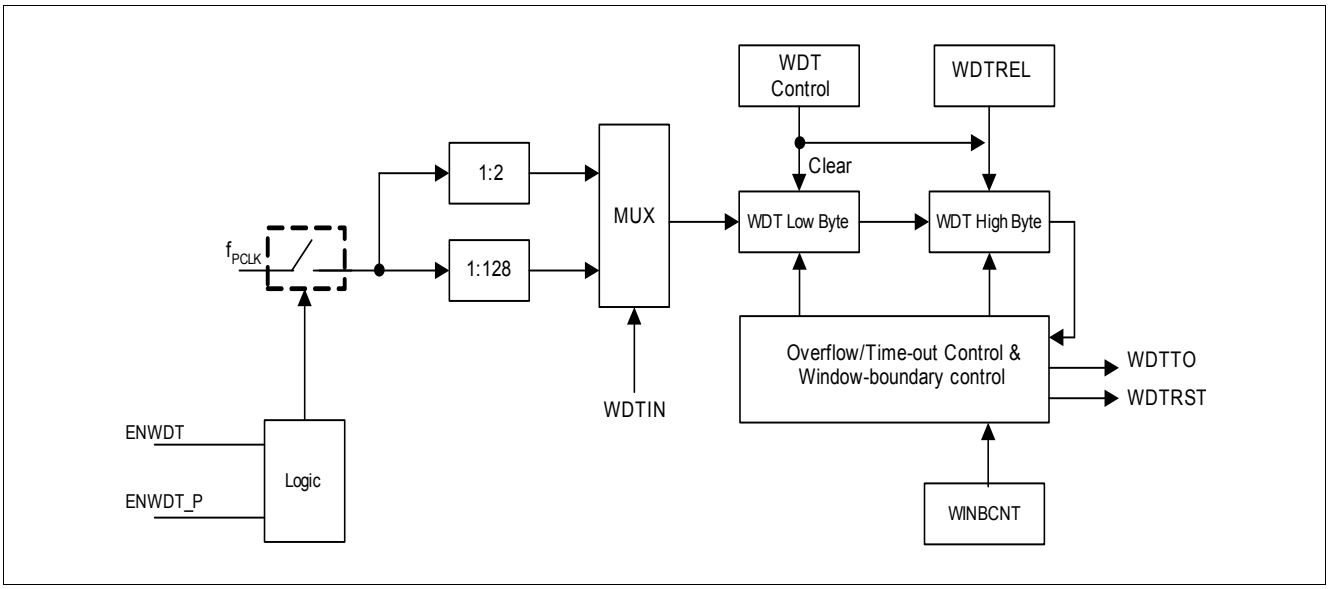

Figure 13 WDT Block Diagram

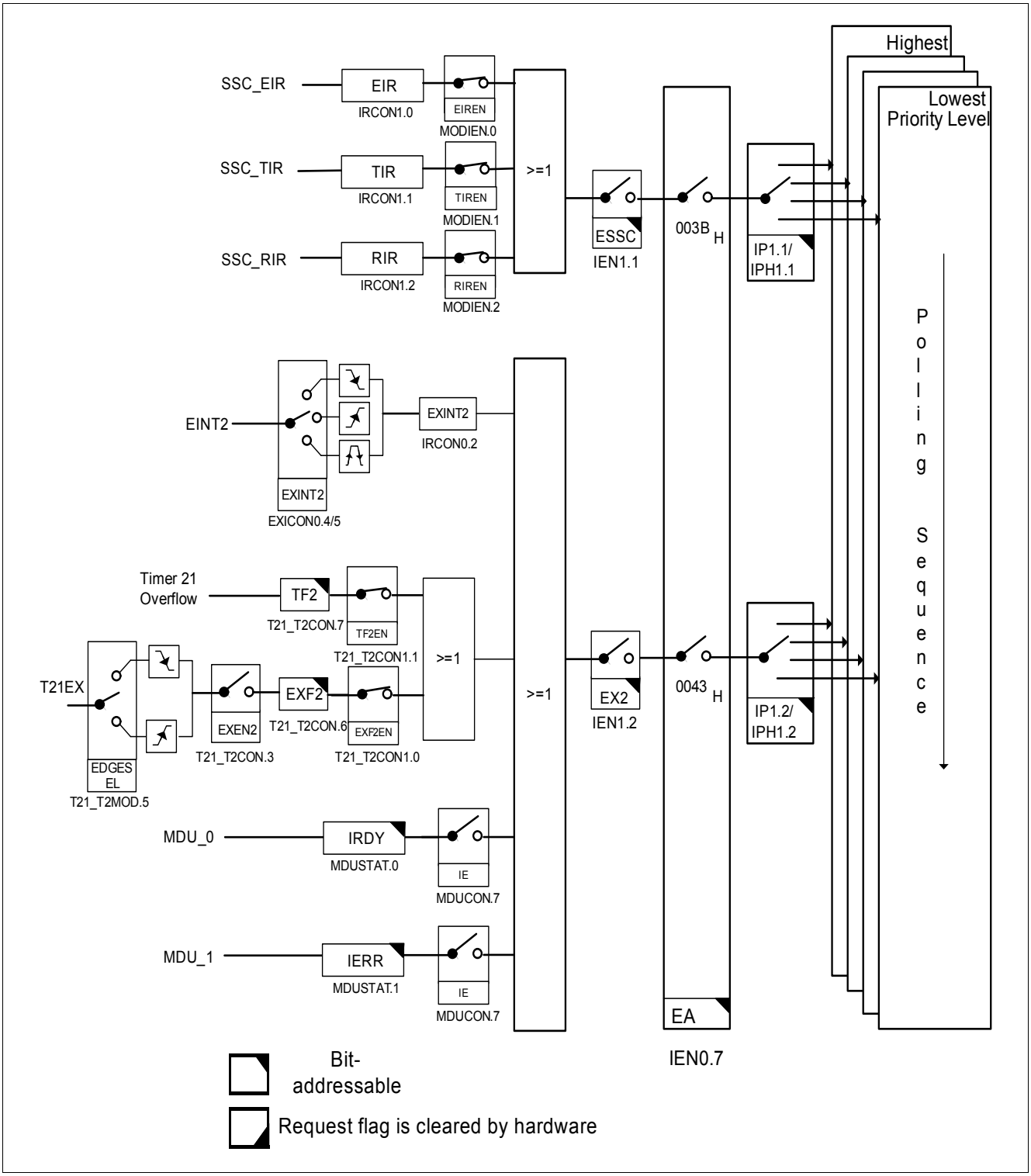

Figure 16 Interrupt Request Sources (Part 3)

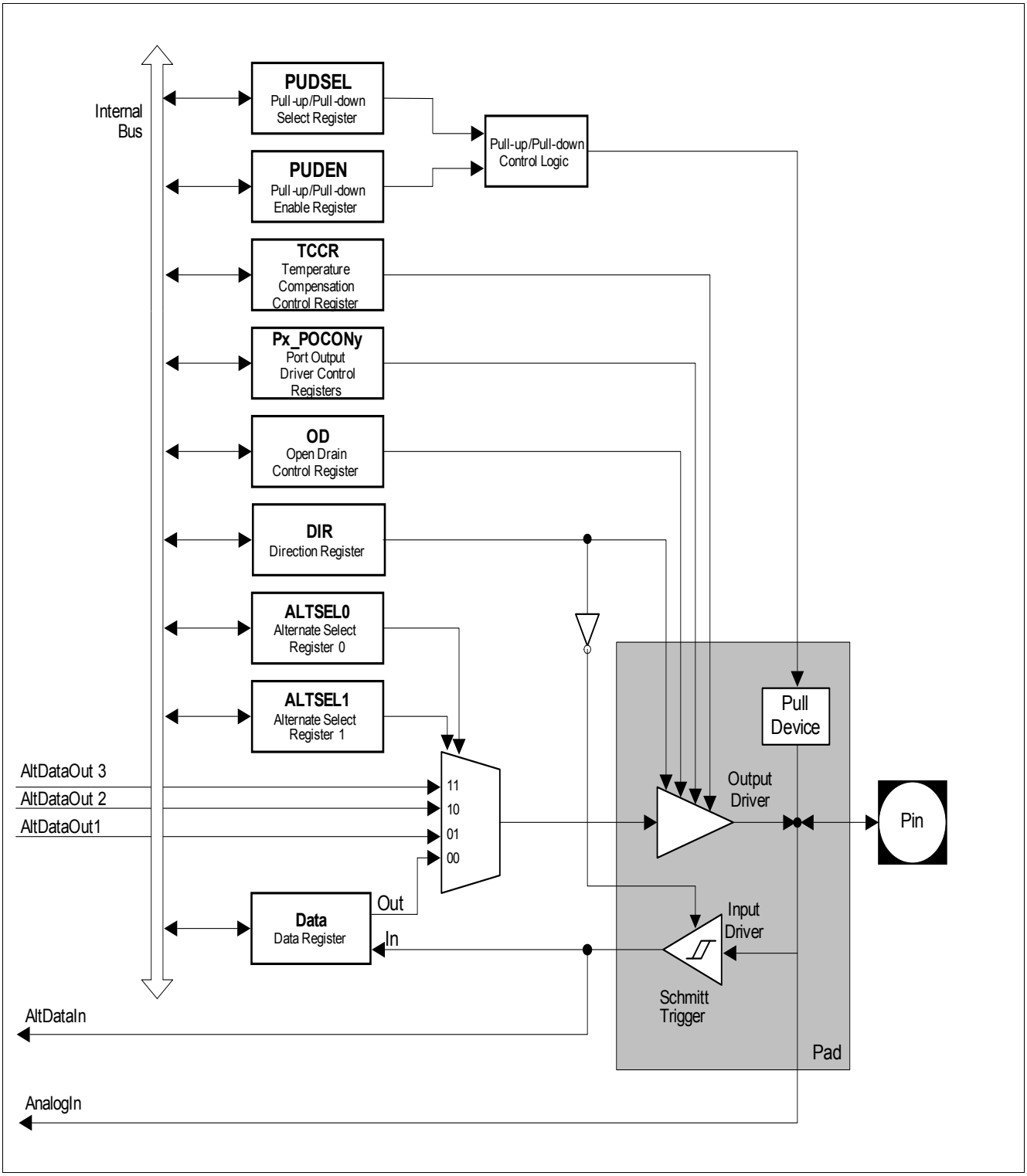

Figure 20 General Structure of a Bidirectional Port Pin

Figure 21 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via register. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. The analog input (Analog In) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC1 input channel.

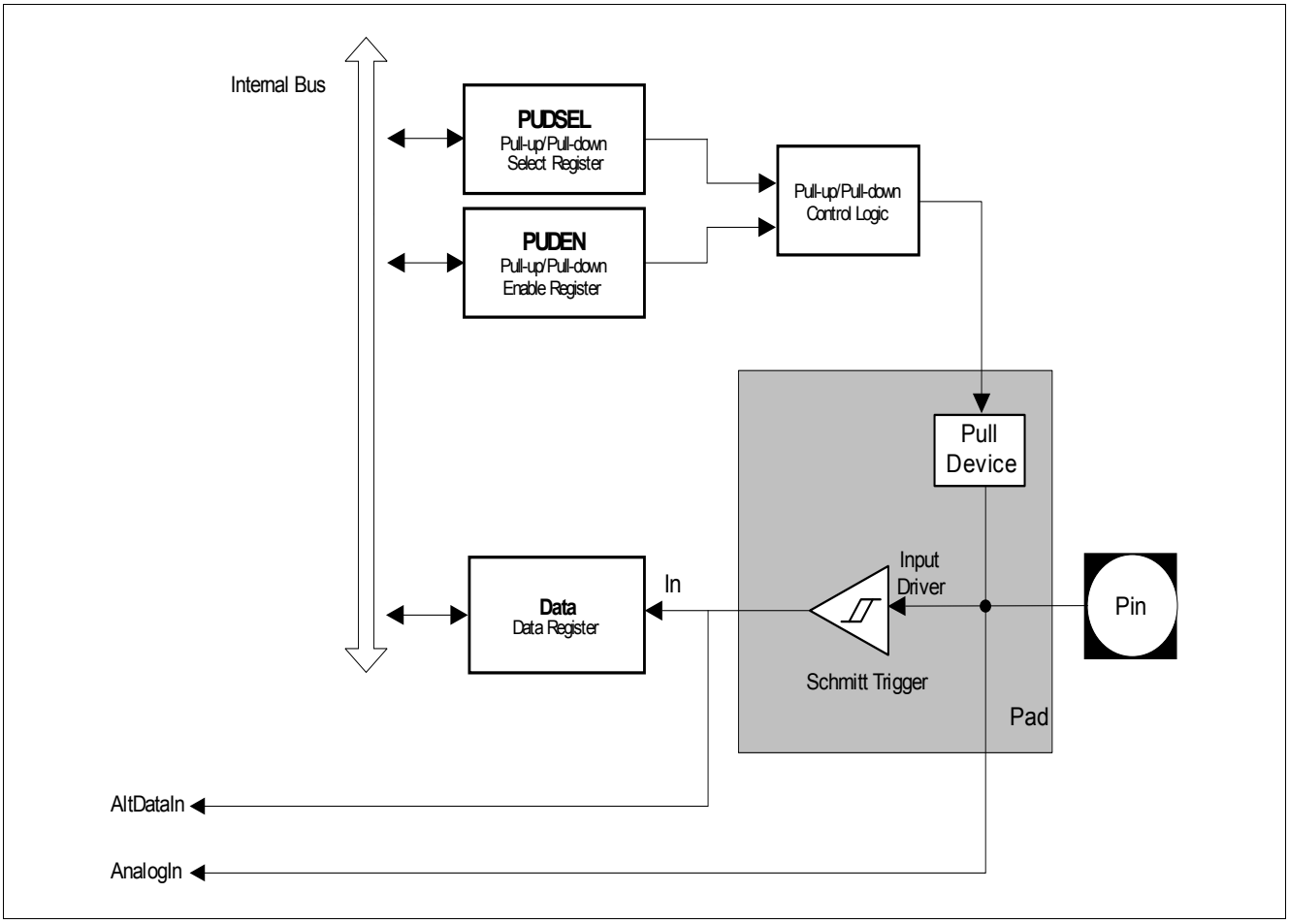

Figure 21 General Structure of an Input Port Pin

3.12 Timer 2 and Timer 21

Timer 2 and Timer 21 are 16-Bit general purpose timers that are fully compatible and have two modes of operation, a 16-Bit auto-reload mode and a 16-Bit one channel capture mode, see **Table 7**. As a timer, the timers count with an input clock of PCLK/12 (if prescaler is disabled). As a counter, they count 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is PCLK/24 (if prescaler is disabled).

Table 7 Timer 2 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-Bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-Bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generate with reload or capture event

3.20 Analog Digital Converter (ADC1)

The TLE9832 includes a high-performance 10-Bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN1, AN3 - AN5, AN7.

Features

- Successive approximation
- 8-Bit or 10-Bit resolution
- 8 analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

4 Application Information

4.1 Electric Drive Application

Figure 31 shows the TLE9832 in an electric drive application setup controlling a DC-brush motor. The two Low Side Switches are controlling a relay each. An external FET allows to control the window lift motor with a PWM signal as generated with the CCU6 module of the microcontroller.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

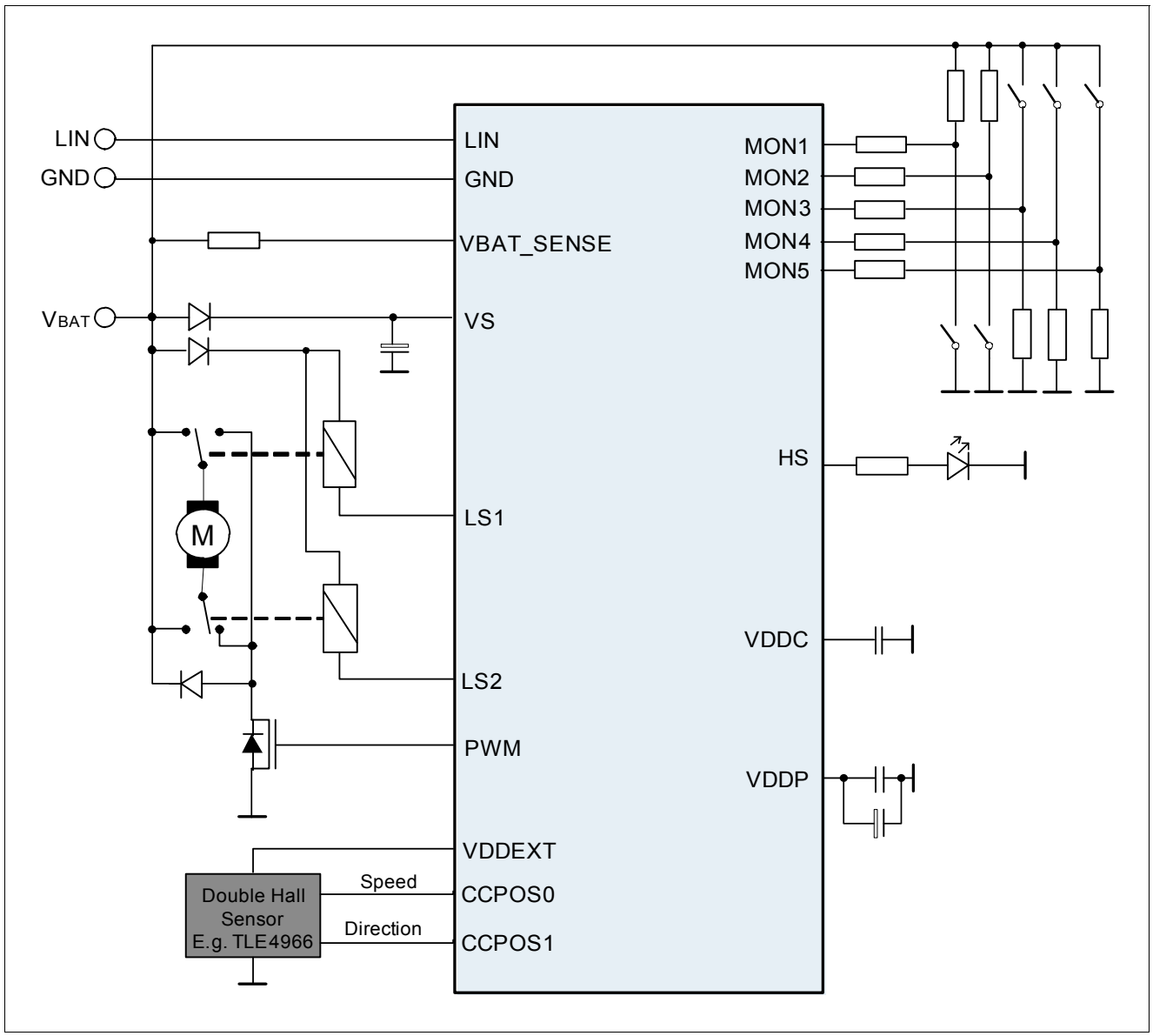

Figure 31 Simplified Application Diagram

Table 27 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Nominal Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	VDDP < 4.5V	VDDP ≥ 4.5V	VDDP < 4.5V	
Strong Driver	7.5 mA	7.5 mA	2.5 mA	2.5 mA	P_5.5.16
Medium Driver	4 mA	2.5 mA	1.0 mA	1.0 mA	P_5.5.17
Weak Driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA	P_5.5.18

1) Not subject to production test, specified by design.

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < GND$) the voltage on V_{DDP} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;(LIN Spec 2.1; Param. 31)	P_5.6.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kBit/s)	t_{duty1}	0.396	–	–		[5] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 27)	P_5.6.19
Duty cycle D2 Normal Slope Mode (for worst case at 20 kBit/s)	t_{duty2}	–	–	0.581		[6] duty cycle 2 TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)	P_5.6.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	(LIN Spec 2.1; Param. 31)	P_5.6.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN Spec 2.1; Param. 32)	P_5.6.23

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis	$I_{OLONhys}$	1	–	4	mA	[1] OL_EN = 1; HS_ON = 1	P_5.11.26
Off-state open load detection							
Open load voltage threshold	V_{OLth1}	0.5* V_S	0.67 *V_S	0.85* V_S	V	I_{OL_test}; open load activated; OLTH_SEL = 1	P_5.11.27
Hysteresis	V_{OLhys}	0.1* V_S	–	0.3* V_S	V	IOL_SEL = 1	P_5.11.28
Open load output current	I_{OL_test}	-150	–	-25	µA	IOL_SEL = 0	P_5.11.29
Open load output current	I_{OL_test}	-1.5	–	-0.5	mA	IOL_SEL = 1	P_5.11.30
Cyclic sense mode							
ON-State Resistance	$R_{ON,static}$	–	–	40	Ω	Definition: differential resistance or resistance at 40 mA	P_5.11.31
Output Slew Rate (rising)	SR_{rise} [1]	1	–	–	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω [1]	P_5.11.32
Output Slew Rate (falling)	SR_{fall} [1]	–	–	-1	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω	P_5.11.33
Delay Time CYCLIC_ON-HS	t_{IN-CYC}	–	–	2	µs	ON =1 to 10% of V_S RL=300Ω	P_5.11.34
Turn-ON time	t_{ON}	–	–	15	µs	V_S =13.5V ON=1 to 90% R_L =300Ω	P_5.11.35
Turn-OFF time	t_{OFF}	–	–	15	µs	V_S =13.5V ON=0 to 10% of V_S R_L =300Ω; T_j=25°C	P_5.11.36

1) Not subject to production test, specified by design.

Table 41 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn OFF Delay time, PWM mode	$t_{dOff,f\text{-}LS}$	–	–	2	µs	LS_ON=0 to 0.1*Vs V_S=13.5V, R_L =270Ω	P_5.12.12
Turn OFF Rise time, PWM mode	$t_{OFFR,PWM}$	–	1	1.25	µs	V_{LS} 0.1*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.13
Turn OFF Rise time, slow mode	$t_{OFFR,Slow}$	–	100	150	µs	1) V_{LS} 0.9*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.14
Minimum Duty Cycle Pulse Width variation	ton_{MIN}	1.5	2	3.5	µs	ton(dig) = 2µs2)	P_5.12.15
Typical (systematic) Pulse Width increase LS_ON to VLS	$d\ ton_{TYP}$	–	1.25	–	µs	ton(dig) = 2µs2)	P_5.12.16
Zener Clamp Voltage	V_{AZ}	–	50	–	V	values are valid at T_j = 25°C	P_5.12.17
Clamping Energy (repetitive)	E_{clamp}	–	–	2	mJ	2) 1.000.000 cycles	P_5.12.18
Clamping Energy	E_{clamp}	–	–	14	mJ	2) Tstart = 25°C	P_5.12.19
Clamping Energy (single), hot	E_{clamp}	–	–	7	mJ	2) 10 cycles, Tstart = 85°C	P_5.12.20

1) Static ON mode (no PWM)

2) Not subject to production test, specified by design

7 Revision History

Revision	Date	Changes
1.1	2012-03-08	Editorial Changes
1.1	2012-03-08	Added full package name (VQFN-48-22)
1.1	2012-03-08	**Table 4**: VDD1V5P: Power Mode configurations: added comment: "Power Down Supply"
1.1	2012-03-08	**Table 5**: Description of PMU Submodules: PMU-CYCMU description added and PMU-CMU changed from “cyclic” to “clock” management
1.1	2012-03-08	**Table 30**: Changed Value Max. from parameter “Common input voltage in differential mode” from V_{DD} to V_{DDP}
1.1	2012-03-08	**Table 23**: Changed Value Min. from parameter “Input voltage (amplitude) on XTAL1” from $0.3xV_{DDI}$ to $0.3xV_{DDP}$
1.1	2012-03-08	**Table 41**: for “Turn ON..., Turn OFF...” Parameters changed Test condition from R_L =1kΩ to R_L =270Ω
1.1	2012-03-08	**Table 14**: - Removed “max” from the symbol suffixes - Corrected Symbol of Parameter “Input voltage at LIN” from V_{MONx} to V_{LIN}
1.1	2012-03-08	**Table 41**: Parameter “Overcurrent Limitation”: - Renamed Parameter from “Typical on-state current” to “Overcurrent Limitation”. - Added min. (175mA) and max (325mA) values - Removed Parameter “Overcurrent threshold accuracy”. This information is added in the “Note/Test” Condition of the Parameter ”Overcurrent Limitation”
1.1	2012-03-08	**Table 19**: - Renamed Parameter “Output Current” to “Specified Output Current” - Renamed Parameter “Output Capacitance” to “Required Output Capacitance”
1.1	2012-03-08	**Table 20**: - Renamed Parameter “Output Current” to “Specified Output Current” - Renamed Parameter “Output Capacitance” to “Required Output Capacitance” - Parameter “Dynamic Line Regulation”: Correct typo in “Note/Test Condition” from V_{DDC} to V_{DDP} - Parameter “Output Voltage including line regulation @ Stop Mode”: Value Max. changed from 1.01 to 1.15
1.1	2012-03-08	**Figure 31**: Application Diagram updated
1.1	2012-03-08	**Figure 29**: Modul Block Diagram updated (replaced 500mA by 250mA)
1.1	2012-03-08	**Table 27**: Change “Maximum Output Current” to “Nominal Output Current” in third row
1.1	2012-03-08	**Table 14**: Added “Output voltage VDDP” for t < 100ms, in Stop Mode only
1.1	2012-03-08	**Chapter 4.1**: Added disclaimer note
1.1	2012-03-08	**Table 11**: Changed value C_{VDDEXT} of blocking capacitor at VDDEXT pin to100nF (from 10nF)
1.1	2012-03-08	**Table 11** and **Table 12**: Changed headline from “External Component Requirements” to “External Component Recommendation”

Revision	Date	Changes
1.1	2012-03-08	**Table 14**: - Renamed Parameter “Output voltage VDDP” to “Voltage VDDP” (2x) - Renamed Parameter “Output voltage VDDC” to “Voltage VDDC”
1.1	2012-03-08	**Table 28**: Added value LIN input capacity C_{LIN_IN}