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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | - |
| Core Processor | - |
| Program Memory Type | - |
| Controller Series | - |
| RAM Size | - |
| Interface | - |
| Number of I/O | - |
| Voltage - Supply | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qvxuma3 |

## 1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832 device configuration.

**Table 1 Device Configuration**

| Device Name | Max Clock Frequency | High Side Switches | High Voltage Monitor Inputs | Flash Size | Bidirectional Parallel Port I/O´s | Operational Amplifier |
|---|---|---|---|---|---|---|
| TLE9832QV | 40 MHz | 1 | 5 | 36 kByte | 11 | no |
| TLE9832QX | 40 MHz | 1 | 5 | 36 kByte | 11 | no |

## 1.2 Abbreviations

The following acronyms and terms are used within this document. List see in Table 2.

**Table 2 Acronyms**

| Acronyms | Name |
|---|---|
| ALU | Arithmetic Logic Unit |
| CCU6 | Capture Compare Unit 6 |
| CGU | Clock Generation Unit |
| CMU | Cyclic Management Unit |
| DAP | Device Access Port |
| DPP | Data Post Processing |
| ECC | Error Correction Code |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| GPIO | General Purpose Input Output |
| FSR | Full Scale Range |
| ICU | Interrupt Control Unit |
| IRAM | Internal Random Access Memory - Internal Data Memory |
| LDO | Low DropOut voltage regulator |
| LIN | Local Interconnect Network |
| LSB | Least Significant Bit |
| MCU | Micro Controller Unit |
| MDU | Multiplication Division Unit |
| MMC | Monitor Mode Control |
| MSB | Most Significant Bit |
| NMI | Non Maskable Interrupt |
| OCDS | On Chip Debug Support |
| OTP | One Time Programmable |
| OSC | Oscillator |
| PC | Program Counter |
| PCU | Power Control Unit |
| PD | Pull Down |
| PGU | Power supply Generation Unit |
| PLL | Phase Locked Loop |
| PMU | Power Management Unit |
| PSW | Program Status Word |
| PU | Pull Up |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RCU | Reset Control Unit |
| RMU | Reset Management Unit |

**Table 2 Acronyms**

| Acronyms | Name |
|---|---|
| ROM | Read Only Memory |
| SCK | SSC Clock |
| SFR | Special Function Register |
| SOW | Short Open Window (for WDT1) |
| SPI | Serial Peripheral Interface |
| SSC | Synchronous Serial Channel |
| SSU | System Status Unit |
| TMS | Test Mode Select |
| UART | Universal Asynchronous Receiver Transmitter |
| UDIG | Universal Digital Controller for ADC1 |
| VBG | Voltage reference Band Gap |
| WDT | Watchdog timer |
| WMU | Wake-up Management Unit |
| XRAM | On-Chip eXternal Data Memory |
| XSFR | On-Chip eXternal Special Function Register |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| VAREF | 34 | I/O | O | 5V ADC1 reference voltage |
| XTAL1 | 27 | I | I | External oscillator input |
| XTAL2 | 28 | O | Hi-Z | External oscillator output |
| TMS | 18 | I | I/PD | TMS test mode select input<br>DAP1 Debug Access Port 1 |
| RESET | 21 | I/O | I/O/PU | Reset input, not available during Sleep Mode |
| VBAT_SENSE | 48 | I | I | Battery supply voltage sense input |
| N.C. | 10, 29, 40, 41, 46 | – | – | Not connected - can be connected to GND |
| N.C. | 4 | – | – | Not connected - leave pin open |

## Block Diagram

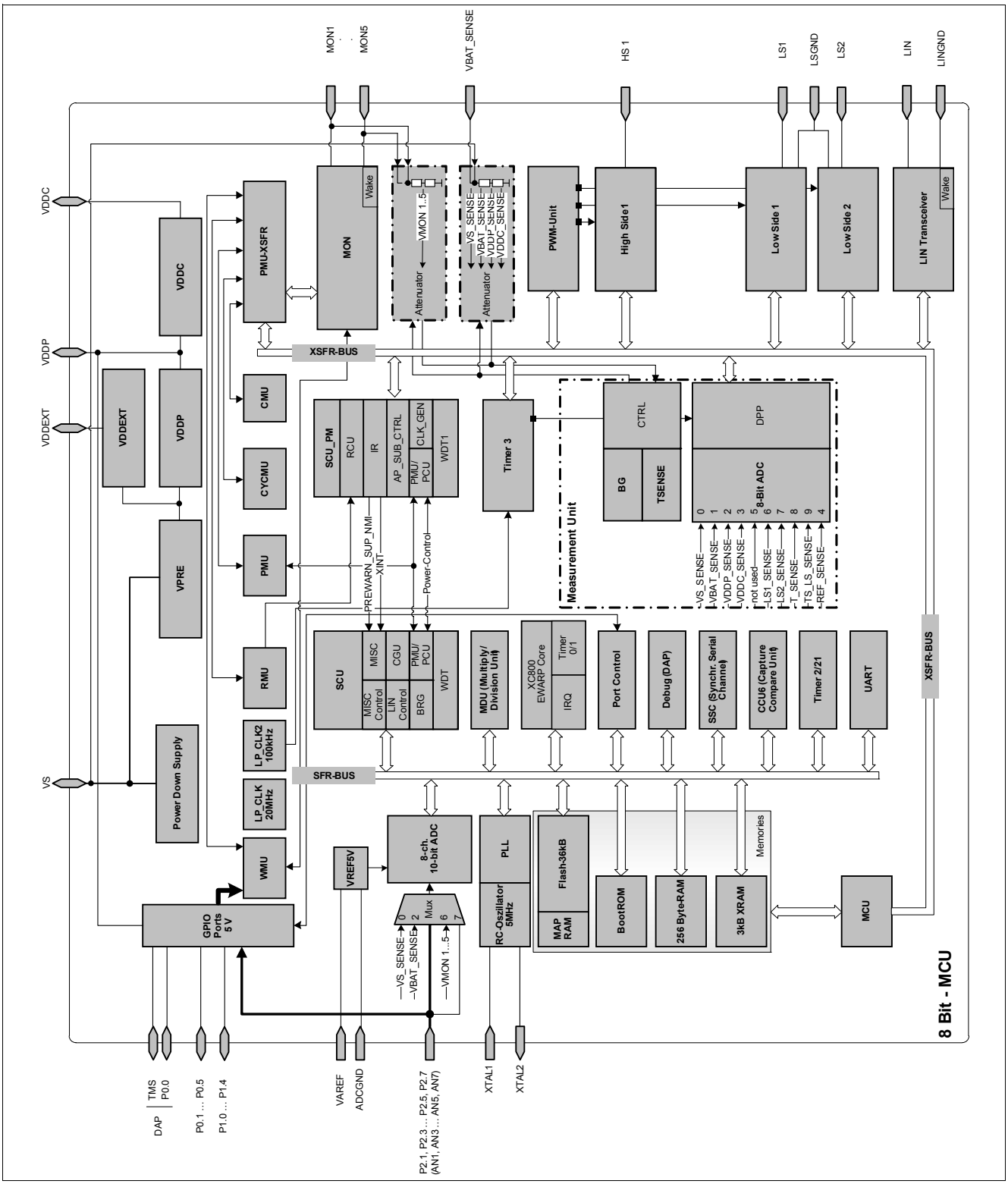


**Figure 2 Block Diagram**

The TLE9832 has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

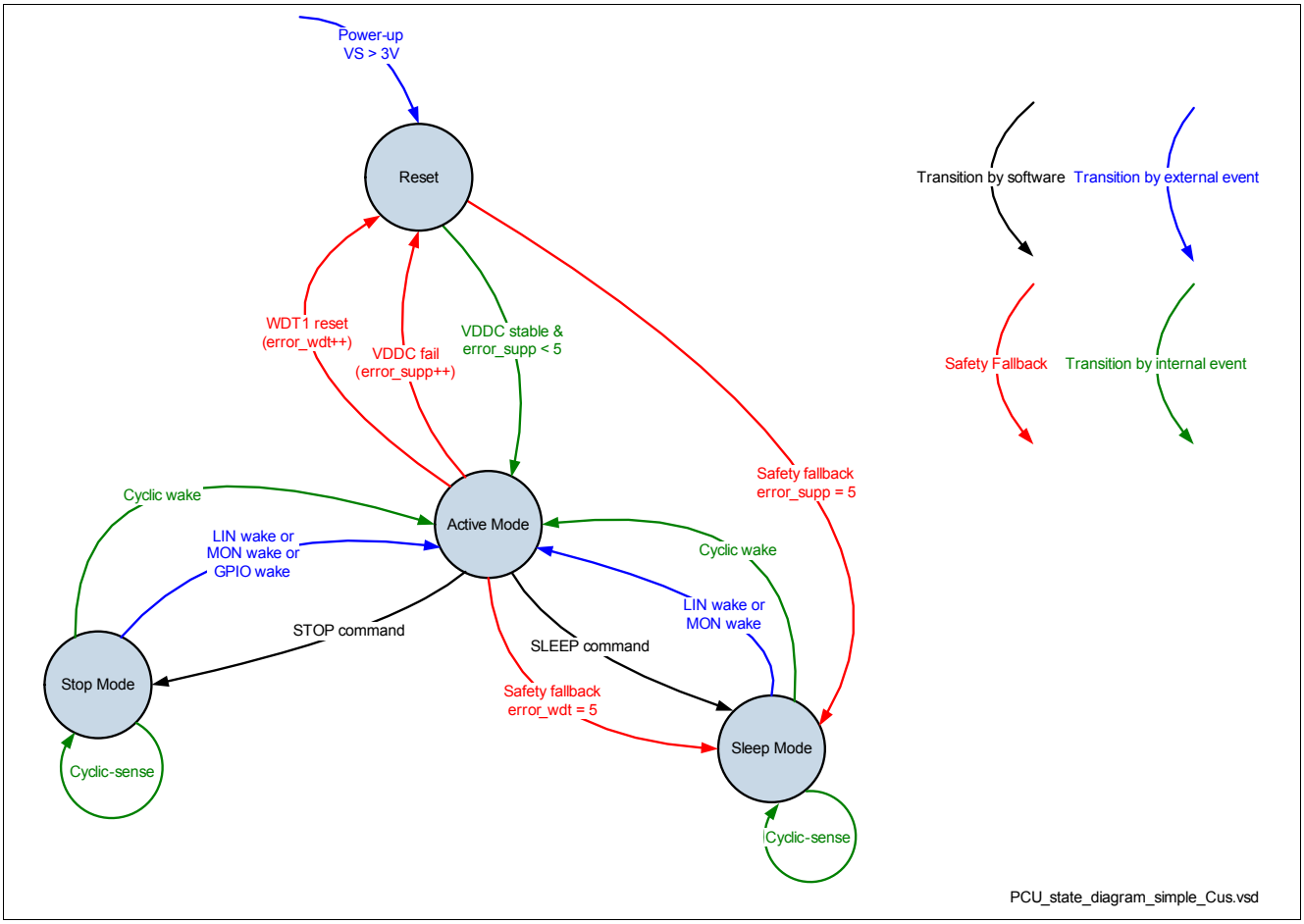


**Figure 3 Power Control State Diagram**

### Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

### Active Mode

In Active Mode all modules are activated and the TLE9832 is fully operational.

### Stop Mode

The Stop Mode is one out of two low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

### Sleep Mode

The Sleep Mode is the second low-power mode. The transition to the low-power modes is done by setting the respective Bits in the MCU mode control register. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins. A wake-up from Sleep Mode behaves similar to a power-on reset.

**Table 5 Description of PMU Submodules**

| Mod. Name | Modules | Functions |
|---|---|---|
| Power Down Supply | Independent Supply Voltage Generation for PMU | This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC). |
| LP_CLK (= 20 MHz) | - Clock Source for all PMU submodules<br>- Backup Clock Source for System<br>- Clock Source for WDT1 | This ultra low power oscillator generates the clock for the PMU.<br>This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1 |
| LP_CLK2 (= 100 kHz) | Clock Source for PMU | This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes. |
| Peripherals | Peripheral blocks of PMU | This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation |
| Power Supply Generation Unit (PGU) | Voltage regulators for VDDP and VDDC | This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features |
| VDDEXT (Hall Sensor Supply) | Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors) | This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor) |
| PMU-XSFR | All PMU relevant Extended Special Function Registers | This module contains all PMU relevant registers, which are needed to control and monitor the PMU. |
| PMU-PCU | Power Control Unit of the PMU | This block is responsible for controlling all power related actions within the PGU Module. |
| PMU-WMU | Wake-up Management Unit of the PMU | This block is responsible for controlling all wake-up related actions within the PMU Module. |
| PMU-CYCMU | Cyclic Management Unit of the PMU | This block is responsible for controlling all actions within cyclic mode. |
| PMU-CMU | Clock Management Unit of the PMU | This block is responsible for controlling all clocking actions within the PMU. |
| PMU-RMU | Reset Management Unit of the PMU | This block is responsible for generating all system required resets. |

### 3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

**Features**

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/µs max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 µA)
- Cyclic sense option together with GPIOs

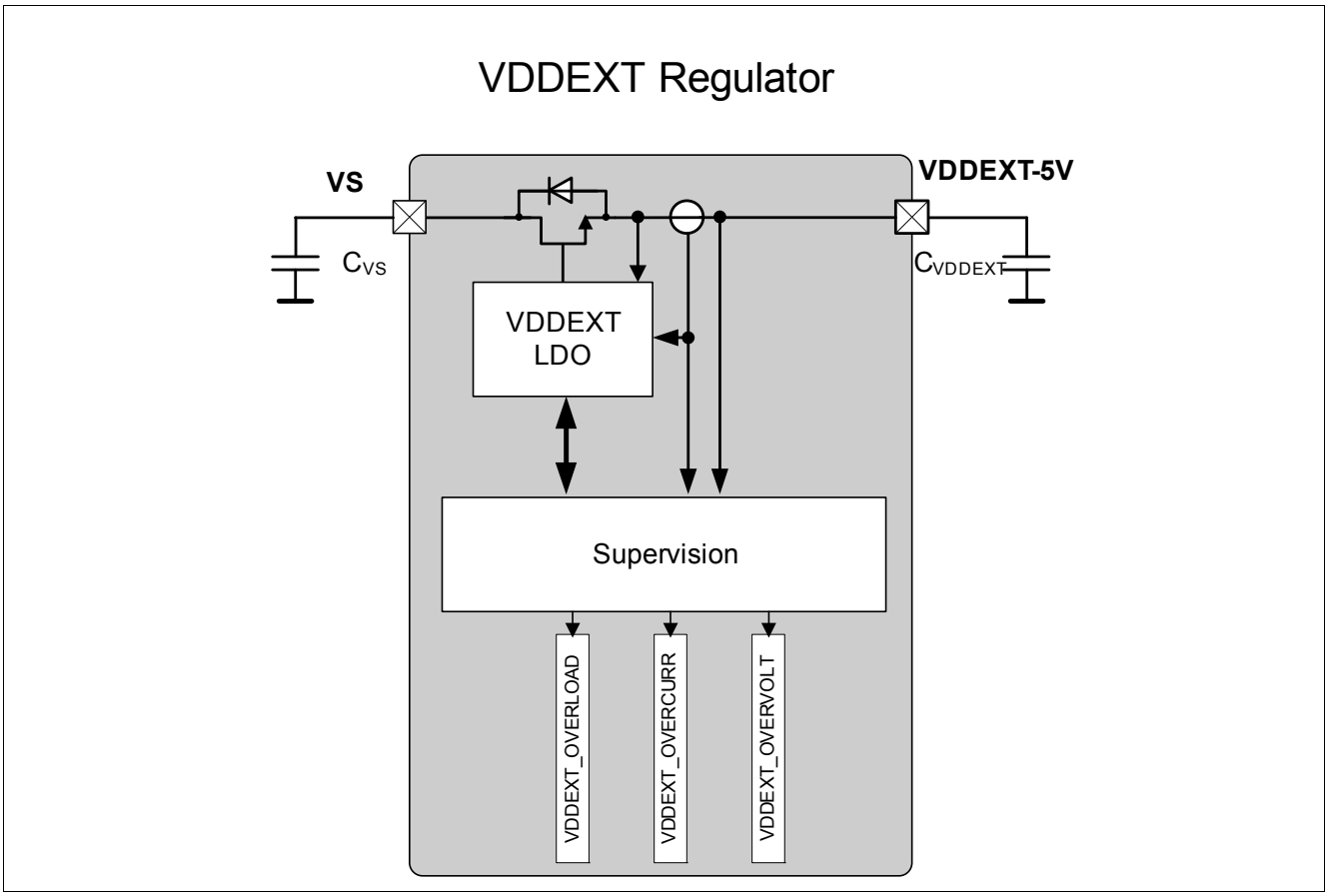


**Figure 8 Module Block Diagram**

## 3.8 Interrupt System

The TLE9832 supports 14 interrupt vectors with four priority levels. Eleven of these interrupt vectors are assigned to the on-chip peripherals: Timer 0, Timer 1, UART, SSC and A/D Converter are each assigned to one dedicated interrupt vector; while Timer2, Timer21, MDU, LIN and the Capture/Compare Unit share six interrupt vectors.

Two interrupt vectors are assigned to the external interrupts. External interrupts 0 to 1 are each assigned to one dedicated interrupt vector, external interrupt 2 shares on interrupt vector with Timer21 and the MDU.

One interrupt vector is dedicated to the XINT interrupt events whose interrupt flags are also located in registers in XSFR area.

A non-maskable interrupt (NMI) with the highest priority is shared by the following:

- Watchdog Timer, warning before overflow
- MI_CLK Watchdog Timer overflow event
- PLL, loss of lock
- Flash, on operation complete, e.g. erase.
- OCDS, on user IRAM event
- Oscillator watchdog detection for too low oscillation of $f_{OSC}$
- Flash map error
- Uncorrectable ECC error on Flash, XRAM and IRAM
- VSUP supply pre warning when any supply voltage drops below or exceeds any threshold.

**Figure 14**, **Figure 15**, **Figure 16**, **Figure 17** and **Figure 18** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags. **Figure 19** gives the corresponding overview for the NMI sources.

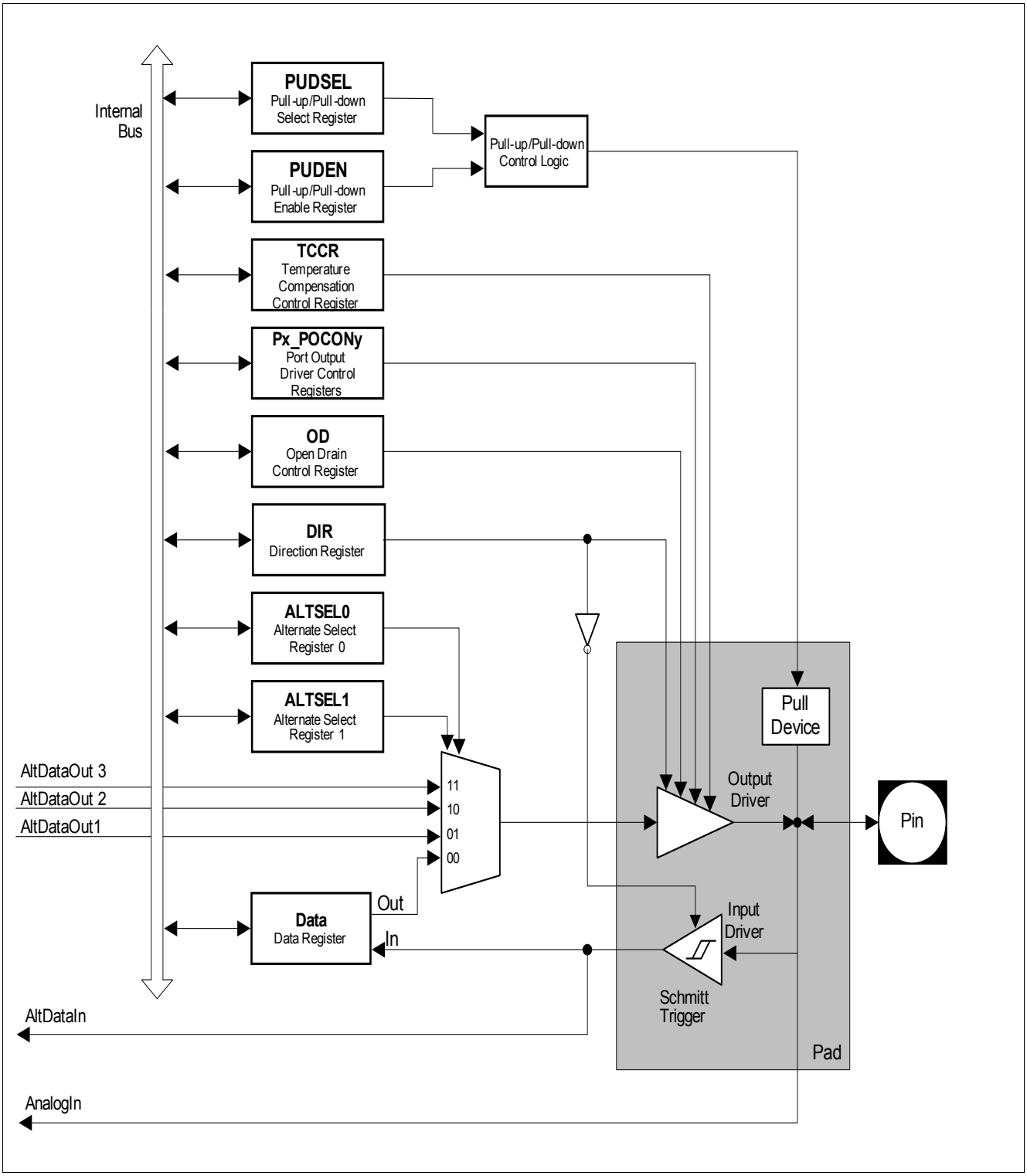


**Figure 20 General Structure of a Bidirectional Port Pin**

## 3.14 Capture/Compare Unit 6 (CCU6)

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status Bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

*Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.*

**Timer 12 Block Features**

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and Low Side Switches)
- 16-Bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

**Timer 13 Block Features**

- One independent compare channel with one output
- 16-Bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

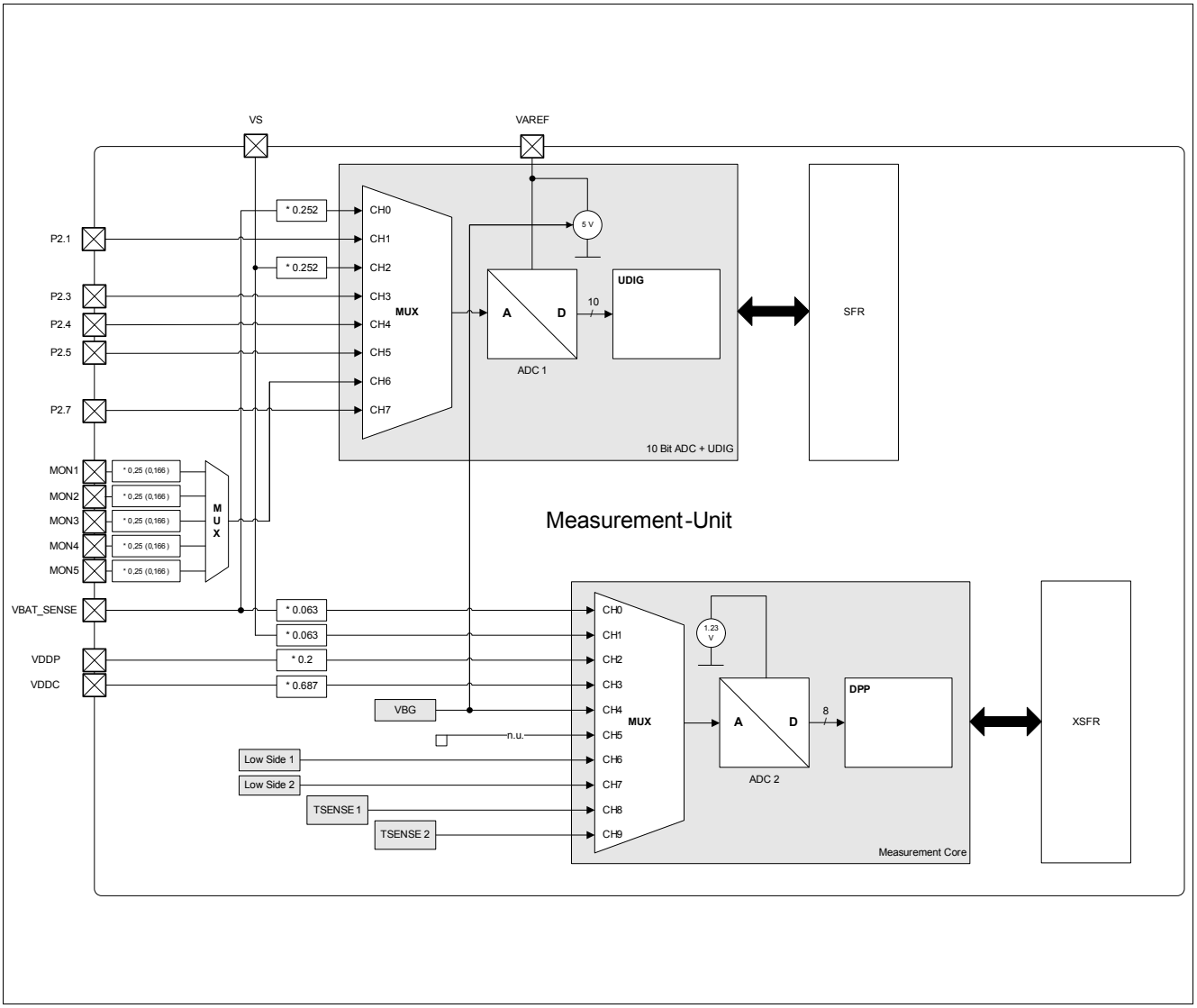


**Figure 25 TLE9832 Measurement Unit-Overview**

## 3.19 Measurement Core Module (incl. ADC2)

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of ten identical channel units attached to the outputs of the 10-channel 8-Bit ADC (ADC2). It processes ten channels, where the channel sequence and prioritization is programmable within a wide range.

### Features

- 10 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
  - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
  - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable interrupts and status for all channel thresholds

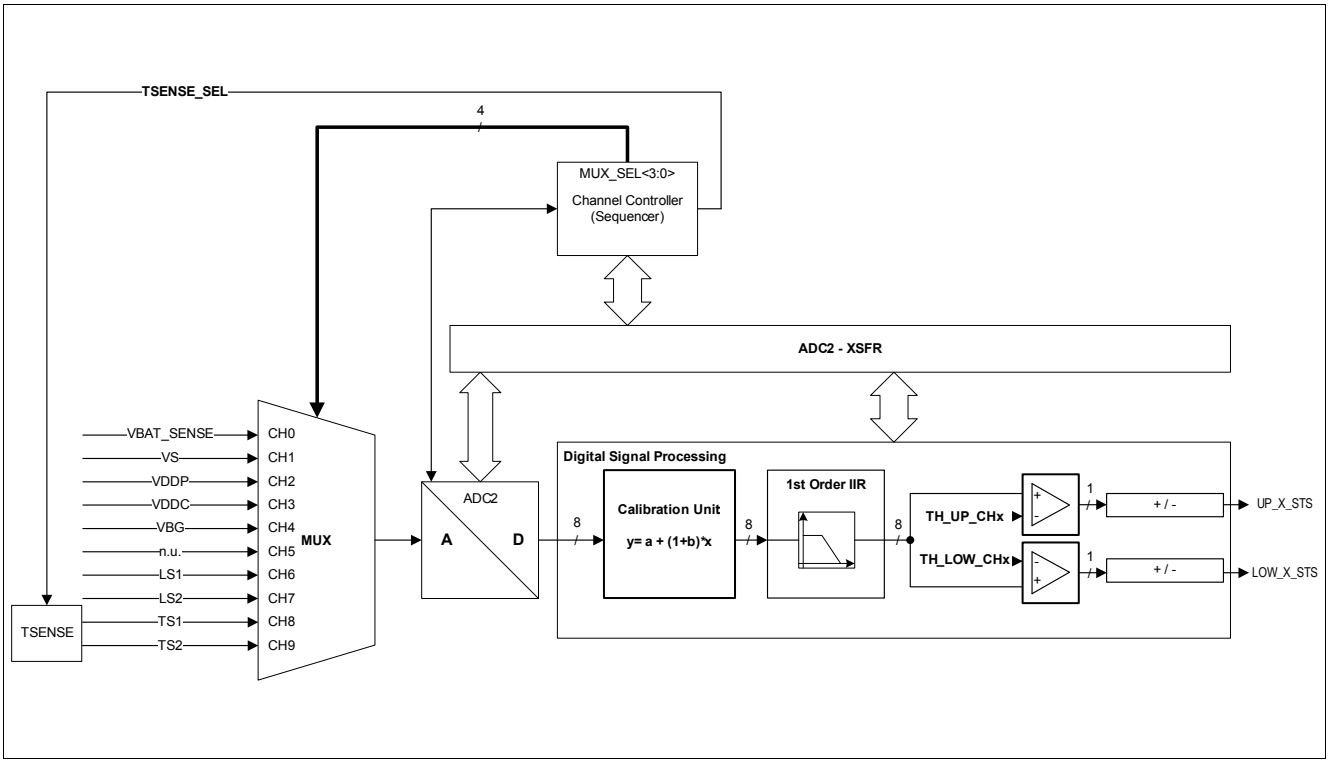


**Figure 26 Measurement Core Module Block Diagram**

### 5.1.3 Current Consumption

**Table 16 Electrical Characteristics** [1)]

$V_s$ = 5.5V to 18V, $T_J$ = -40°C to 85°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Current Consumption @VS pin** | | | | | | | |
| Current Consumption in Active Mode | $I_{Active}$ | – | 30 | 40 | mA | fsys = 40 MHz<br>no loads on pins, LIN in recessive state, LS1, LS2, HS1 off | P_5.1.25 |
| Current consumption in Stop Mode | $I_{Powerdown}$ | – | 85 | 95 | µA | microcontroller in Stop Mode, LIN recessive state, MON1-5 disabled, GPIOs open (no loads) | P_5.1.26 |
| Current consumption in Stop Mode with cyclic sense enabled | $I_{Powerdown2}$ | – | – | 110 | µA | microcontroller in Stop Mode, LIN recessive state, GPIOs open (no loads) | P_5.1.27 |
| Current consumption in Sleep Mode | $I_{Sleep}$ | – | – | 25 | µA | system in Sleep Mode, microcontroller not powered, LIN recessive state, MON1-5 disabled and GPIOs open (no loads) | P_5.1.28 |

1) Not subject to production test, specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 5.1.4 Thermal Resistance

**Table 17 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Ambient | $R_{thJA}$ | – | 23.9 | – | K/W | 1) | P_5.1.29 |

1) EIA/JESD 52_2, FR4, 76.2 x 114.3 x 1.5 mm; 35µ Cu, 5µ Sn; 300 $mm^2$

### 5.2.2 PMU Core Supply Parameters VDDC

**Table 20 Electrical Characteristics**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | $I_{VDDC}$ | 0 | – | 30 | mA | 1) only used as internal core supply | P_5.2.11 |
| Required Output Capacitance | $C_{VDDC}$ | 0.1 | – | 10 | µF | 2) ESR < 1Ω | P_5.2.12 |
| Output Voltage including line regulation @ Active Mode | $V_{DDCOUT}$ | 1.44 | 1.5 | 1.56 | V | $I_{load}$ < 40mA | P_5.2.13 |
| Output Voltage including line regulation @ Stop Mode | $V_{DDCOUT}$ | 0.89 | 0.95 | 1.15 | V | $I_{load}$ < 200µA | P_5.2.14 |
| Dynamic Load Regulation | $V_{DDCLOR}$ | -50 | – | 50 | mV | 2) 2 ... 30mA; C=330nF; dI/dt=100mA/µs | P_5.2.15 |
| Dynamic Line Regulation | $V_{DDCLIR}$ | -25 | – | 25 | mV | 2) $V_{DDP}$= 2.5 ... 5.5V; dV/dt=5V/µs | P_5.2.16 |
| Over Voltage Detection | $V_{DDCOV}$ | 1.61 | – | 1.68 | V | Overvoltage leads to SUPPLY_NMI | P_5.2.17 |
| Under Voltage Reset | $V_{DDVUV}$ | 1.10 | – | 1.19 | V | – | P_5.2.18 |
| Over Current Shutdown | $I_{VDDCOC}$ | 35 | – | 80 | mA | – | P_5.2.19 |

1) VDDC is not intended to be used as external voltage regulator

2) Not subject to production test, specified by design

### 5.2.3 VDDEXT Voltage Regulator 5.0V

**Table 21 Electrical Characteristics**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output Current | $I_{VDDEXT}$ | 0 | – | 20 | mA | 1) | P_5.2.20 |
| Output Capacitance | $C_{VDDEXT}$ | 10 | – | 1000 | nF | 1) ESR < 1 Ω | P_5.2.21 |
| Output Voltage including line regulation | $V_{DDEXT}$ | 4.9 | 5.0 | 5.1 | V | $I_{load}$ < 20mA;Vs > 5.5V | P_5.2.22 |
| Output Drop | $V_s$-$V_{DDEXT}$ | | – | +400 | mV | 1) $I_{load}$ < 20mA; 3V < $V_s$ < 5.5V | P_5.2.23 |
| Dynamic Load Regulation | $V_{DDEXTLOR}$ | -50 | – | 50 | mV | 1) 2 ... 20mA; C=10nF; dI/dt=10mA/µs | P_5.2.24 |
| Dynamic Line Regulation | $V_{VDDEXTLIR}$ | -25 | – | 25 | mV | $V_s$= 5.5 ... 20V; dV/dt=5V/µs | P_5.2.25 |
| Power Supply Ripple Rejection1) | $P_{SSRVDDEXT}$ | 50 | – | – | dB | $V_s$= 13.5V; f=0 ... 1KHz; $V_r$=2Vpp | P_5.2.26 |
| Over Voltage Detection | $V_{VDDEXTOV}$ | 5.05 | – | 5.4 | V | $V_s$ > 5.5V | P_5.2.27 |
| Under Voltage Detection | $V_{VDDEXTUV}$ | 2.6 | – | 2.9 | V | 2)$V_s$ > 3.0V | P_5.2.28 |
| Over Current Diagnostic | $I_{VDDEXTOC}$ | 25 | – | 70 | mA | – | P_5.2.29 |

1) Not subject to production test, specified by design

2) When the condition is met, the Bit VDDEXT_CTRL.VDDEXT_SHORT will be set

**Table 22 Electrical Characteristics**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Accumulated jitter | jacc | – | – | 5 | ns | for K=1 | P_5.3.15 |
| lock-in time | $T_L$ | – | – | 200 | µs | – | P_5.3.16 |

1) $V_{DDC}$ = 1.5 V, $T_j$ = 25°C

## 5.3.2 External Clock Parameters XTAL1, XTAL2

**Table 23 Functional Range**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input voltage range limits for signal on XTAL1 | $V_{IX1\_SR}$ | -1.7 + $V_{DDC}$ | – | 1.7 | V | 1) | P_5.3.17 |
| Input voltage (amplitude) on XTAL1 | $V_{AX1\_SR}$ | 0.3 x $V_{DDP}$ | – | – | V | 2) Peak-to-peak voltage | P_5.3.18 |
| XTAL1 input current | $I_{IL}$ | – | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DDC}$ | P_5.3.19 |
| Oscillator frequency | $f_{OSC}$ | 4 | – | 24 | MHz | Clock signal | P_5.3.20 |
| Oscillator frequency | $f_{OSC}$ | 4 | – | 16 | MHz | Crystal or Resonator | P_5.3.21 |
| High time | $t_1$ | 6 | – | – | ns | – | P_5.3.22 |
| Low time | $t_2$ | 6 | – | – | ns | – | P_5.3.23 |
| Rise time | $t_3$ | – | 8 | 8 | ns | – | P_5.3.24 |
| Fall time | $t_4$ | – | 8 | 8 | ns | – | P_5.3.25 |

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.

**Table 27 Current Limits for Port Output Drivers[1)]**

| Port Output Driver Mode | Maximum Output Current ($I_{OLmax}$ , - $I_{OHmax}$) | | Nominal Output Current ($I_{OLnom}$ , - $I_{OHnom}$) | | Number |
|---|---|---|---|---|---|
| | VDDP ≥ 4.5V | VDDP < 4.5V | VDDP ≥ 4.5V | VDDP < 4.5V | |
| Strong Driver | 7.5 mA | 7.5 mA | 2.5 mA | 2.5 mA | P_5.5.16 |
| Medium Driver | 4 mA | 2.5 mA | 1.0 mA | 1.0 mA | P_5.5.17 |
| Weak Driver | 0.5 mA | 0.5 mA | 0.1 mA | 0.1 mA | P_5.5.18 |

1) Not subject to production test, specified by design.

*Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.*
*During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < GND$) the voltage on $V_{DDP}$ pins with respect to ground ($GND$) must not exceed the values defined by the absolute maximum ratings.*

## 5.8 Measurement Unit

### 5.8.1 Analog Digital Converter 8-Bit

**Table 30 DC Specifications ADC 8 Bit**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Resolution | – | – | 8 | – | Bit | – | P_5.8.1 |
| Offset error | – | -10 | 4 | +10 | mV | – | P_5.8.2 |
| Gain single-ended input mode | GSE | – | 1 | – | | – | P_5.8.3 |
| Input voltage single-ended mode | $V_{ainp}$,$V_{ainn}$ | 0 | – | $V_{DD1V5\_A}$ | V | – | P_5.8.4 |
| Gain differential input mode | GDF | | 1.24 | – | – | – | P_5.8.5 |
| Common input voltage in differential mode | $V_{icm}$ | 0.5 | 0.6 | $V_{DDP}$/2 +0.1 | – | $V_{icm}$=($V_{ainp}$ + $V_{ainn}$)/2 | P_5.8.6 |
| Gain error | – | -5 | 1.5 | +5 | %FSR | – | P_5.8.7 |
| Differential nonlinearity (DNL) | – | -1.5 | 0.5 | +1.5 | LSB | – | P_5.8.8 |
| Integral Nonlinearity (INL) | – | -3 | ±1.5 | 3 | LSB | – | P_5.8.9 |

### 5.8.2 Measurement Unit (VBAT_SENSE - Supply Voltage Attenuator)

**Table 31 Supply voltage signal conditioning**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Battery Voltage Measurement $V_{BAT\_SENSE}$** | | | | | | | |
| Nominal operating input voltage range[1)] | $V_{S/BAT\_SENSE}$ | 3 | – | 20 | V | Max. value corresponds to typ. ADC full scale input | P_5.8.10 |
| Measurement input resistance | $R_{in,VS/VBAT\_SENSE}$ | 200 | 289 | 380 | kΩ | PD_N=1 (on-state) | P_5.8.11 |
| Measurement input leakage current | $I_{leak}$ | 0 | – | 1.0 | µA | PD_N=0 (off-state), $V_{BAT\_SENSE}$=13.5V | P_5.8.12 |
| **Overall (calibrated) measurement accuracy after A/D-conversion[2)]** | | | | | | | |
| $V_{BAT\_SENSE}$ / $V_s$ 8-bit ADC | $\Delta V_{BATADC8B}$ | -250 | – | 250 | mV | $V_s$= 5.5V to 18V, $T_j$ = 40..85°C | P_5.8.13 |
| $V_{BAT\_SENSE}$ / $V_s$ 10-bit ADC | $\Delta V_{BATADC10B}$ | -200 | – | 200 | mV | $V_s$= 5.5V to 18V, $T_j$ = 40..85°C | P_5.8.14 |

## 5.9 ADC - 10-Bit

### 5.9.1 VAREF

#### 5.9.1.1 Functional Range

**Table 34 Functional Range**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VAREF input voltage | $V_{AREF\_IN}$ | 0 | – | $V_{DDP}$+0.3 | V | – | P_5.9.1 |

#### 5.9.1.2 Electrical Characteristics

**Table 35 10-Bit ADC - VAREF**

$V_S$ = 5.5 V to 27 V, $T_j$ = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output Capacitance | $C_{VAREF}$ | 0.1 | – | 1 | µF | ESR < 1Ω | P_5.9.2 |
| Reference output voltage | $V_{AREF}$ | 4.95 | 5 | 5.05 | V | $V_s$ > 5.5V | P_5.9.3 |
| DC Supply voltage rejection | $DC_{PSRVAREF}$ | 30 | – | – | dB | 1) | P_5.9.4 |
| Supply voltage ripple rejection | $AC_{PSRVAREF}$ | 26 | – | – | dB | 1) $V_s$= 13.5V; f=0 ... 1KHz; Vr=2Vpp | P_5.9.5 |
| Turn ON time | $t_{so}$ | – | – | 200 | µs | 1) Cext=100nF PD_N to 99.9% of final value (test setup: measure 1τ, calculate 5τ. | P_5.9.6 |

1) Not subject to production test, specified by design.