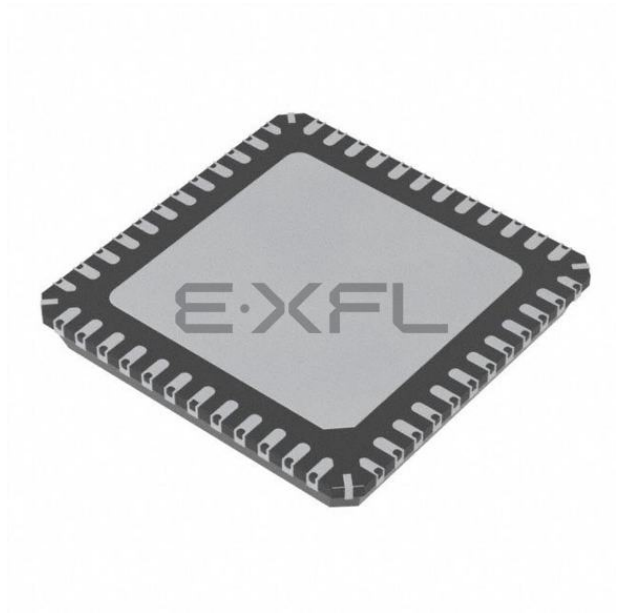

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qxxuma1

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832 device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9832QV	40 MHz	1	5	36 kByte	11	no
TLE9832QX	40 MHz	1	5	36 kByte	11	no

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P0.5	25	I/O	I/PU	MRST_0 EXINT0_0 T21EX_2 T1 CCPOS2_1 COUT60_0	SSC master receive input / slave transmit output External interrupt input 0 Timer 21 external trigger input Timer 1 input CCU6 hall input 2 CCU6 capture/compare channel 0 output
P1				**Port 1** Port 1 is an 5-Bit bidirectional general purpose I/O port. Alternate functions can be assigned as follows: CCU6, Timer 0, Timer 1 Timer 21, SSC, external interrupt input and clock output.	
P1.0	14	I/O	I	T0_1 CC61_0 SCK_1 EXF21_3	Timer 0 input CCU6 capture/compare channel 1 input/output SSC clock input (for slave) / output (for master) Timer 21 external flag output
P1.1	15	I/O	I	T1_1 MTSR_1 T21EX_3 COUT61_0	Timer 1 input SSC master transmit output/slave receive input Timer 21 external trigger input CCU6 capture/compare channel 1 output
P1.2	16	I/O	I	EXINT0_1 T21_1 MRST_1 CCPOS2_2 COUT63_0	External interrupt input 0 Timer 21 input SSC master receive input/slave transmit output CCU6 hall input 2 CCU6 capture/compare channel 3 output
P1.3	39	I/O	I	EXINT1_1 CC62_0 CCPOS0_2 EXF21_1	External interrupt input 1 CCU6 capture/compare channel 2 input/output CCU6 hall input 0 Timer 21 external flag output
P1.4	26	I/O	I	EXINT2_1 T21EX_1 CCPOS1_2 CLKOUT_1 COUT62_0	External interrupt input 2 Timer 21 external trigger input CCU6 hall input 1 Clock output CCU6 capture/compare channel 2 output
P2				**Port 2** Port 2 is an 5-Bit general purpose input-only port. Alternate functions can be assigned as follows: CCU6, Timer 0, Timer 1, Timer 21 and external interrupt input It is also used as analog inputs for the 10-Bit ADC (ADC1).	
P2.1	37	I	I	AN1 CCPOS0_0 EXINT1_0 T12HR_1 CC61_1	ADC1 analog input channel 1 CCU6 hall input 0 External interrupt input 1 CCU6 Timer 12 hardware run input CCU6 capture/compare channel 1 input

3 Functional Description

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 8-Bit state-of-the-art microcontroller, compatible to the standard 8051 core with On-Chip Debug Support (OCDS), is available. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore one High Side Switch (e.g. for driving LEDs or cyclic powering of switches), two Low Side Switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit (MCU) supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs, via the GPIO ports or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a VQFN-48-22 and VQFN-48-29 package with 0.5 mm pitch and is designed to withstand the severe conditions of automotive applications.

3.7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a sub-module in the System Control Unit (SCU). The Watchdog Timer provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT helps to abort an accidental malfunction of the TLE9832 in a user-specified time period. When enabled, the WDT will cause the TLE9832 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing an TLE9832 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

The WDT is disabled by default.

In debug mode, the WDT is suspended by default and stops counting (its debug suspend Bit is set by default i.e. MODSUSP.WDTSUSP = 1). Therefore during debugging, there is no need to refresh the WDT.

Features

- 16-Bit Watchdog Timer
- Programmable reload value for upper 8 Bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$

The Watchdog Timer is a 16-Bit timer, which is incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-Bit timer is realized as two concatenated 8-Bit timers. The upper 8 Bits of the Watchdog Timer can be preset to a user-programmable value via a watchdog service access in order to vary the watchdog expiring time. The lower 8 Bits are reset on each service access. **Figure 13** shows the block diagram of the watchdog timer unit.

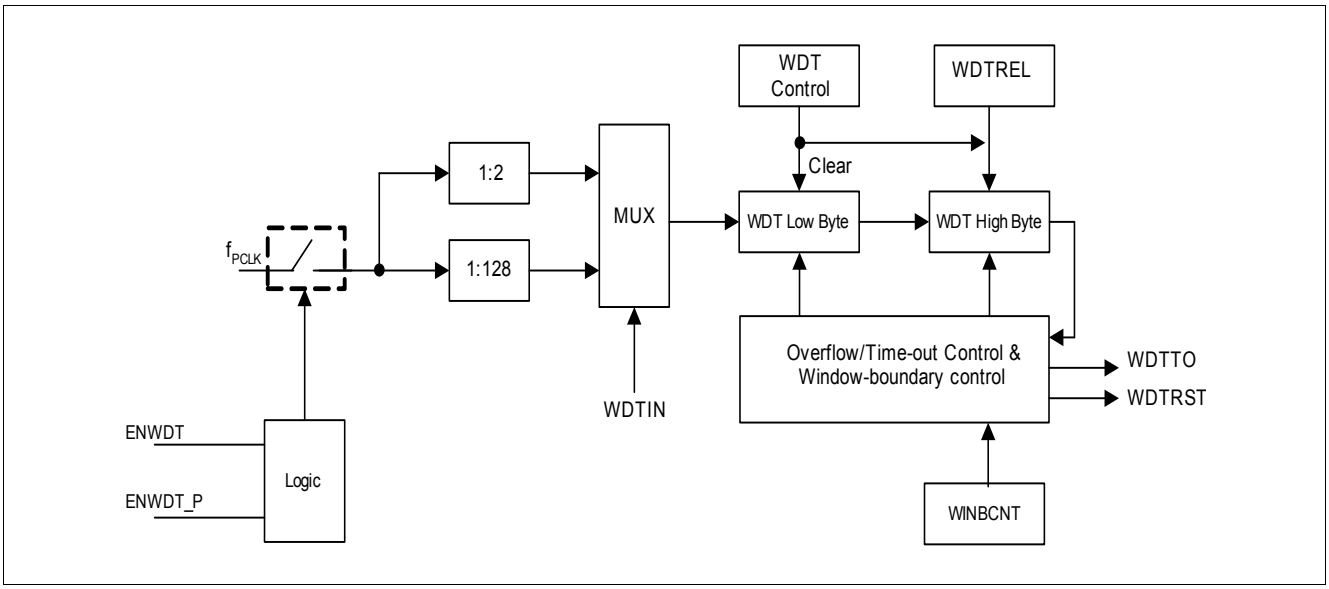

Figure 13 WDT Block Diagram

3.8 Interrupt System

The TLE9832 supports 14 interrupt vectors with four priority levels. Eleven of these interrupt vectors are assigned to the on-chip peripherals: Timer 0, Timer 1, UART, SSC and A/D Converter are each assigned to one dedicated interrupt vector; while Timer2, Timer21, MDU, LIN and the Capture/Compare Unit share six interrupt vectors.

Two interrupt vectors are assigned to the external interrupts. External interrupts 0 to 1 are each assigned to one dedicated interrupt vector, external interrupt 2 shares on interrupt vector with Timer21 and the MDU.

One interrupt vector is dedicated to the XINT interrupt events whose interrupt flags are also located in registers in XSFR area.

A non-maskable interrupt (NMI) with the highest priority is shared by the following:

- Watchdog Timer, warning before overflow
- MI_CLK Watchdog Timer overflow event
- PLL, loss of lock
- Flash, on operation complete, e.g. erase.
- OCDS, on user IRAM event
- Oscillator watchdog detection for too low oscillation of f_{OSC}
- Flash map error
- Uncorrectable ECC error on Flash, XRAM and IRAM
- VSUP supply pre warning when any supply voltage drops below or exceeds any threshold.

Figure 14, **Figure 15**, **Figure 16**, **Figure 17** and **Figure 18** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags. **Figure 19** gives the corresponding overview for the NMI sources.

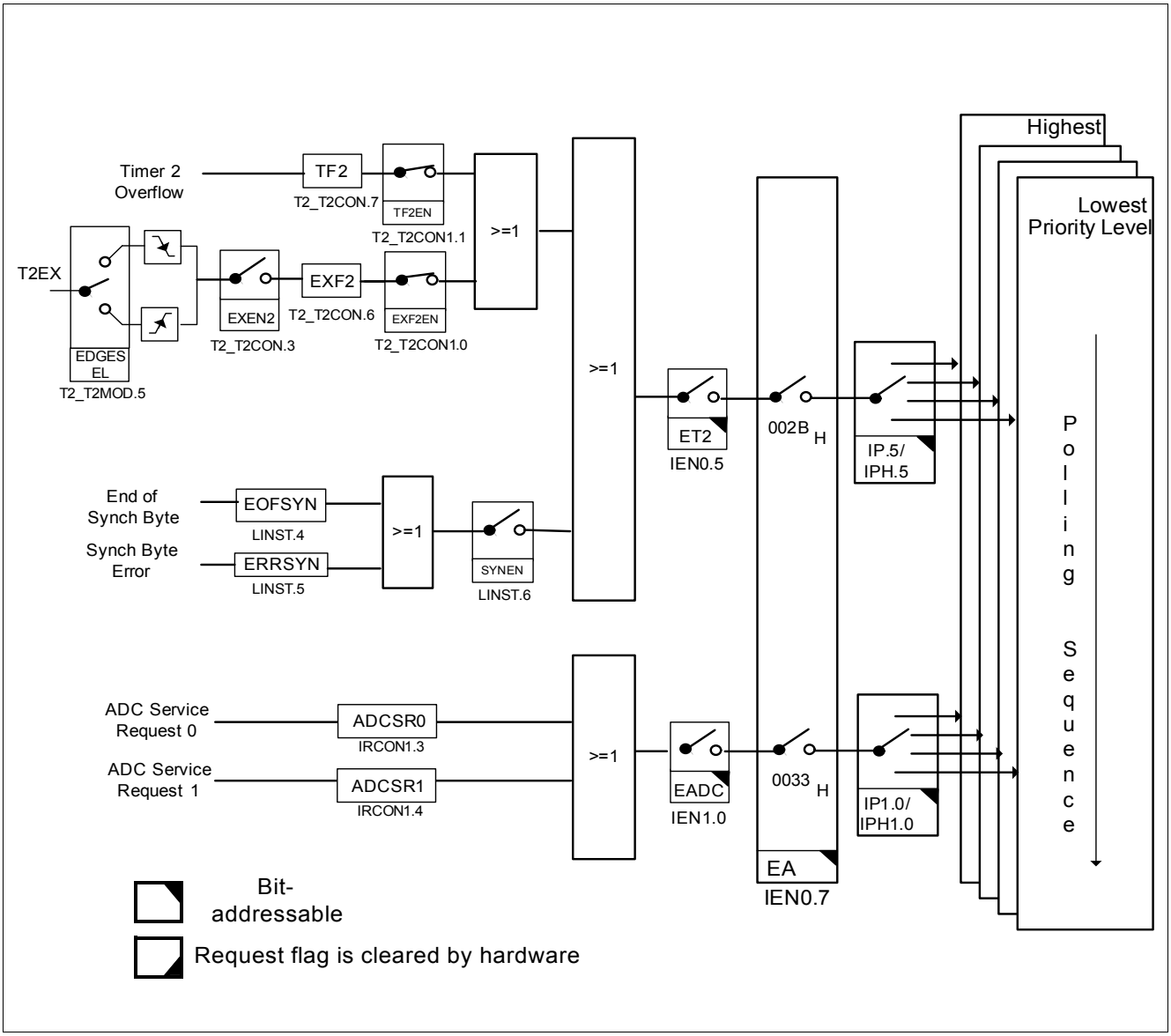

Figure 15 Interrupt Request Sources (Part 2)

3.14 Capture/Compare Unit 6 (CCU6)

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status Bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and Low Side Switches)
- 16-Bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-Bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

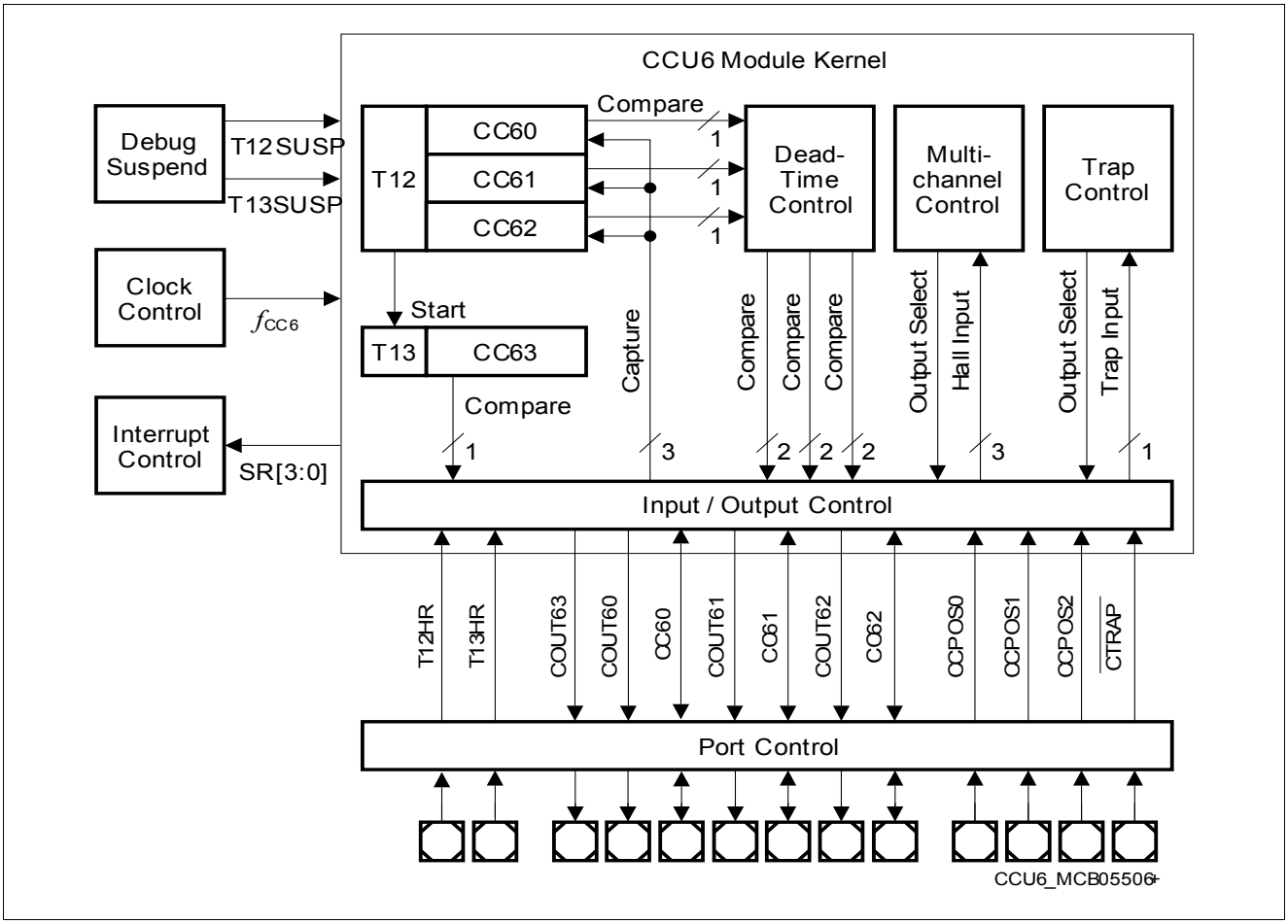

Figure 22 CCU6 Block Diagram

3.15 UART

The UART provides a full-duplex asynchronous receiver/transmitter, i.e. it can transmit and receive simultaneously. It is also receive-buffered, i.e. it can commence reception of a second Byte before a previously received Byte has been read from the receive register. However, if the first Byte still has not been read by the time reception of the second Byte is complete, one of the Bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

UART Features

- Full-duplex asynchronous modes
  - 8-Bit or 9-Bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch Byte detection

UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-Bit shift register. In mode 1, it operates as an 8-Bit serial port. In modes 2 and 3, it operates as a 9-Bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting Bits SM0 and SM1 to their corresponding values, as shown in **Table 9**.

Table 9 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-Bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-Bit shift UART	Variable
1	0	Mode 2: 9-Bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-Bit shift UART	Variable

3.16 LIN Transceiver

The LIN module is a transceiver for the Local Interconnect Network (LIN) compliant to the standards LIN 1.3, LIN 2.0 and LIN 2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kbps and 20 kbps. Additionally baud rates up to 40 kBaud are implemented.

The LIN module offers several different operation modes, including a Sleep Mode and the normal operation mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kBaud is also implemented.

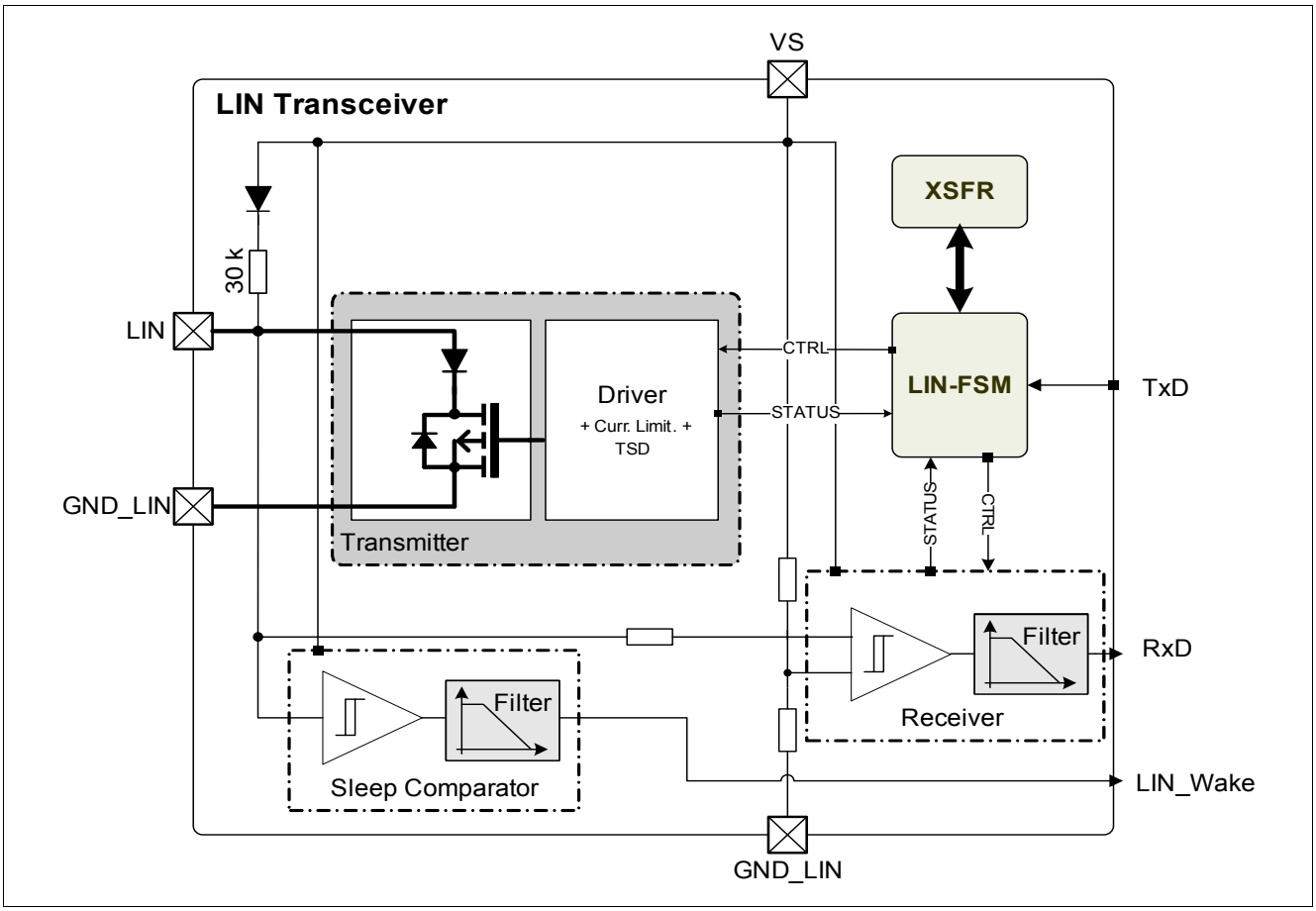

Figure 23 LIN Transceiver Block Diagram

3.17 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format

3.18 Measurement Unit

The measurement unit is a functional unit that comprises the following associated sub-modules:

- 1 x 8 Bit ADC (ADC2) with 10 inputs. 5 are for single ended input signals and 5 are for differential input signals.
- Monitoring inputs voltage attenuators with two selectable attenuation settings: divide by 4 and divide by 6
- Supply voltage attenuators with attenuation of VBAT_SENSE, VS, VDDP and VDDC.
- VBG monitoring of 8-Bit ADC (ADC2) to guarantee functional safety requirements.
- Low Side Switch current sensing of LS1 and LS2. Allows a scalable overcurrent pre warning.
- Temperature sensor for monitoring the chip temperature and Low Side Switches temperature.
- Supplement block with reference voltage generation, bias current generation, voltage buffer for Flash reference voltage, voltage buffer for analog module reference voltage and test interface.

Table 10 Measurement functions and associated modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-Bit ADC. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the Flash module
8-Bit ADC (ADC2)	8-Bit ADC module with 10 multiplexed inputs	1. 5 single-ended inputs 0 ... 1.23V 2. 5 differential inputs 0 ... 1.23V (allocation see following overview figure)
10-Bit ADC (ADC1)	10-Bit ADC module including analog test bus interface - part of µC subsystem	1. VBAT_SENSE measurement on channel 0 of ADC1. 2. VS measurement on channel 2 of ADC1. 3. MONx measurement on channel 6 of ADC1. 4. 5 additional (5V) analog inputs from Port 2.
Supply Voltage Attenuator	Resistive supply voltage attenuator	Scales down the supply voltages of the system to the input voltage range of ADC1 and ADC2.
Monitoring Input Attenuator	Resistive attenuator for (HV)	Scales down 5 monitoring input voltages to the input voltage range of the ADC1.
Central Temperature - Low Side Switch Temperature Sensor	Temperature sensor readout with two multiplexed ΔV_{be} sensing elements	Generates outputs voltage which is a linear function of the local chip (junction) temperature.
Measurement Core Module	Digital signal processing and ADC control unit	1. Generates the control signal for the 8-Bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

The structure of the measurement functions module is shown in **Figure 29**.

3.23 Low Side Switches

The general purpose Low Side Switches are intended to control an on-board relay. They include an over-current detection function.The module is designed for on-board connections.

Features

- Multi purpose Low Side Switch
  - configurable over-current protection with automatic shutdown
  - configurable over-temperature protection with automatic shutdown
- Intended for relay driver
  - PWM relay driver
  - simple relay driver
- Integrated clamping
- PWM capability up to 25 kHz
- Selectable PWM source: PWM-Unit or CCU6

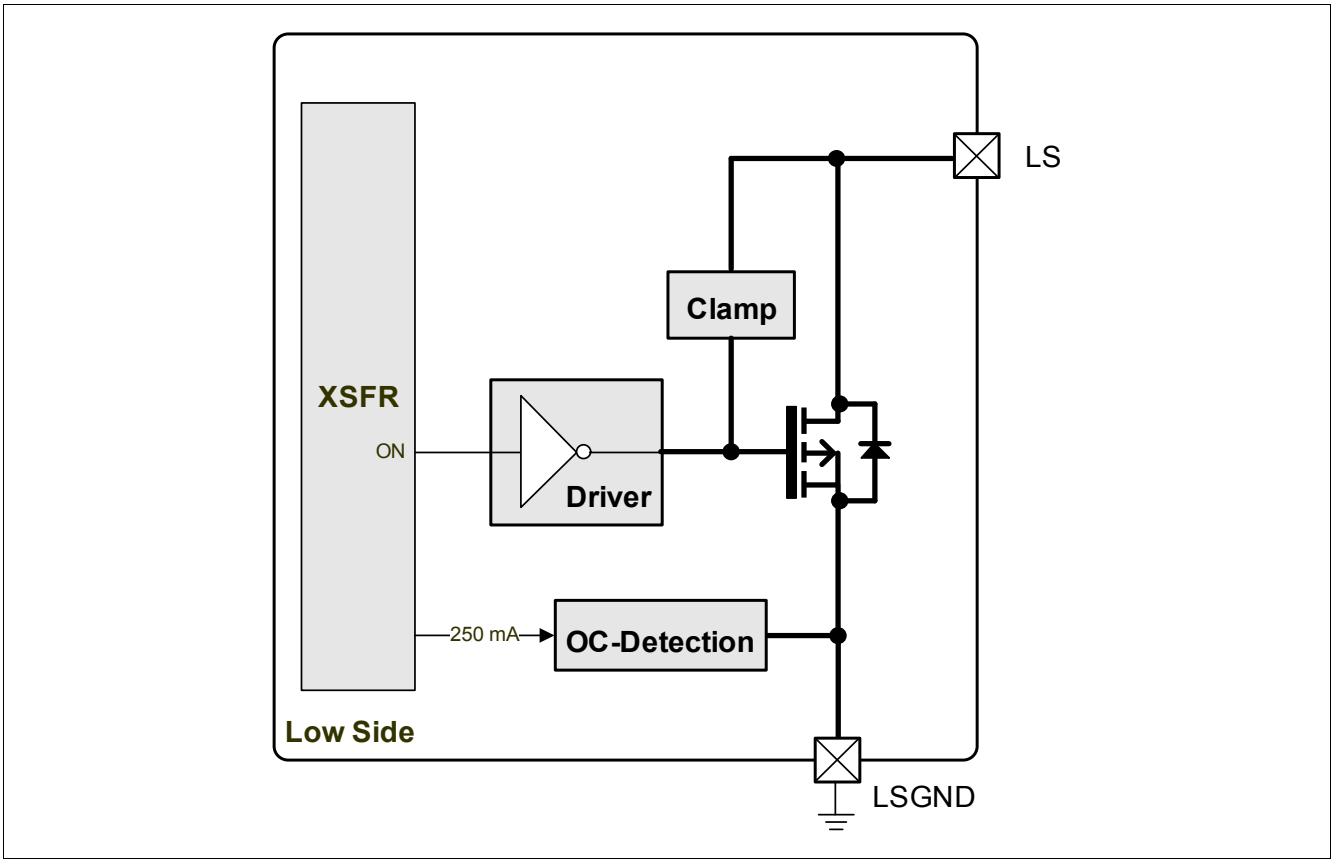

Figure 29 Module Block Diagram

3.25 Debug System

The On-Chip Debug Support (OCDS) provides the basic functionality required for software development and debugging of XC800 based systems.The OCDS design is based on the following principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a monitor program
- Use standard interfaces to communicate with the Host (a debugger)

Features

- Set breakpoints on instruction address and on address range within the program memory
- Set breakpoints on internal RAM address range
- Support unlimited amount of software breakpoints in Flash / RAM code region
- Step through the program code

The Monitor Mode Control (MMC) block at the center of the OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals. After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work data and monitor stack). The OCDS system is accessed through the DAP, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated TMS pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after TLE9832 has been started in OCDS mode.

4.2 Connection of N.C. Pins

It is recommended to connect N.C. pins to GND unless otherwise specified. Since pins 10 and 46 are located next to high voltage pins (VS, MON5, LS1) these 2 N.C. pins can be also left unconnected in order to avoid huge current flow and damage of the system in case of short-circuit.

4.3 Connection of ADCGND Pin

The ADCGND pin is chip-internal connected to reference ground. In order to provide full offset compensation and achieve full accuracy of ADC1 the ADCGND pin must not be connected to board ground. ADCGND pin should be connected with a capacitor (100 nF) to VAREF only.

4.4 Connection of Exposed Pad

It is recommended to connect the exposed pad to GND.

4.5 Voltage Regulators-Blocking Capacitors

Table 11 External Component Recommendation

Symbol	Function	Comment
C_{VS}	blocking capacitor at VS pin	> 20 µF Elco + 100 nF Ceramic, ESR < 1 Ω
C_{VDDP}	blocking capacitor at VDDP pin	1 µF typ. + 100 nF Ceramic, ESR < 1 Ω
C_{VDDEXT}	blocking capacitor at VDDEXT pin	100 nF typ., ESR < 1 Ω
C_{VDDC}	blocking capacitor at VDDC pin	> 330 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VAREF}	blocking capacitor at VAREF pin	> 100 nF, ESR < 1 Ω

4.6 Additional External Components

Table 12 External Component Recommendation

Symbol	Function	Comment
C_{HSx}	HF blocking capacitor at HSx pin	6.8 nF
R_{MONx}	resistor at MONx pin	1 kΩ
$R_{VBAT\_}$	resistor at VBAT_SENSE pin	1 kΩ

5.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

5.2.1 PMU I/O Supply Parameters VDDP

Table 19 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDP}	0	–	60	mA	1)	P_5.2.1
Required Output Capacitance	C_{VDDP}	0.1	–	10	µF	1) ESR < 1Ω	P_5.2.2
Output Voltage including line regulation	V_{DDPOUT}	4.9	5.0	5.1	V	I_{load} < 90mA;Vs > 5.5V	P_5.2.3
Output Drop	$Vs_{V\ DDPout}$	–	–	+400	mV	I_{load} < 70mA; 3V < V_s < 5.5V	P_5.2.4
Dynamic Load Regulation	$V_{VDDPLOR}$	-50	–	50	mV	1) 2 ... 70mA; C=470nF; dI/dt=100mA/µs	P_5.2.5
Dynamic Line Regulation	$V_{VDDPLIR}$	-25	–	25	mV	1) V_s= 5.5 ... 20V; dV/dt=5V/µs	P_5.2.6
Power Supply Ripple Rejection	$P_{SSRVDDP}$	50	–	–	dB	1) V_s= 13.5V; f=0 ... 1KHz; Vr=2Vpp	P_5.2.7
Over Voltage Detection	V_{DDPOV}	5.05	–	5.4	V	V_s > 5.5V; Overvoltage leads to SUPPLY_NMI	P_5.2.8
Under Voltage Reset	V_{DDPUV}	2.4	–	2.7	V	V_s > 5.5V	P_5.2.9
Over Current Shutdown	I_{VDDPOC}	90	–	180	mA	–	P_5.2.10

1) Not subject to production test, specified by design

5.3 System Clocks

5.3.1 Oscillators and PLL

Table 22 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK1}	14	18	22	MHz	this clock is used at startup and can be used in case the PLL fails	P_5.3.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake and cyclic sense	P_5.3.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation	f_{TRIMST}	-1.5%	5	+1.5%	MHz	[1] with respect to nominal configured system frequency within one LIN message (< 10ms ... 100ms)	P_5.3.3
Long term frequency deviation	f_{TRIMLT}	-3.0%	5	+3.0%	MHz	with respect to nominal configured system frequency over lifetime and temperature	P_5.3.4
CGU-OSC Start-up time	T_{OSC}	–	–	10	µs	startup time OSC from Sleep Mode and Stop Mode, power supply stable	P_5.3.5
PLL (Clock Generation Unit Microcontroller)							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_5.3.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_5.3.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_5.3.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_5.3.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_5.3.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_5.3.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_5.3.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_5.3.13
Peak period jitter	t_{jp}	-500	–	500	ps	for K=1	P_5.3.14

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current (all other)	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.5.12
Pull level keep current	I_{PLK}	-240	–	+240	µA	6) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.5.13
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	6) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.5.14
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	–	P_5.5.15

1) Not subject to production test, specified by design.

2) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

3) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). However, only the levels for nominal output currents are verified.

4) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

5) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (ΔV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × ΔV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

6) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IH} for a pull-up; V_{PIN} ≤ V_{IL} for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{IL} for a pull-up; V_{PIN}≥ V_{IH} for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

Table 31 Supply voltage signal conditioning

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
V_{DD5_SENSE}	ΔV_{DDP_SENSE}	-150	–	150	mV	–	P_5.8.15
V_{DD1V5_SENSE}	ΔV_{DDC_SENSE}	-45	–	45	mV	–	P_5.8.16

1) This parameter is not subject to production test

2) The device is calibrated based on an external 1kΩ resistor

5.8.3 Measurement Functions Monitoring Input Voltage Attenuator

Table 32 Monitoring input voltage attenuation

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power Supply							
Input resistance[1)]	R_{IN}	300	400	500	kΩ	PD_N=1 (on-state) V_{MON_X}=0 to 18V if VMON_SEN_SEL_INRANGE = 0	P_5.8.17
Input resistance	R_{IN}	250	–	–	kΩ	V_{MON_X} =0 to 28V if VMON_SEN_SEL_INRANGE = 1 >200 kΩ under all other conditions	P_5.8.18
Timing Characteristics							
Analog Multiplexer Settling Time	$T_{MUXsettle}$	–	–	30	µs	This time frame is valid from writing the corresponding selection register to proper settling of the voltage at channel 7 of the 10-Bit ADC	P_5.8.19
Overall (calibrated) measurement accuracy after A/D-conversion							
V_{MONx} 10-bit ADC	$\Delta V_{MONxADC10B}$	-200	–	200	mV	V_s=5.5V to 18V, T_j = 40..85°C	P_5.8.20

1) Not subject to production test, specified by design.

1)TUE is tested at V_{AREF} = $5V$±1%, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if V_{AREF} and V_{AGND} remain stable during the measurement time.

2) Only valid in case of external supplied reference voltage.
3) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be 000_H or $3FF_H$, respectively.
4) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
5) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
6) Not subject to production test, specified by design.
7) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors. All error specifications are based on measurement methods standardized by IEEE 1241.2000.
8) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

5.10 High-Voltage Monitor Input

Table 37 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_s	0.5*V_s	0.6*V_s	V	without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.1
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_s	0.06*V_s	0.12*V_s	V	in all modes; without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.2
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = low	$I_{PU, MONx}$	-20	-10	-1	µA	0 V < V_{MON_IN} < V_s - 2 V	P_5.10.3
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PU, MONx}$	-20	-10	-1	µA	0.6*V_s < V_{MON_IN} < V_s - 2 V	P_5.10.4
Pull-down current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < V_s	P_5.10.5
Pull-down current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < 0.4*V_s	P_5.10.6
Input leakage current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = low	$I_{LK,I}$	-2	–	2	µA	0 V < V_{MON_IN} < 28 V	P_5.10.7

The Parameters of the analog measurement are listed in the chapter Measurement Interface.