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What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qxxuma2

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1 Summary of Features

- High performance XC800 core
 - compatible to standard 8051 core
 - up to 40 MHz clock frequency
 - two clocks per machine cycle architecture
 - two data pointers
- On-chip memory
 - 32 kByte + 4 kByte Flash for program code and data (4 kByte EEPROM emulation built-in)
 - 512 Byte One Time Programmable Memory (OTP)
 - 512 Byte 100 Time Programmable Memory (100TP)
 - 256 Byte RAM, 3 kByte XRAM
 - BootROM for startup firmware and Flash routines
- Core logic supply at 1.5 V
- On-chip OSC and PLL for clock generation
 - Loss of clock detection with fail safe mode for power switches
- Watchdog timer (WDT) with programmable window feature for refresh operation and warning prior to overflow
- General-purpose I/O Port (GPIO) with wake-up capability
- Multiplication/division unit (MDU) for arithmetic calculation
- Software libraries to support floating point and MDU calculations
- Five 16-Bit timers - Timer 0, Timer 1, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6) with Timer 12 and Timer 13
- Full duplex serial interface (UART) with LIN support
- Synchronous serial channel (SSC)
- On-chip debug support via 2-wire Device Access Port (DAP)
- LIN Bootstrap loader (LIN BSL)
- LIN transceiver compliant to LIN 1.3, LIN 2.0 and LIN 2.1
- 2 x Low Side Switches with clamping capability incl. PWM functionality, e.g. as relay driver
- 1x High Side Switch with cyclic sense option and PWM functionality, e.g. for LED or powering of switches
- 5 x High Voltage Monitor Input pins for wake-up and with cyclic sense and analog measurement option
- Measurement unit with 10 channels, 8-Bit A/D Converter (ADC2) and data post processing
- 8 channels, 10-Bit A/D Converter (including battery voltage and supply voltage measurement) (ADC1)
- Single power supply from 3.0 V to 27 V
- Low-dropout voltage regulators (LDO)
- Dedicated 5 V voltage regulator for external loads (e.g. hall sensor)
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
 - MCU slow-down mode
 - Stop Mode
 - Sleep Mode
 - Cyclic wake-up and cyclic sense during Stop Mode and Sleep Mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Overcurrent protection with shutdown
- Supported by a full range of development tools including C compilers, macro assembler packages, emulators, evaluation boards, HLL debugger, programming tools, software packages
- Temperature Range T_j : -40 °C up to 150 °C
- Packages TLE9832QV: VQFN-48-22 and TLE9832QX: VQFN-48-29
- Green package (RoHS compliant)

2 General Device Information

2.1 Pin Configuration

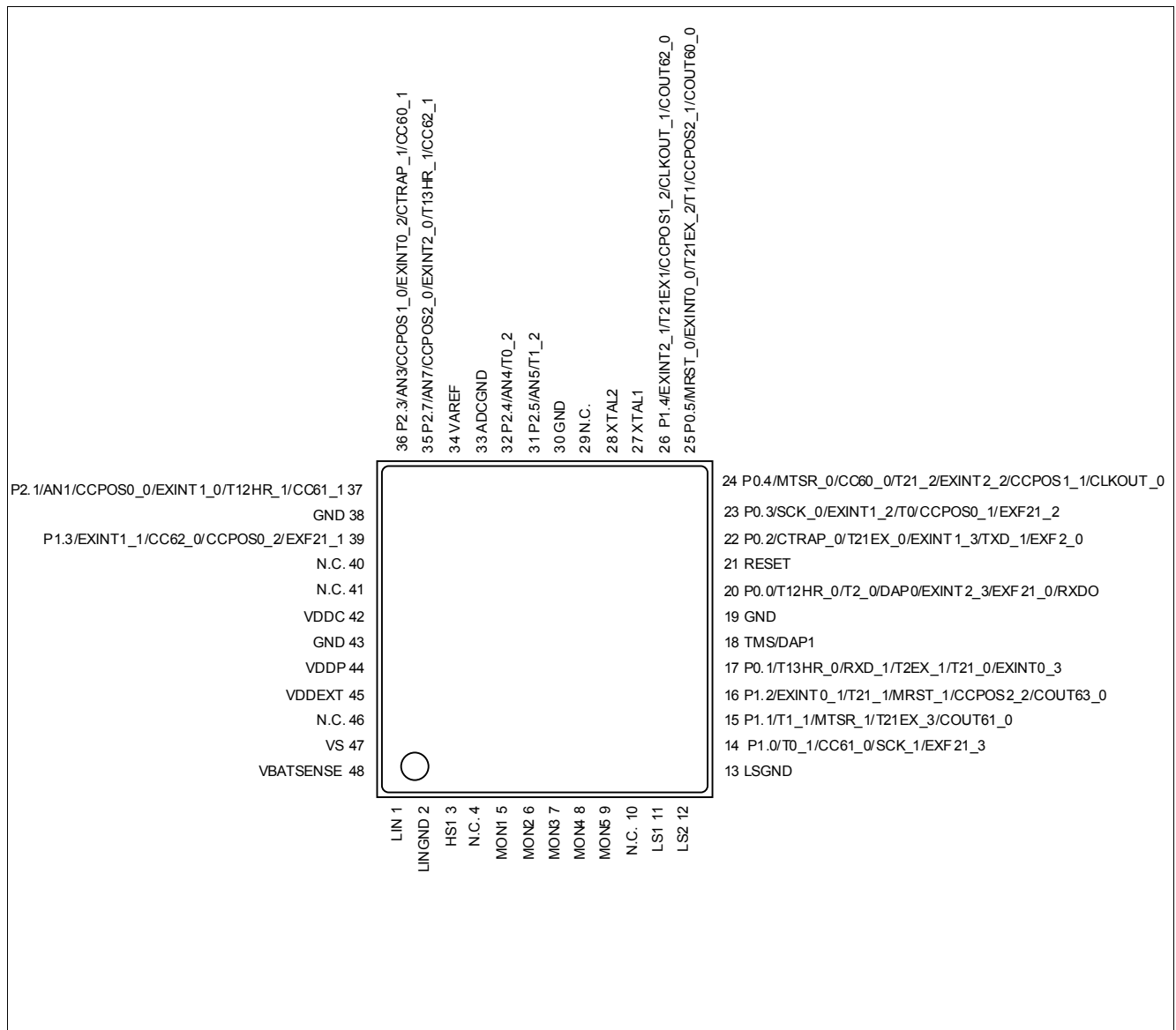


Figure 1 TLE9832 pin configuration, VQFN-48-22 and VQFN-48-29 package (top view)

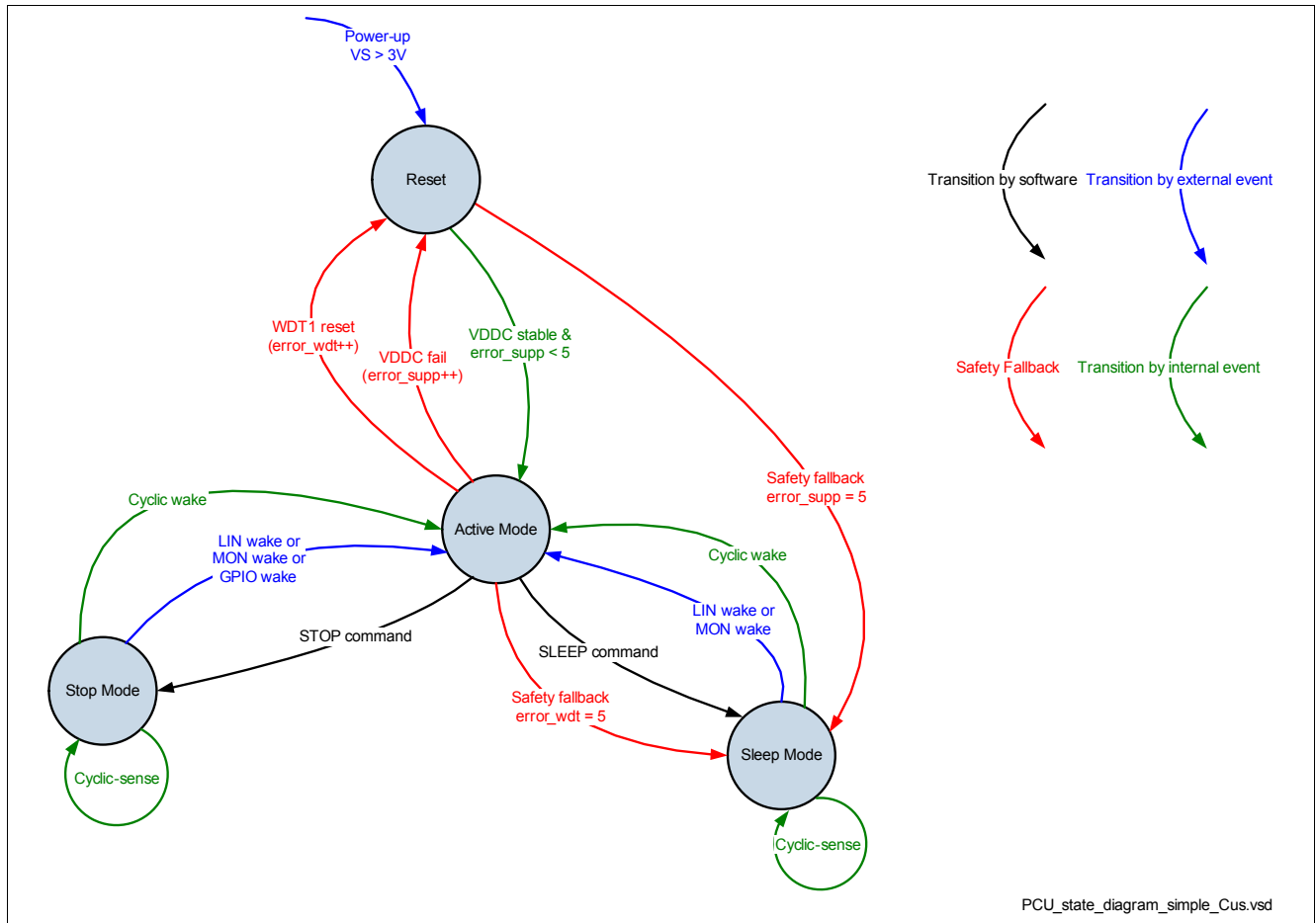


Figure 3 Power Control State Diagram

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9832 is fully operational.

Stop Mode

The Stop Mode is one out of two low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is the second low-power mode. The transition to the low-power modes is done by setting the respective Bits in the MCU mode control register. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins. A wake-up from Sleep Mode behaves similar to a power-on reset.

3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

Features

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/ μ s max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 μ A)
- Cyclic sense option together with GPIOs

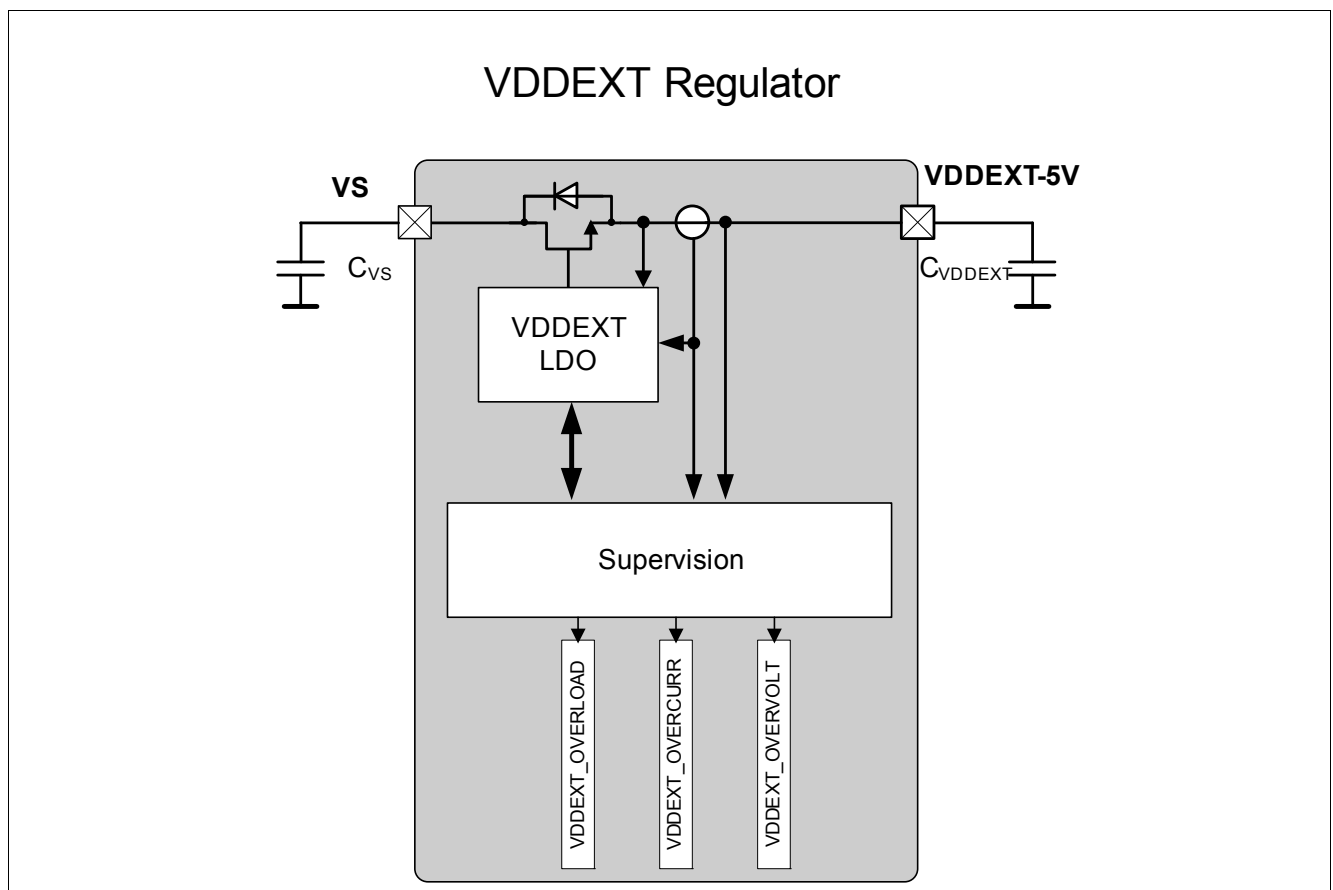


Figure 8 Module Block Diagram

Functional Description

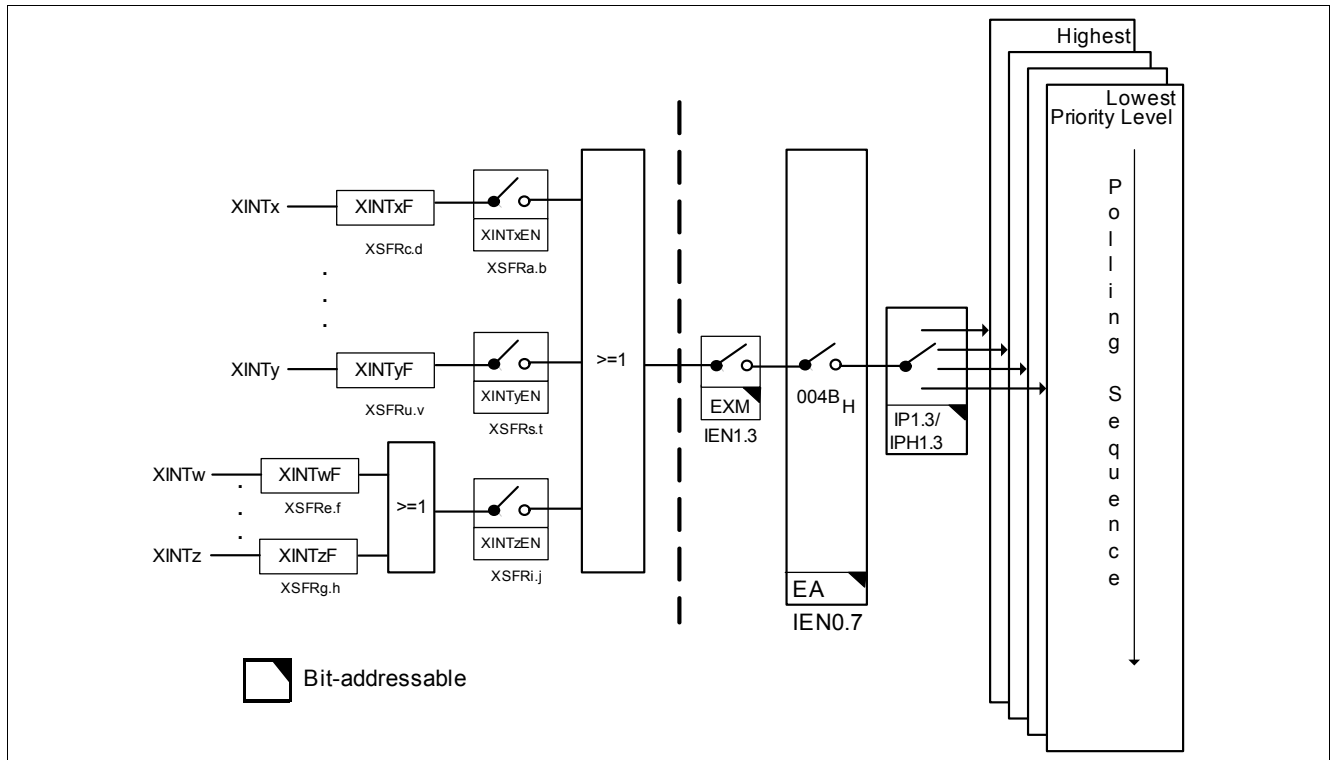


Figure 17 Interrupt Request Sources (Part 4)

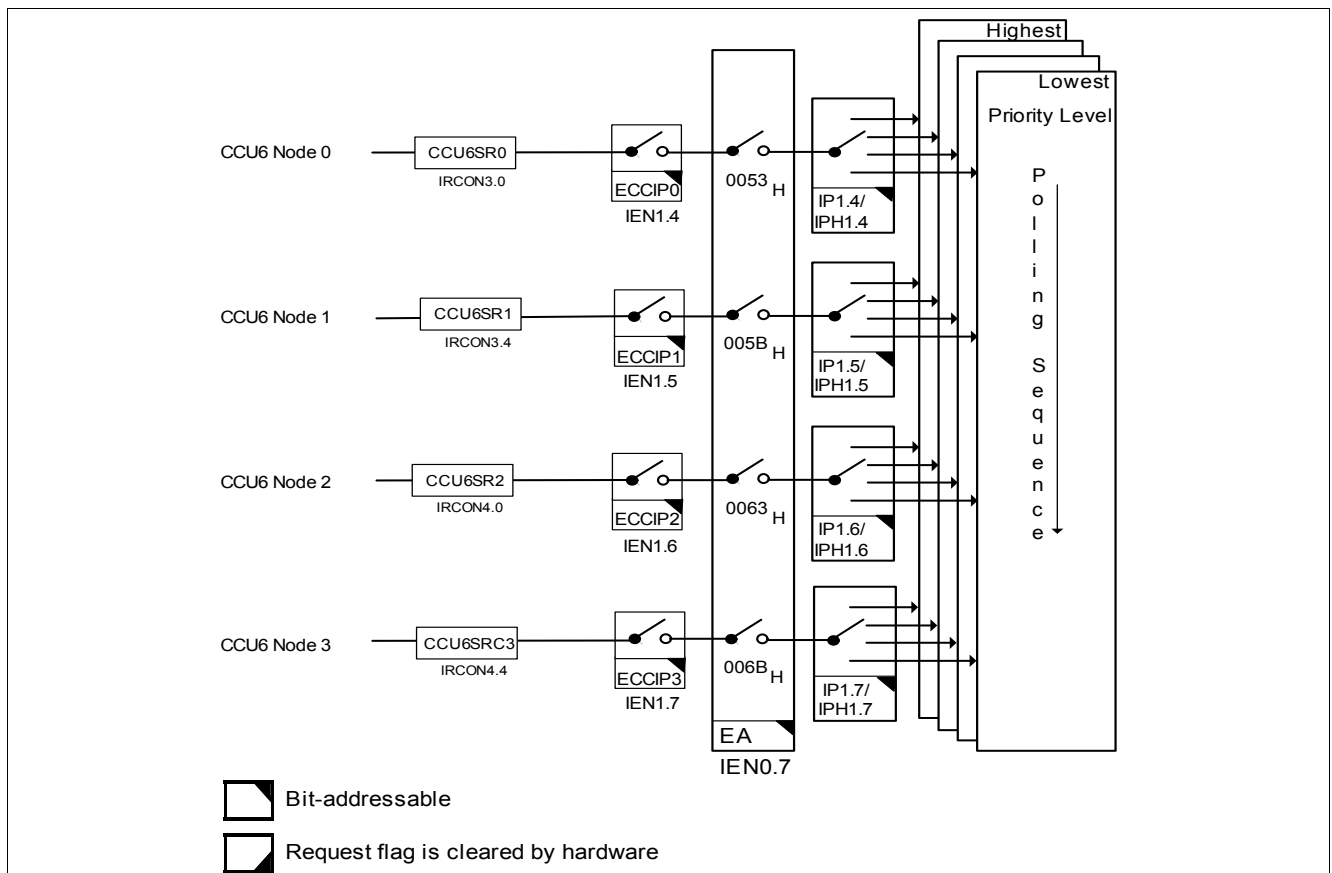


Figure 18 Interrupt Request Sources (Part 5)

3.14 Capture/Compare Unit 6 (CCU6)

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status Bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and Low Side Switches)
- 16-Bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-Bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

- Programmable number of data Bits: 2 to 8 Bits
- Programmable shift direction: LSB or MSB shift first
- Programmable clock polarity: idle low or high state for the shift clock
- Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

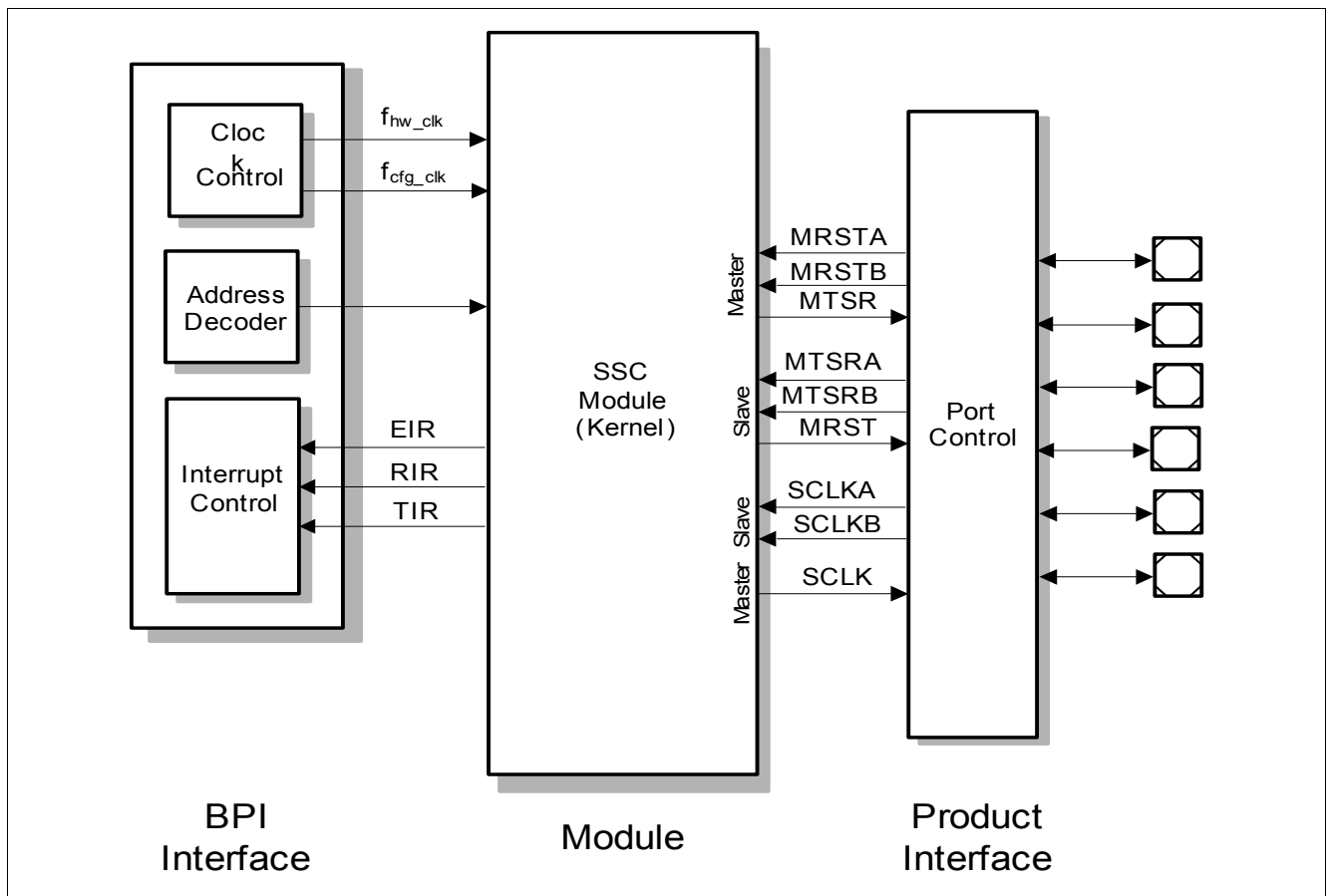


Figure 24 SSC Interface Diagram

3.19 Measurement Core Module (incl. ADC2)

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of ten identical channel units attached to the outputs of the 10-channel 8-Bit ADC (ADC2). It processes ten channels, where the channel sequence and prioritization is programmable within a wide range.

Features

- 10 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
 - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
 - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable interrupts and status for all channel thresholds

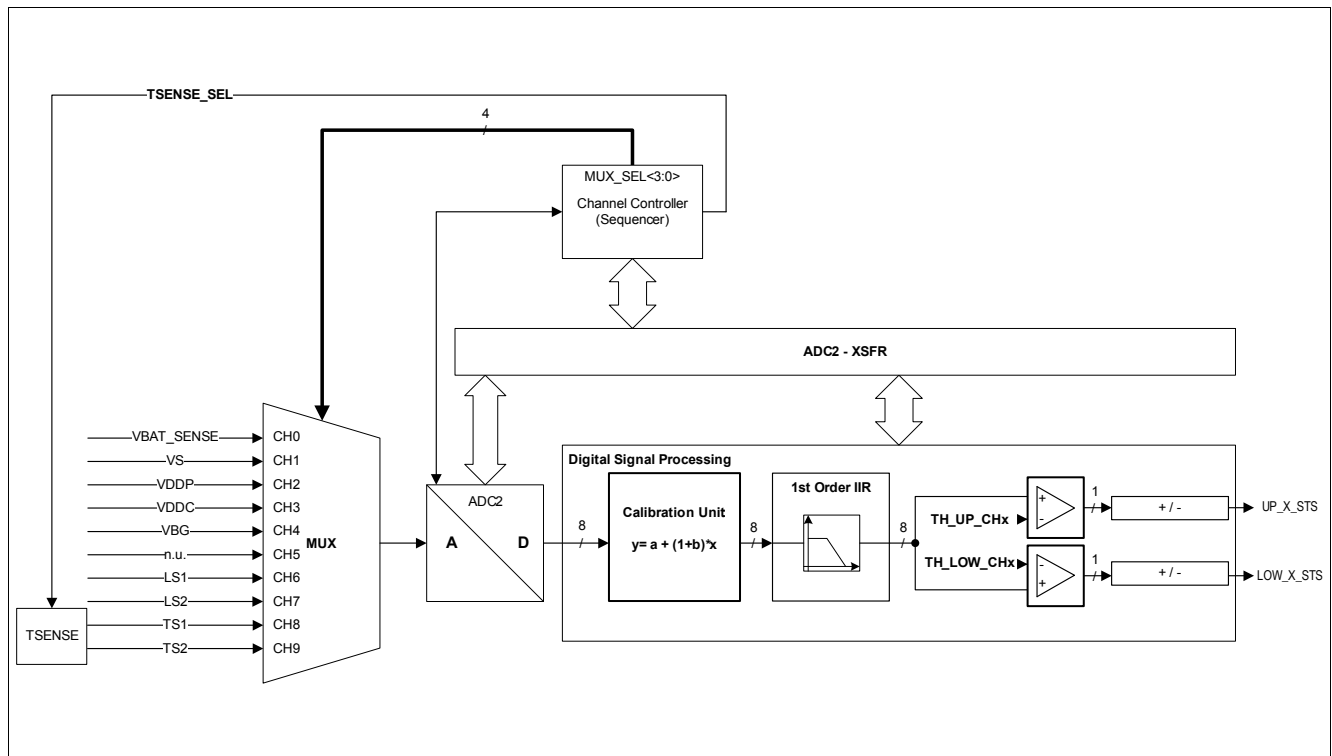


Figure 26 Measurement Core Module Block Diagram

3.20 Analog Digital Converter (ADC1)

The TLE9832 includes a high-performance 10-Bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN1, AN3 - AN5, AN7.

Features

- Successive approximation
- 8-Bit or 10-Bit resolution
- 8 analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.24 PWM Generator

The PWM generator provides up to two configurable PWM channels in order to drive the Low Side Switches LS1, LS2 and the High Side Switch HS1 in a PWM mode.

Features

- Programmable modulation frequency per channel
- Programmable duty-cycle per channel with glitch-free reprogramming
- PWM frequency up to 25 kHz
- Duty-cycle resolution from 0 % ... 100 % in steps of 0.5 %

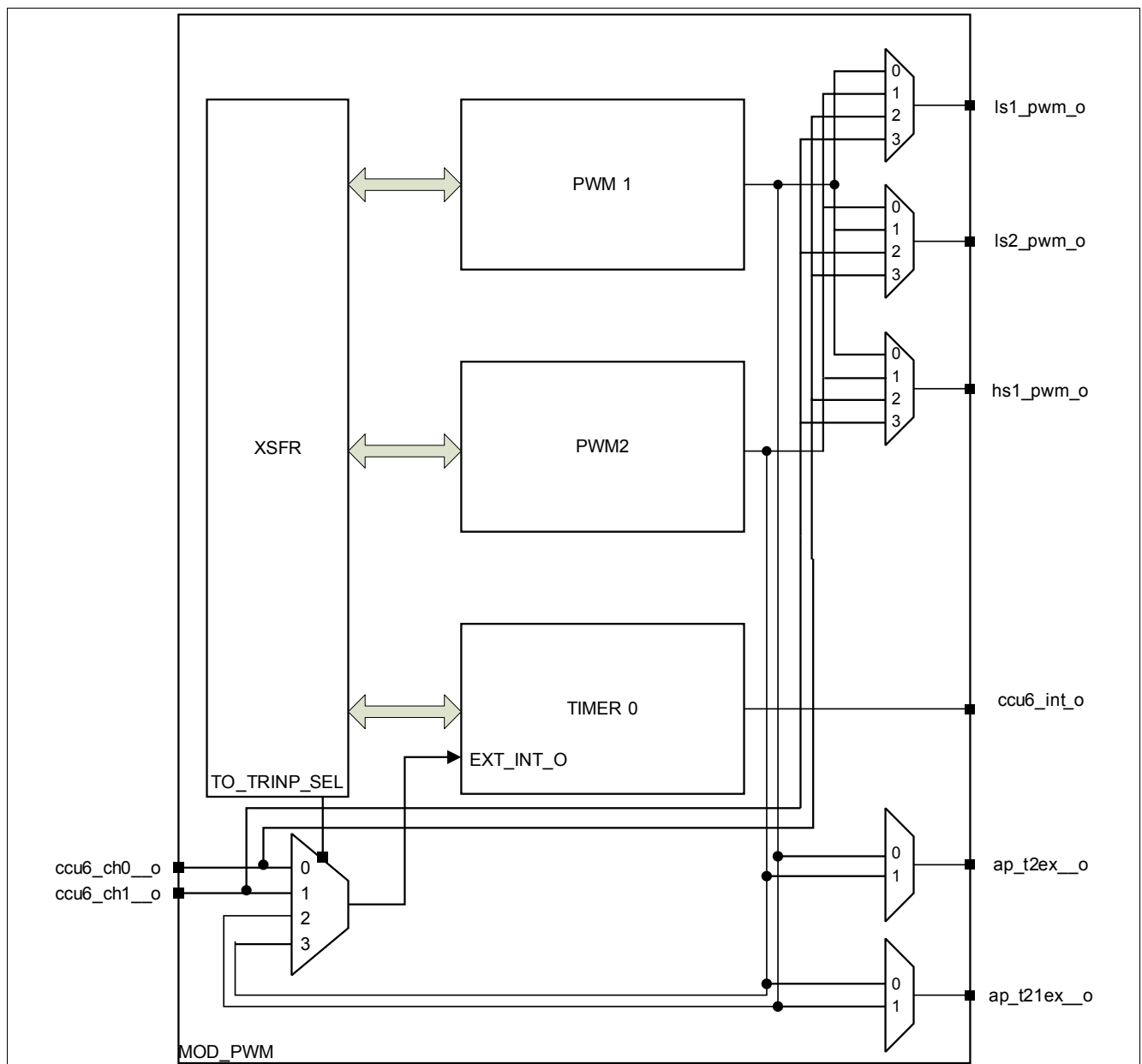


Figure 30 Module Block diagram of PWM module and included PWM switching matrix

4 Application Information

4.1 Electric Drive Application

Figure 31 shows the TLE9832 in an electric drive application setup controlling a DC-brush motor. The two Low Side Switches are controlling a relay each. An external FET allows to control the window lift motor with a PWM signal as generated with the CCU6 module of the microcontroller.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

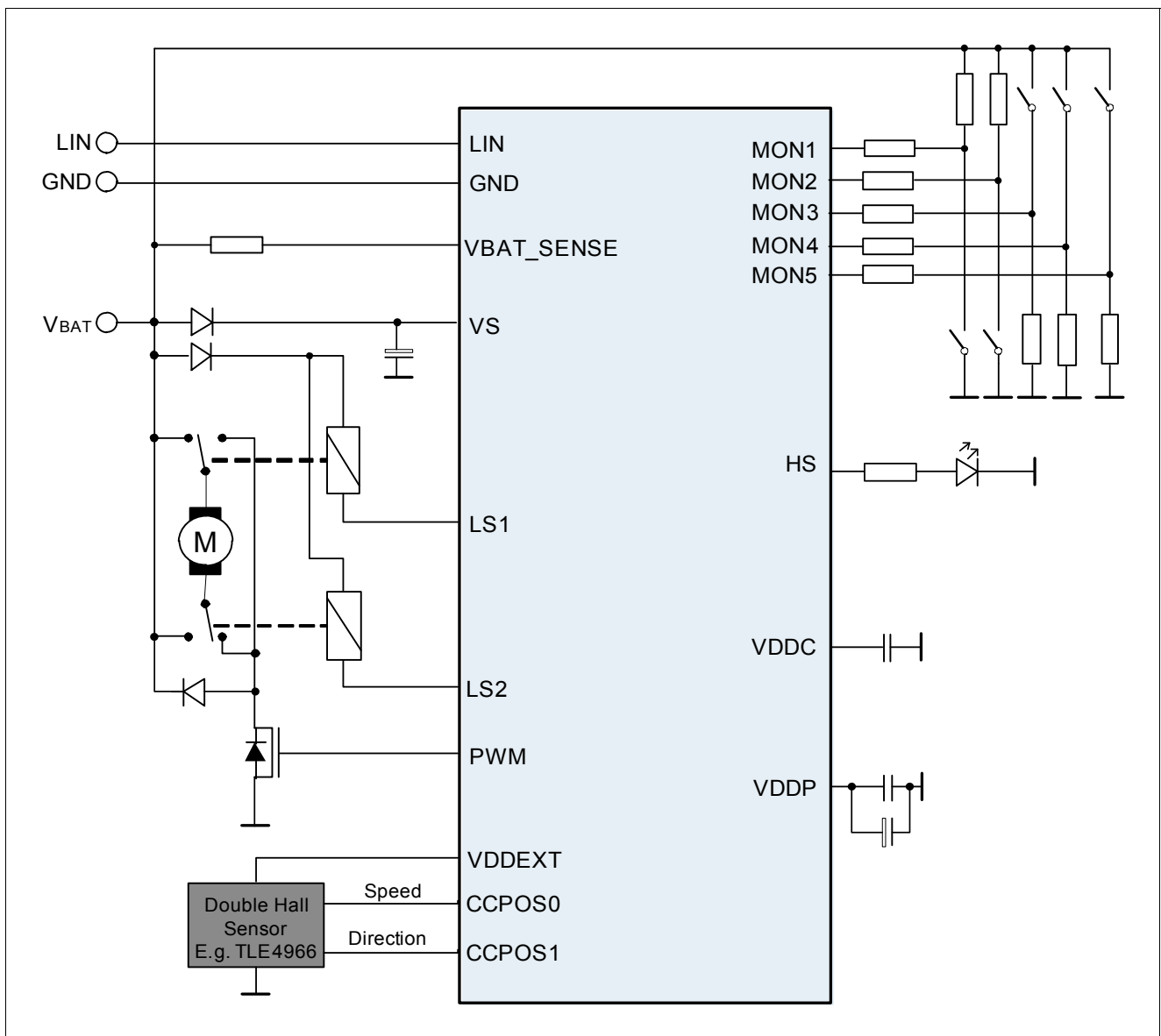


Figure 31 Simplified Application Diagram

5.4 Flash Parameters

This chapter includes the parameters for the 36 kByte embedded flash module.

Table 24 Flash Characteristics ¹⁾

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 Byte page	t_{PR}	–	²⁾ 3	3.5	ms	–	P_5.4.1
Erase time per sector/page	t_{ER}	–	²⁾ 4	4.5	ms	–	P_5.4.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_5.4.3
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_5.4.4

1) Not subject for production test, specified by design

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.

5.7 High-Speed Synchronous Serial Interface

The table below provides the SSC timing in the TLE9832.

Table 29 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	¹⁾ $2 \cdot T_{SSC}$	–	–		–	P_5.7.1
MTSR delay from SCLK	t_1	10	–	–	ns	–	P_5.7.2
MRST setup to SCLK	t_2	10	–	–	ns	–	P_5.7.3
MRST hold from SCLK	t_3	15	–	–	ns	–	P_5.7.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24 \text{ MHz}$, $t_0 = 83.3 \text{ ns}$. T_{CPU} is the CPU clock period.

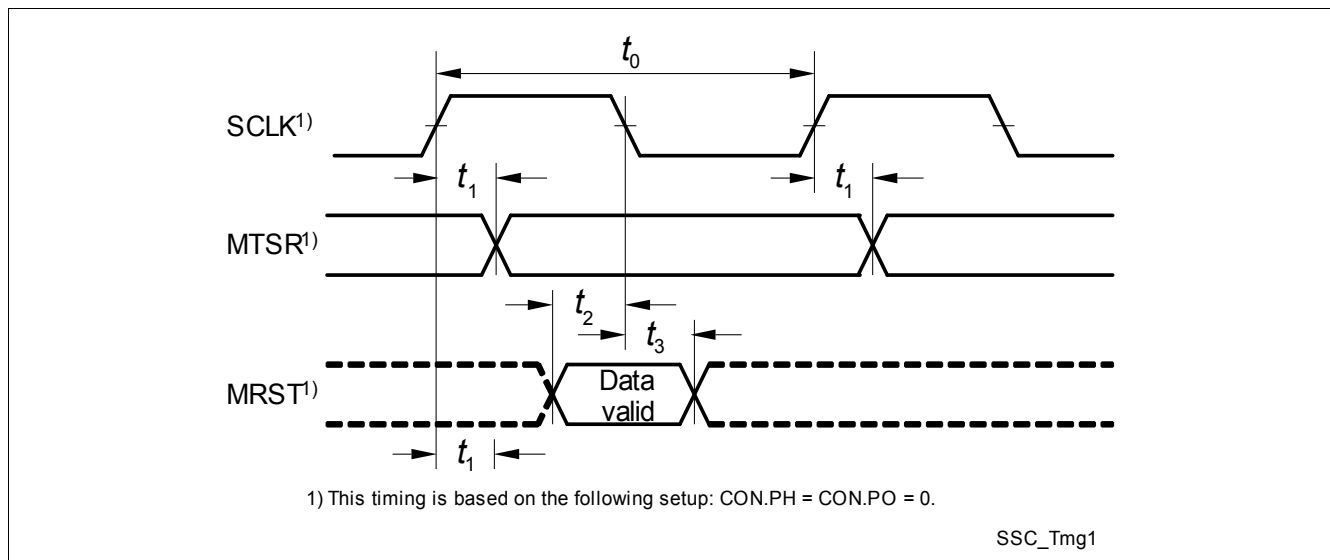


Figure 32 SSC Master Mode Timing

5.8 Measurement Unit

5.8.1 Analog Digital Converter 8-Bit

Table 30 DC Specifications ADC 8 Bit

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resolution	—	—	8	—	Bit	—	P_5.8.1
Offset error	—	-10	4	+10	mV	—	P_5.8.2
Gain single-ended input mode	GSE	—	1	—	—	—	P_5.8.3
Input voltage single-ended mode	V_{ainp}, V_{ainn}	0	—	V_{DD1V5_A}	V	—	P_5.8.4
Gain differential input mode	GDF	—	1.24	—	—	—	P_5.8.5
Common input voltage in differential mode	V_{icm}	0.5	0.6	$V_{DDP}/2 + 0.1$	—	$V_{icm} = (V_{ainp} + V_{ainn})/2$	P_5.8.6
Gain error	—	-5	1.5	+5	%FSR	—	P_5.8.7
Differential nonlinearity (DNL)	—	-1.5	0.5	+1.5	LSB	—	P_5.8.8
Integral Nonlinearity (INL)	—	-3	± 1.5	3	LSB	—	P_5.8.9

5.8.2 Measurement Unit (VBAT_SENSE - Supply Voltage Attenuator)

Table 31 Supply voltage signal conditioning

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Battery Voltage Measurement $V_{\text{BAT_SENSE}}$							
Nominal operating input voltage range ¹⁾	$V_{\text{S/BAT_SENSE}}$	3	–	20	V	Max. value corresponds to typ. ADC full scale input	P_5.8.10
Measurement input resistance	$R_{\text{in,VS/VBAT_SENSE}}$	200	289	380	kΩ	PD_N=1 (on-state)	P_5.8.11
Measurement input leakage current	I_{leak}	0	–	1.0	μA	PD_N=0 (off-state), $V_{\text{BAT_SENSE}}$ =13.5V	P_5.8.12
Overall (calibrated) measurement accuracy after A/D-conversion ²⁾							
$V_{\text{BAT_SENSE}} / V_{\text{s}}$ 8-bit ADC	$\Delta V_{\text{BATADC8B}}$	-250	–	250	mV	V_{s} = 5.5V to 18V, T_{j} = 40..85°C	P_5.8.13
$V_{\text{BAT_SENSE}} / V_{\text{s}}$ 10-bit ADC	$\Delta V_{\text{BATADC10B}}$	-200	–	200	mV	V_{s} = 5.5V to 18V, T_{i} = 40..85°C	P_5.8.14

5.8.4 Temperature Sensor Module

Table 33 Electrical Characteristics Temperature Sensor Module

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Linear temperature range	T_{RANGE}	-40		175	$^\circ\text{C}$	–	P_5.8.21
Output voltage V_{TEMP} at $T_0=273 \text{ K } (0^\circ\text{C})$ Mode 1	a	–	0.4893	–	V	¹⁾ DVBE_MODE=0 $T=273\text{K } (0^\circ\text{C})$	P_5.8.22
Output voltage V_{TEMP} at $T_0=273 \text{ K } (0^\circ\text{C})$ Mode 2	a	–	0.5365	–	V	DVBE_MODE=1 $T_0=273 \text{ K } (0^\circ\text{C})$	P_5.8.23
Temperature sensitivity b in Mode 1	b	–	1.685	–	mV/K	¹⁾ DVBE_MODE=0	P_5.8.24
Temperature sensitivity b Mode 2	b	–	1.834	–	mV/K	DVBE_MODE=1	P_5.8.25
Accuracy_1 ²⁾	Acc_1	-10	–	10	$^\circ\text{C}$	$-40^\circ\text{C} < T_j < 125^\circ\text{C}$	P_5.8.26
Accuracy_2	Acc_2	-15	–	15	$^\circ\text{C}$	$125^\circ\text{C} < T_j < 175^\circ\text{C}$	P_5.8.27

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement

5.11 High Side Switch

5.11.1 Functional Range

Table 38 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	5.5	–	27	V	–	P_5.11.1
Current range for Sleep Mode / Stop Mode	$I_{HS\ max\ sleep_pd}$	–	–	40	mA	Cyclic Sense Mode	P_5.11.2
PWM frequency of HS with Slew Rate Control	$f_{PWM_W_SR}$	0	–	10	kHz	¹⁾ Frequency must be configured in the PWM Generator	P_5.11.3
PWM frequency of HS without Slew Rate Control	f_{PWM_W/O_SR}	0	–	25 ²⁾	kHz	¹⁾ Frequency must be configured in the PWM Generator	P_5.11.4

1) Not subject to production test, specified by design.

2) referring to a 47ohm series resistor to charge an external power mos gate

5.11.2 Electrical Characteristics

Table 39 Electrical Characteristics

$V_S = 5.5\text{ V}$ to 27 V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Maximum ratings							
Output voltage	V_{HSxOUT}	-0.3	–	V_{S}	V	min. value referred to GND_A	P_5.11.5
Output HS							
ON-State Resistance	R_{ON}	–	–	20	Ω	V_{S} =5.5 to 27 V, Ids=100mA, higher resistance below V_{S} =5.5V	P_5.11.6
Output leakage Current	I_{leakage}	–	–	2	μA	Output OFF $0\text{ V} < V_{\text{XLO}} < V_{\text{S}}$; $T_{\text{j}} < 85\text{ }^{\circ}\text{C}$	P_5.11.7
Output Slew Rate (rising) with Slew Rate Control	$SR_{\text{raise_w_SR}}$	1	–	10	V/ μs	10% to 90% of V_{S} V_{S} = 9 to 18V R_{L} =300 Ω ¹⁾	P_5.11.8

5.12 Low Side Switches

5.12.1 Functional Range

Table 40 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	5.5	–	27	V	–	P_5.12.1
PWM Frequency of LS	f_{PWM}	–	–	25 ¹⁾	kHz	2)	P_5.12.2

1) referring to a 47ohm series resistor to charge an external power mos gate

2) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.12.2 Electrical Characteristics

Table 41 Electrical Characteristics

$V_S = 5.5\text{ V}$ to 27 V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent Limitation	I_{LSTyp}	175	250	325	mA		P_5.12.3
ON-State Resistance 150°C	R_{ON}	–	–	10	Ω	$V_S > 5.5\text{ V}$, $I_{\text{ds}} = 100\text{mA}$, $T_j = 150^\circ\text{C}$	P_5.12.4
ON-State Resistance 25°C		–	4	–	Ω	$T_j = 25^\circ\text{C}$	P_5.12.5
Leakage Current	I_{leakage}	–	–	2	μA	$0\text{ V} < V_{\text{LS}} < V_S$; $T_j < 85^\circ\text{C}$	P_5.12.6
Turn ON Delay time, slow mode	$t_{\text{dOn-LS}}$	–	–	50	μs	¹⁾ LS_ON=1 to 0.9*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$	P_5.12.7
Turn ON Delay time, PWM mode	$t_{\text{dOn,f-LS}}$	–	–	0.5	μs	LS_ON=1 to 0.9*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$	P_5.12.8
Turn ON fall time, PWM mode	$t_{\text{ONF,PWM}}$	–	1	1.25	μs	$V_{\text{LS}} 0.9\text{Vs}$ to 0.1Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$	P_5.12.9
Turn ON fall time, slow mode	$t_{\text{ONF,Slow}}$	–	100	150	μs	¹⁾ VLS 0.9*Vs to 0.1*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$	P_5.12.10
Turn OFF Delay time, slow mode	$t_{\text{dOff-LS}}$	–	–	50	μs	¹⁾ LS_ON=0 to 0.1*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$	P_5.12.11

6 Package Outlines

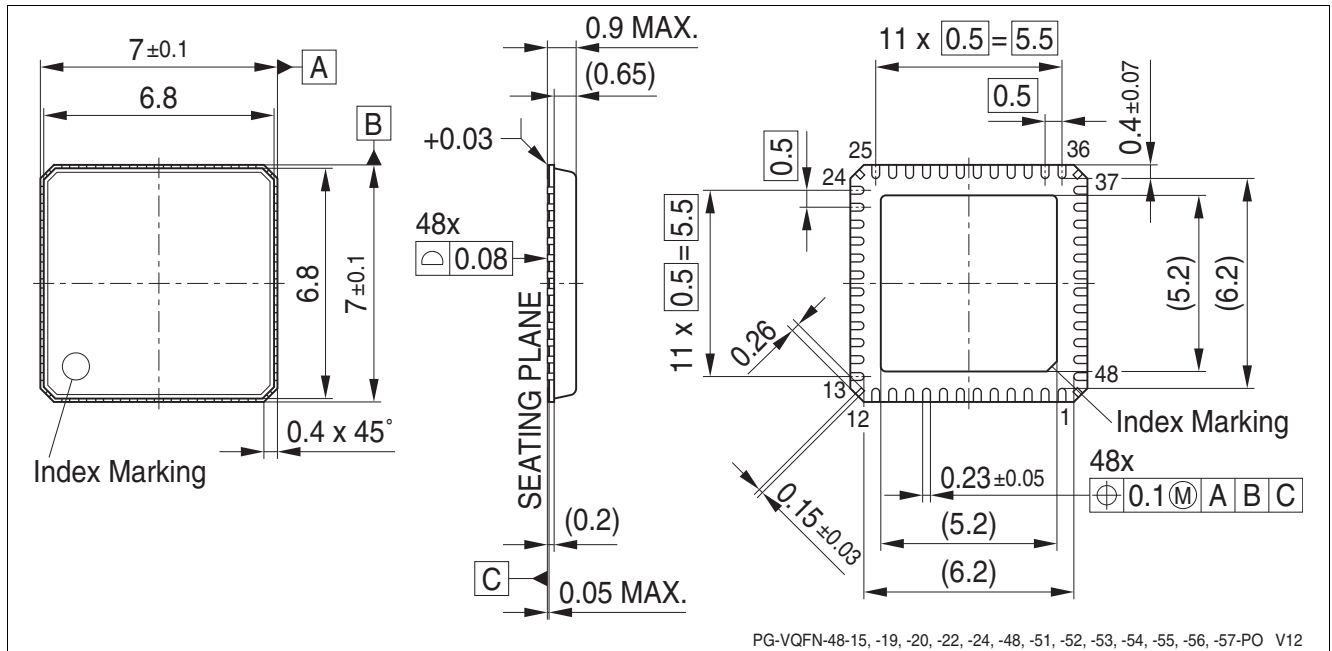


Figure 33 Package outline TLE9832QV, VQFN-48-22

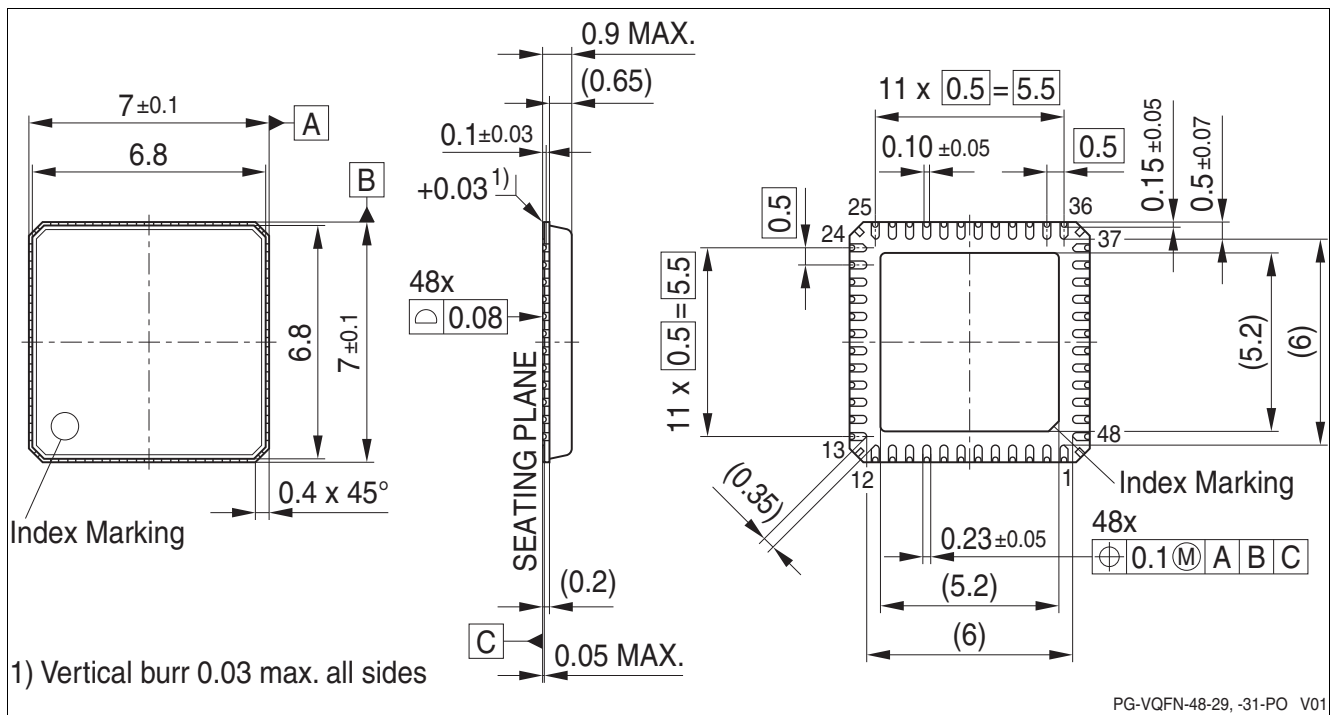


Figure 34 Package outline TLE9832QX, VQFN-48-29

Notes

1. You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products":
<http://www.infineon.com/products>.
2. Dimensions in mm.