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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	-
Core Processor	-
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	-
Number of I/O	-
Voltage - Supply	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9832qxxuma3

1 Summary of Features

- High performance XC800 core
  - compatible to standard 8051 core
  - up to 40 MHz clock frequency
  - two clocks per machine cycle architecture
  - two data pointers
- On-chip memory
  - 32 kByte + 4 kByte Flash for program code and data (4 kByte EEPROM emulation built-in)
  - 512 Byte One Time Programmable Memory (OTP)
  - 512 Byte 100 Time Programmable Memory (100TP)
  - 256 Byte RAM, 3 kByte XRAM
  - BootROM for startup firmware and Flash routines
- Core logic supply at 1.5 V
- On-chip OSC and PLL for clock generation
  - Loss of clock detection with fail safe mode for power switches
- Watchdog timer (WDT) with programmable window feature for refresh operation and warning prior to overflow
- General-purpose I/O Port (GPIO) with wake-up capability
- Multiplication/division unit (MDU) for arithmetic calculation
- Software libraries to support floating point and MDU calculations
- Five 16-Bit timers - Timer 0, Timer 1, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6) with Timer 12 and Timer 13
- Full duplex serial interface (UART) with LIN support
- Synchronous serial channel (SSC)
- On-chip debug support via 2-wire Device Access Port (DAP)
- LIN Bootstrap loader (LIN BSL)
- LIN transceiver compliant to LIN 1.3, LIN 2.0 and LIN 2.1
- 2 x Low Side Switches with clamping capability incl. PWM functionality, e.g. as relay driver
- 1x High Side Switch with cyclic sense option and PWM functionality, e.g. for LED or powering of switches
- 5 x High Voltage Monitor Input pins for wake-up and with cyclic sense and analog measurement option
- Measurement unit with 10 channels, 8-Bit A/D Converter (ADC2) and data post processing
- 8 channels, 10-Bit A/D Converter (including battery voltage and supply voltage measurement) (ADC1)
- Single power supply from 3.0 V to 27 V
- Low-dropout voltage regulators (LDO)
- Dedicated 5 V voltage regulator for external loads (e.g. hall sensor)
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down mode
  - Stop Mode
  - Sleep Mode
  - Cyclic wake-up and cyclic sense during Stop Mode and Sleep Mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Overcurrent protection with shutdown
- Supported by a full range of development tools including C compilers, macro assembler packages, emulators, evaluation boards, HLL debugger, programming tools, software packages
- Temperature Range T_J: -40 °C up to 150 °C
- Packages TLE9832QV: VQFN-48-22 and TLE9832QX: VQFN-48-29
- Green package (RoHS compliant)

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832 device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9832QV	40 MHz	1	5	36 kByte	11	no
TLE9832QX	40 MHz	1	5	36 kByte	11	no

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P2.3	36	I	I	AN3 CCPOS1_0 EXINT0_2 CTRAP_1 CC60_1	ADC1 analog input channel 3 CCU6 hall input 1 External interrupt input 0 CCU6 trap input CCU6 capture/compare channel 0 input
P2.4	32	I	I	AN4 T0_2	ADC1 analog input channel 4 Timer 0 input
P2.5	31	I	I	AN5 T1_2	ADC1 analog input channel 5 Timer 1 input
P2.7	35	I	I	AN7 CCPOS2_0 EXINT2_0 T13HR_1 CC62_1	ADC1 analog input channel 7 CCU6 hall input 2 External interrupt input 2 CCU6 timer 13 hardware run input CCU6 capture/compare channel 2 input
Power Supply					
VS	47	P	–	Battery supply input	
VDDP	44	P	–	I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors.	
VDDC	42	P	–	Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor.	
VDDEXT	45	P	–	External voltage supply output (5.0 V, 20 mA)	
LSGND	13	P	–	Low Side ground LS1, LS2	
GND	30, 43, 19, 38	P	–	Core supply ground; analog supply ground	
ADCGND	33	P	–	Analog supply ground for ADC1	
LINGND	2	P	–	LIN ground	
Monitor Inputs					
MON1	5	I	I	High Voltage Monitor Input 1	
MON2	6	I	I	High Voltage Monitor Input 2	
MON3	7	I	I	High Voltage Monitor Input 3	
MON4	8	I	I	High Voltage Monitor Input 4	
MON5	9	I	I	High Voltage Monitor Input 5	
High Side Switch / Low Side Switch Outputs					
LS1	11	O	Hi-Z	Low Side Switch output 1	
LS2	12	O	Hi-Z	Low Side Switch output 2	
HS1	3	O	Hi-Z	High Side Switch output 1	
LIN Interface					
LIN	1	I/O	PU	LIN bus interface input/output	
Others					

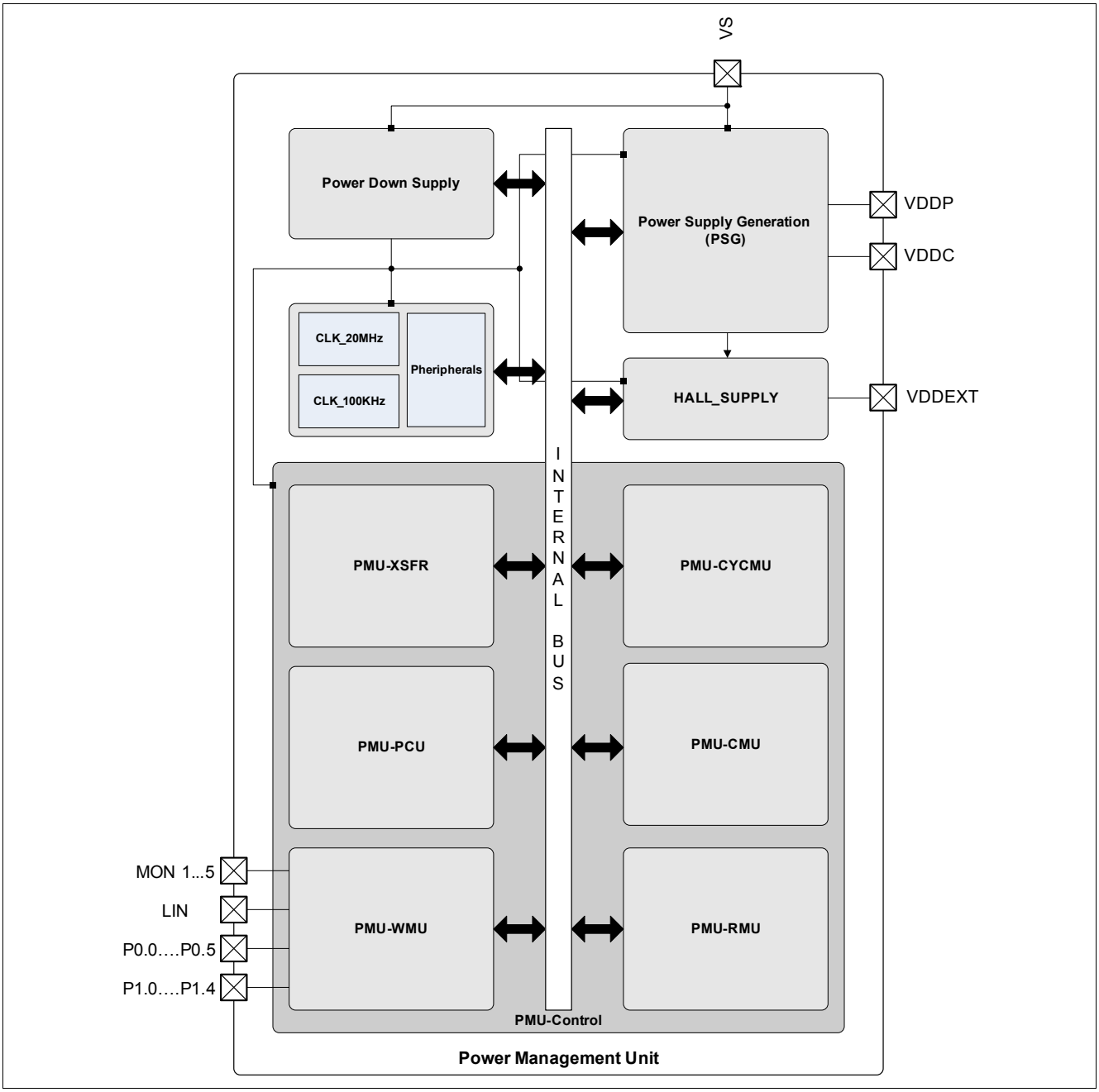

Figure 5 Power Management Unit Block Diagram

3.1.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which serves as pad supply for the parallel port pins and other 5 V analog functions.

Features

- 5 V low-drop voltage regulator
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Preregulator for VDDC regulator
- GPIO supply
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

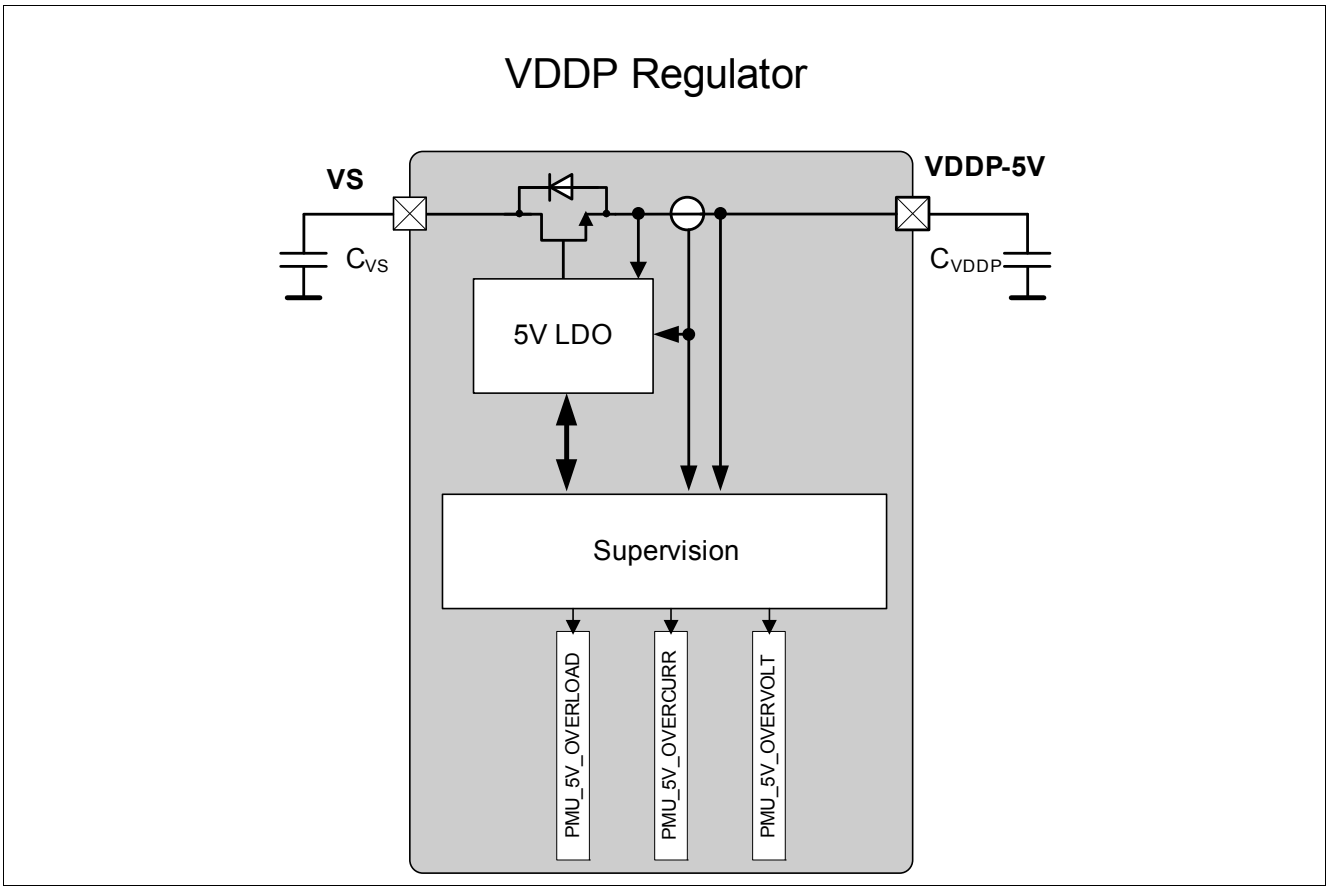

Figure 6 Module Block Diagram of VDDP Voltage Regulator

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

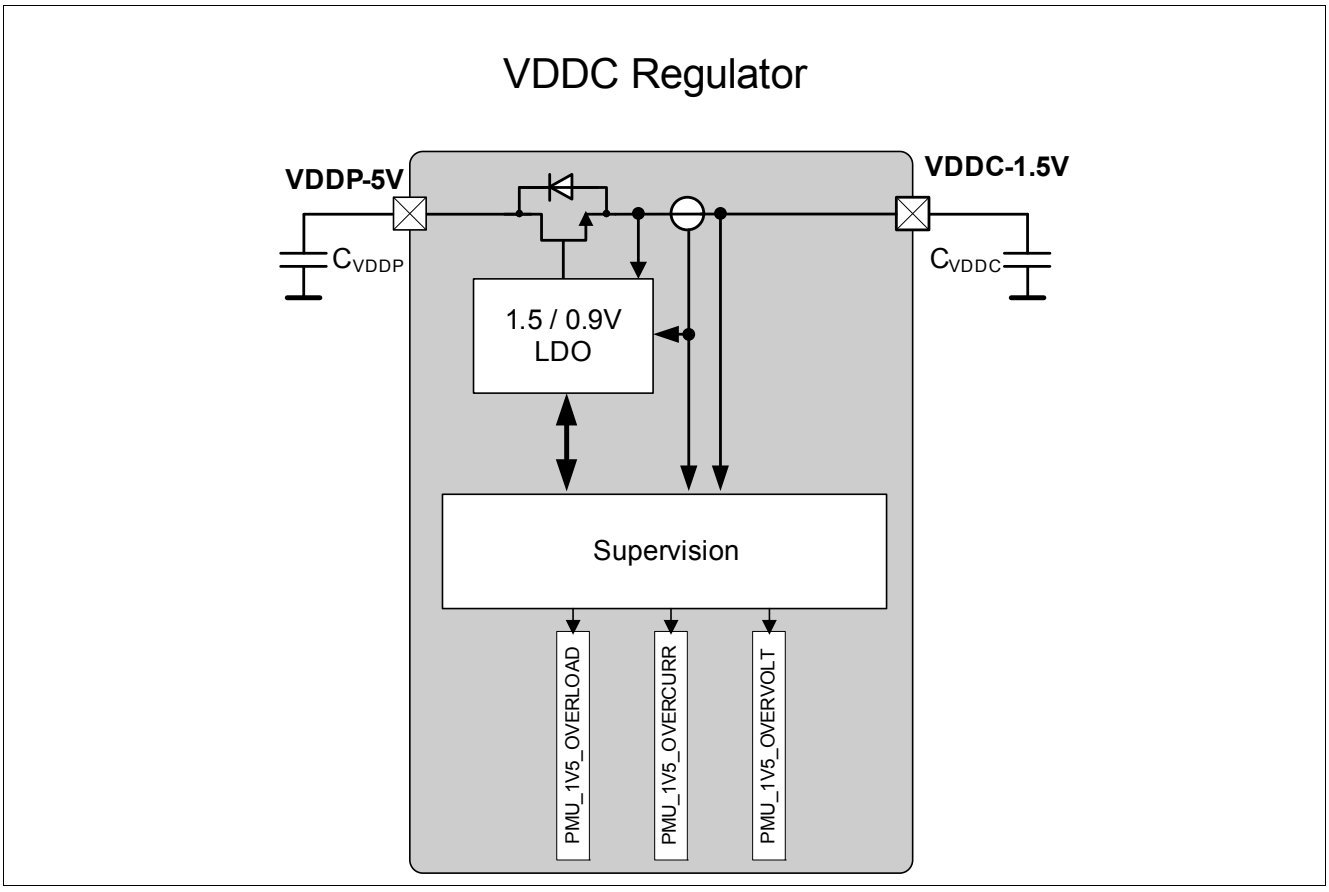

Figure 7 Module Block Diagram of VDDC Voltage Regulator

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

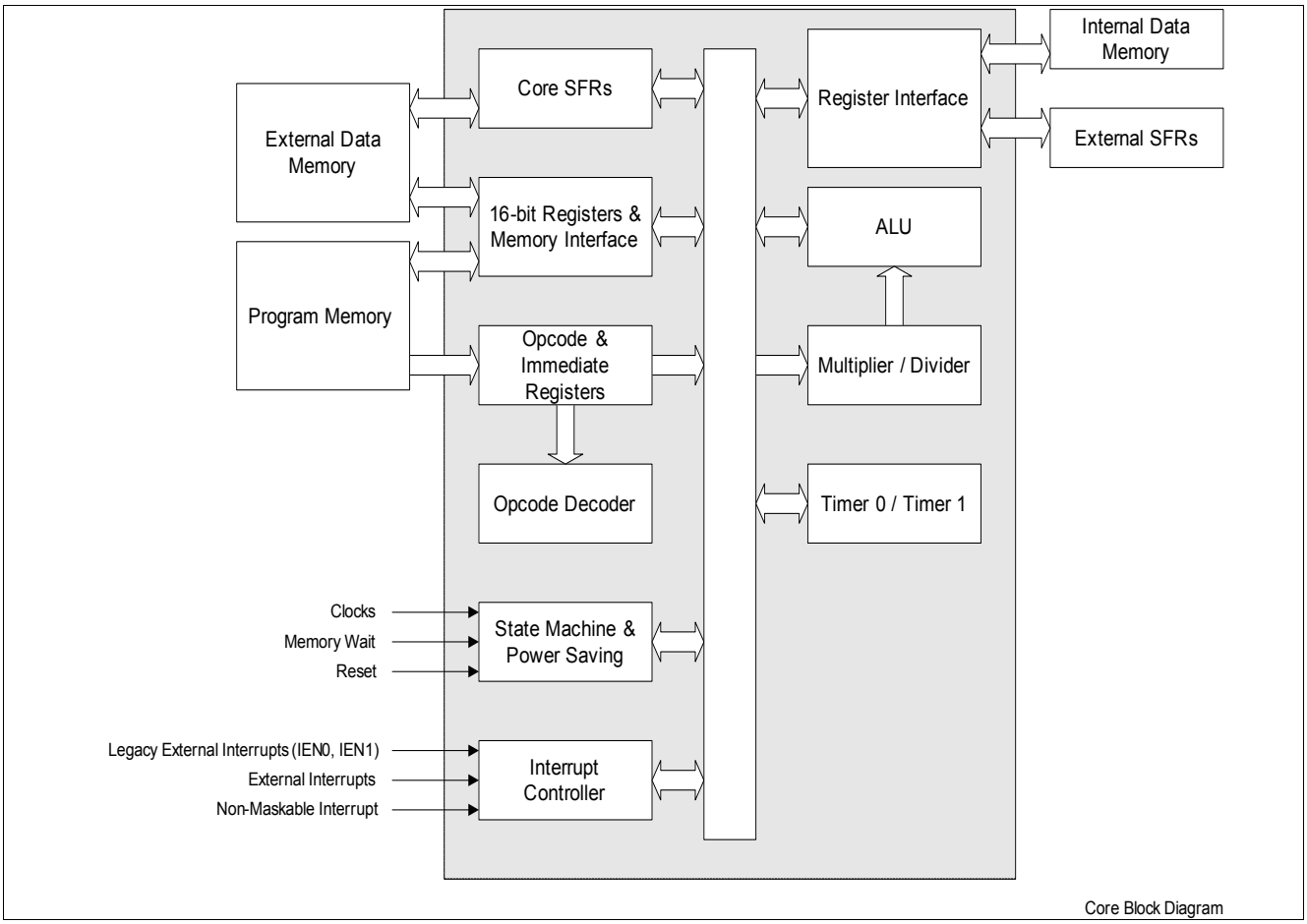

Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

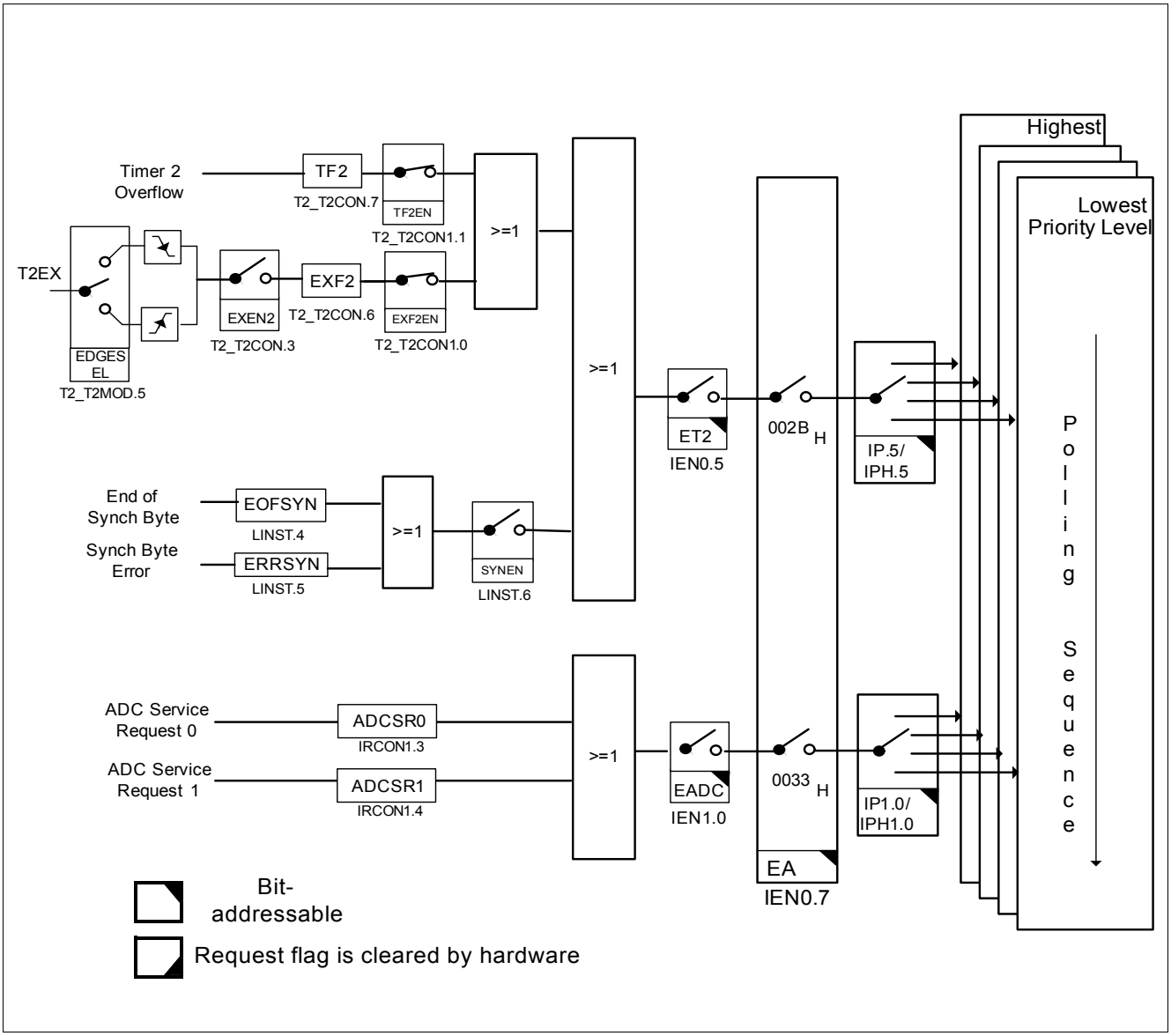

Figure 15 Interrupt Request Sources (Part 2)

  - Programmable number of data Bits: 2 to 8 Bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

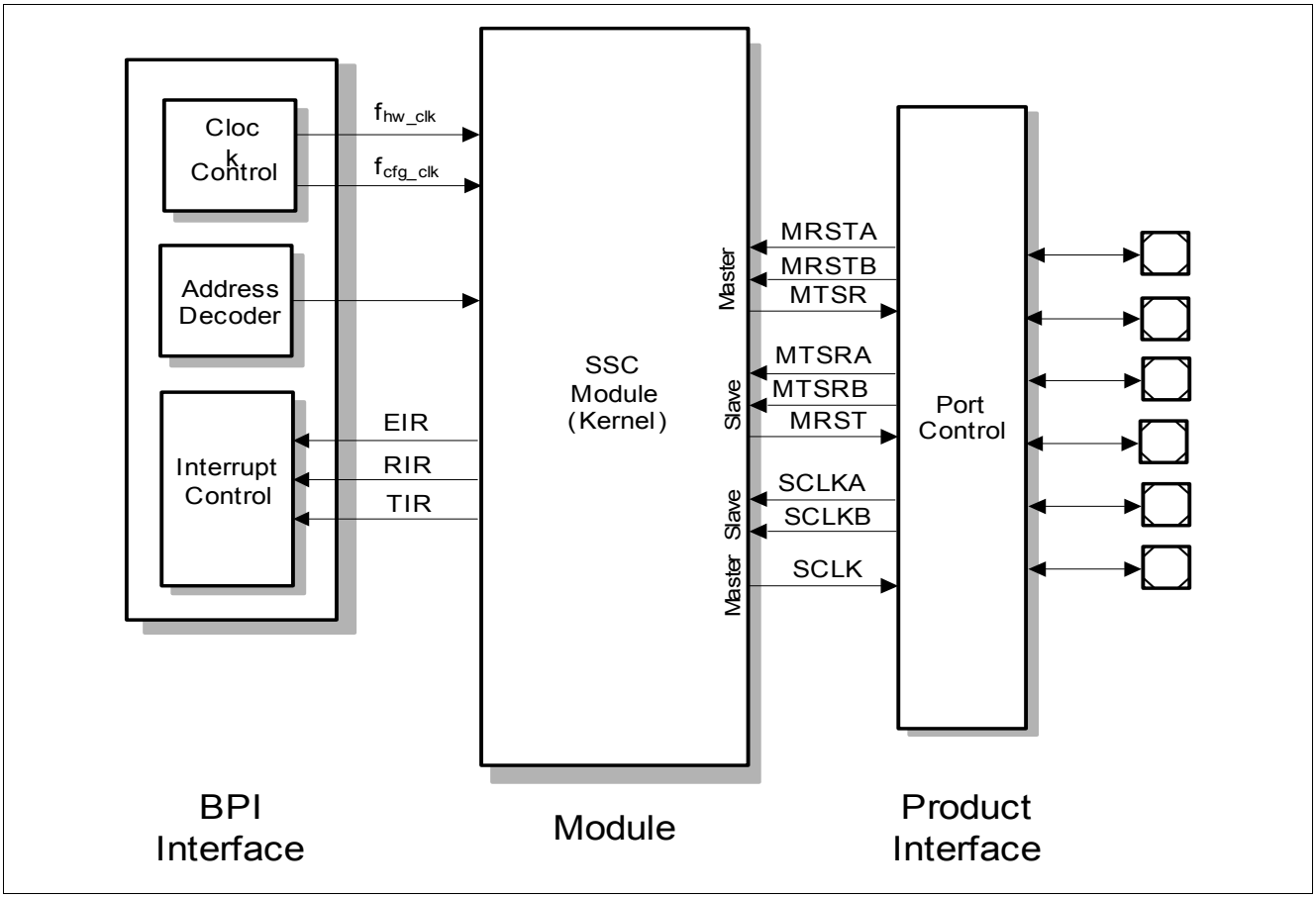

Figure 24 SSC Interface Diagram

3.18 Measurement Unit

The measurement unit is a functional unit that comprises the following associated sub-modules:

- 1 x 8 Bit ADC (ADC2) with 10 inputs. 5 are for single ended input signals and 5 are for differential input signals.
- Monitoring inputs voltage attenuators with two selectable attenuation settings: divide by 4 and divide by 6
- Supply voltage attenuators with attenuation of VBAT_SENSE, VS, VDDP and VDDC.
- VBG monitoring of 8-Bit ADC (ADC2) to guarantee functional safety requirements.
- Low Side Switch current sensing of LS1 and LS2. Allows a scalable overcurrent pre warning.
- Temperature sensor for monitoring the chip temperature and Low Side Switches temperature.
- Supplement block with reference voltage generation, bias current generation, voltage buffer for Flash reference voltage, voltage buffer for analog module reference voltage and test interface.

Table 10 Measurement functions and associated modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-Bit ADC. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the Flash module
8-Bit ADC (ADC2)	8-Bit ADC module with 10 multiplexed inputs	1. 5 single-ended inputs 0 ... 1.23V 2. 5 differential inputs 0 ... 1.23V (allocation see following overview figure)
10-Bit ADC (ADC1)	10-Bit ADC module including analog test bus interface - part of µC subsystem	1. VBAT_SENSE measurement on channel 0 of ADC1. 2. VS measurement on channel 2 of ADC1. 3. MONx measurement on channel 6 of ADC1. 4. 5 additional (5V) analog inputs from Port 2.
Supply Voltage Attenuator	Resistive supply voltage attenuator	Scales down the supply voltages of the system to the input voltage range of ADC1 and ADC2.
Monitoring Input Attenuator	Resistive attenuator for (HV)	Scales down 5 monitoring input voltages to the input voltage range of the ADC1.
Central Temperature - Low Side Switch Temperature Sensor	Temperature sensor readout with two multiplexed ΔV_{be} sensing elements	Generates outputs voltage which is a linear function of the local chip (junction) temperature.
Measurement Core Module	Digital signal processing and ADC control unit	1. Generates the control signal for the 8-Bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

The structure of the measurement functions module is shown in **Figure 29**.

3.21 High Voltage Monitor Input

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at each high-voltage MON_IN pin in low-power mode. Each input is sensitive to an input level monitoring. It is available when the module is switched to Active Mode via the MON_int (internal signal name) output with a small filter delay of typical 2 µs.

Features

- High-voltage input with V_S/2 threshold voltage
- Edge sensitive wake capability for power saving modes
- Level sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC1 in Active Mode, using adjustable threshold values (see also **Chapter 3.20**).

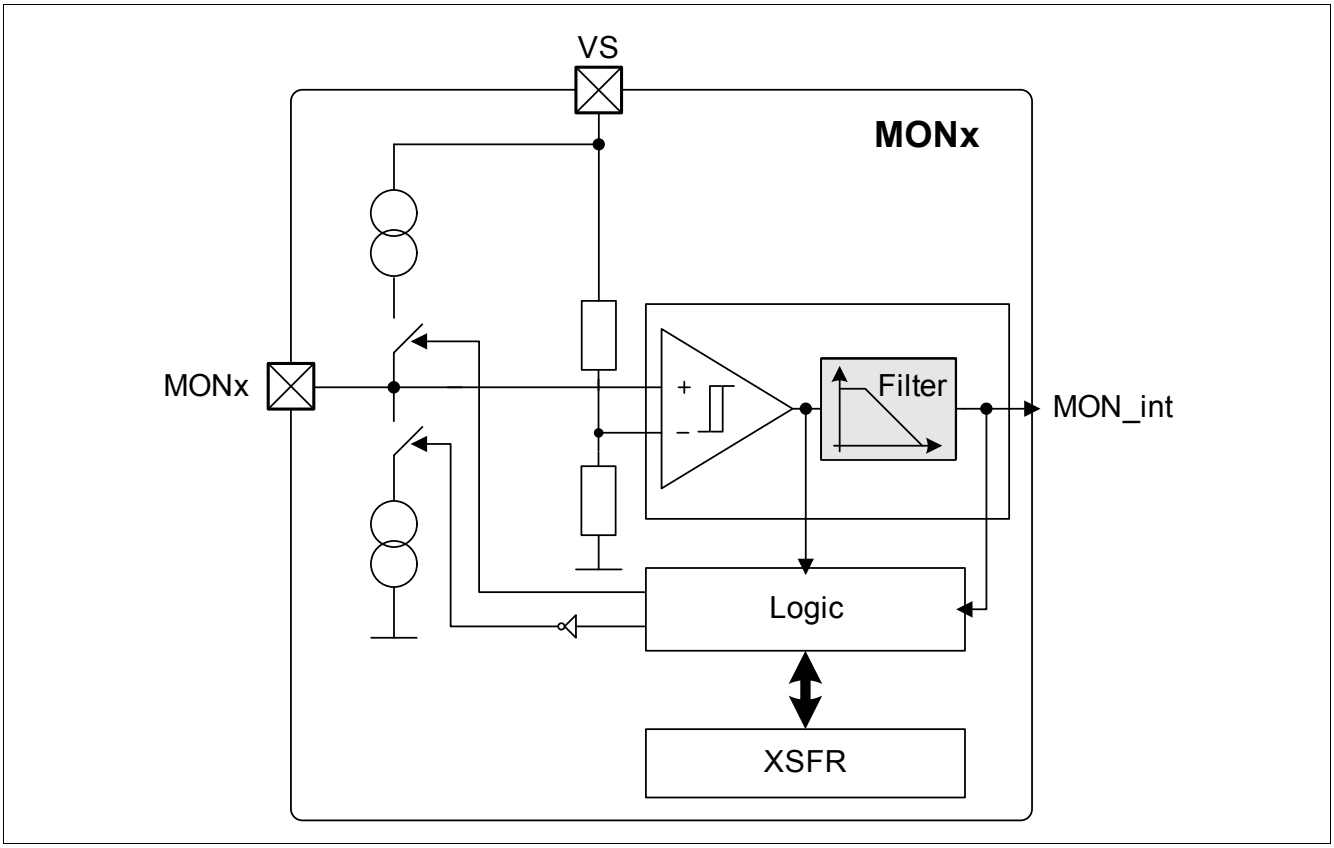

Figure 27 Monitoring Input Block Diagram

3.24 PWM Generator

The PWM generator provides up to two configurable PWM channels in order to drive the Low Side Switches LS1, LS2 and the High Side Switch HS1 in a PWM mode.

Features

- Programmable modulation frequency per channel
- Programmable duty-cycle per channel with glitch-free reprogramming
- PWM frequency up to 25 kHz
- Duty-cycle resolution from 0 % ... 100 % in steps of 0.5 %

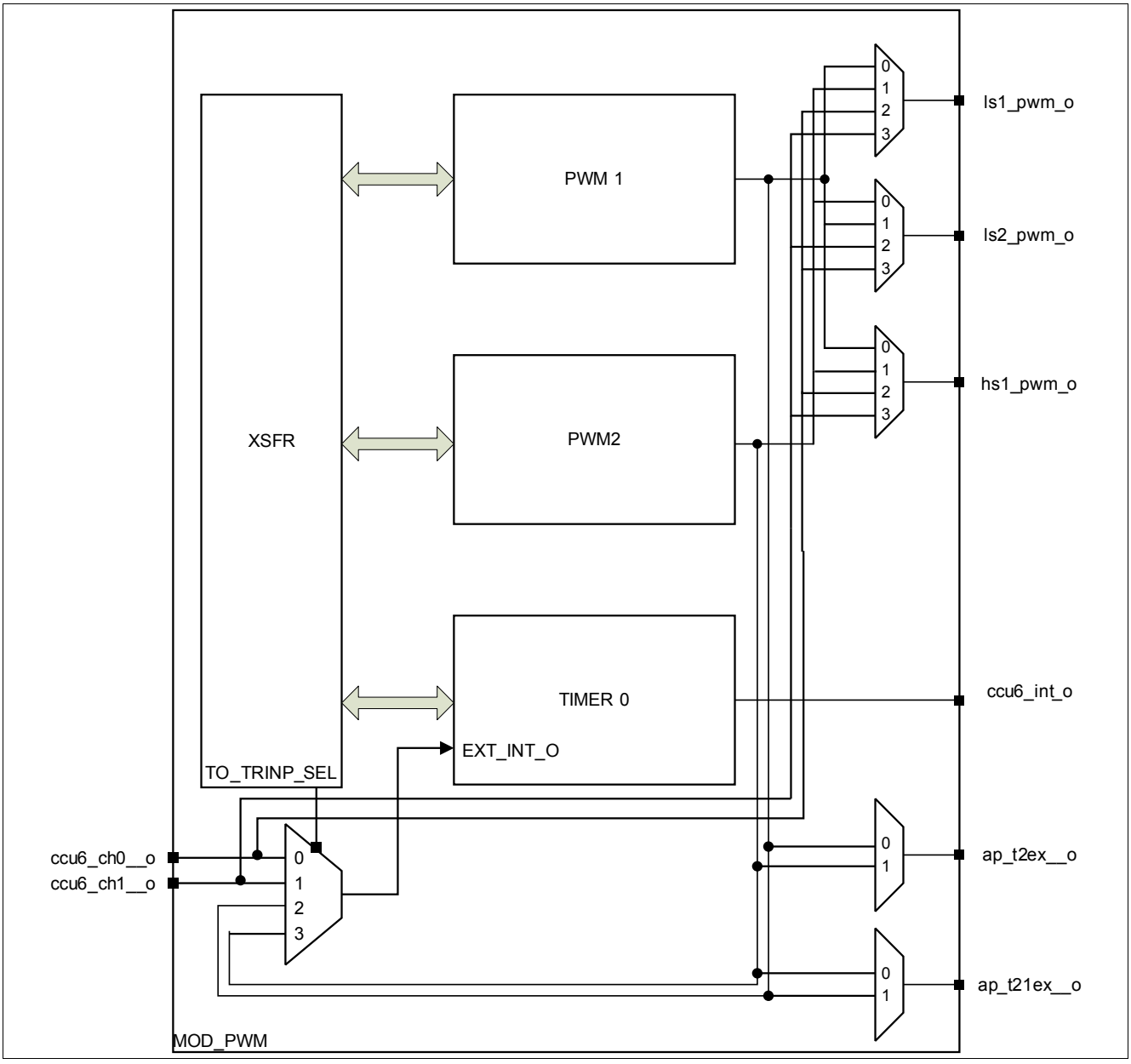

Figure 30 Module Block diagram of PWM module and included PWM switching matrix

5.4 Flash Parameters

This chapter includes the parameters for the 36 kByte embedded flash module.

Table 24 Flash Characteristics [1)]

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 Byte page	t_{PR}	–	[2)]3	3.5	ms	–	P_5.4.1
Erase time per sector/page	t_{ER}	–	[2)]4	4.5	ms	–	P_5.4.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_5.4.3
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_5.4.4

1) Not subject for production test, specified by design

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.

5.5 Parallel Ports (GPIO)

5.5.1 Functional Range

Table 25 Functional Range

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output current on any pin	I_{OH} , I_{OL}	–	–	20	mA	1) 2)	P_5.5.1
Max output current for all GPIOs	I_{max}	–	–	60	mA	1) 2)	P_5.5.2

1) One of these limits must be kept.

2) Not subject to production test, specified by design

5.5.2 DC Parameters

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage (all except XTAL1)	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	–	P_5.5.3
Input high voltage (all except XTAL1)	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	–	P_5.5.4
Input Hysteresis[1)]	HYS	0.11 x V_{DDP}	–	–	V	Series resistance = 0 Ω	P_5.5.5
Output low voltage	V_{OL}	–	–	1.0	V	2) $I_{OL} \le I_{OLmax}$	P_5.5.6
Output low voltage	V_{OL}	–	–	0.4	V	2) $I_{OL} \le$ 3) I_{OLnom}	P_5.5.7
Output high voltage[4)]	V_{OH}	V_{DDP} - 1.0	–	–	V	2) $I_{OH} \ge I_{OHmax}$	P_5.5.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	2)3) $I_{OH} \ge I_{OHnom}$	P_5.5.9
Input leakage current (Port 2)	I_{OZ1}	-400	–	+400	nA	$T_J \le 85°C$, 0 V < V_{IN} < V_{DDP}	P_5.5.10
Input leakage current (all other)[5)]	I_{OZ2}	-5	–	+5	µA	$T_J \le 85°C$, 0.45 V < V_{IN} < V_{DDP}	P_5.5.11

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current (all other)	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.5.12
Pull level keep current	I_{PLK}	-240	–	+240	µA	6) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.5.13
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	6) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.5.14
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	–	P_5.5.15

1) Not subject to production test, specified by design.

2) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

3) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). However, only the levels for nominal output currents are verified.

4) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

5) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (ΔV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × ΔV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

6) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IH} for a pull-up; V_{PIN} ≤ V_{IL} for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{IL} for a pull-up; V_{PIN}≥ V_{IH} for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10,4 kBit/s)	t_{duty1}	0.417	–	–		[7] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 29)	P_5.6.24
Duty cycle D4 (for worst case at 10,4 kBit/s)	t_{duty2}	–	–	0.590		duty cycle 4 TH_{Rec}(max) = 0.389 × V_S; TH_{Dom}(max) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 30)	P_5.6.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	–	P_5.6.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	–	P_5.6.27
Receiver delay symmetry	$t_{sym,R}$	-1	–	1	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_5.6.28
Duty cycle D5 (for worst case at 40 kBit/s)	t_{duty1}	0.395	–	–		[6] duty cycle 5 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};	P_5.6.29
Duty cycle D6 (for worst case at 40 kBit/s)	t_{duty2}	–	–	0.581		[6] duty cycle 6 TH_{Rec}(max)= 0.422 × V_S; TH_{Dom}(max)= 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)	P_5.6.30
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	0.5	6	µs	–	P_5.6.31

Table 31 Supply voltage signal conditioning

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
V_{DD5_SENSE}	ΔV_{DDP_SENSE}	-150	–	150	mV	–	P_5.8.15
V_{DD1V5_SENSE}	ΔV_{DDC_SENSE}	-45	–	45	mV	–	P_5.8.16

1) This parameter is not subject to production test

2) The device is calibrated based on an external 1kΩ resistor

5.8.3 Measurement Functions Monitoring Input Voltage Attenuator

Table 32 Monitoring input voltage attenuation

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power Supply							
Input resistance[1)]	R_{IN}	300	400	500	kΩ	PD_N=1 (on-state) V_{MON_X}=0 to 18V if VMON_SEN_SEL_INRANGE = 0	P_5.8.17
Input resistance	R_{IN}	250	–	–	kΩ	V_{MON_X} =0 to 28V if VMON_SEN_SEL_INRANGE = 1 >200 kΩ under all other conditions	P_5.8.18
Timing Characteristics							
Analog Multiplexer Settling Time	$T_{MUXsettle}$	–	–	30	µs	This time frame is valid from writing the corresponding selection register to proper settling of the voltage at channel 7 of the 10-Bit ADC	P_5.8.19
Overall (calibrated) measurement accuracy after A/D-conversion							
V_{MONx} 10-bit ADC	$\Delta V_{MONxADC10B}$	-200	–	200	mV	V_s=5.5V to 18V, T_j = 40..85°C	P_5.8.20

1) Not subject to production test, specified by design.

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis	$I_{OLONhys}$	1	–	4	mA	[1] OL_EN = 1; HS_ON = 1	P_5.11.26
Off-state open load detection							
Open load voltage threshold	V_{OLth1}	0.5* V_S	0.67 *V_S	0.85* V_S	V	I_{OL_test}; open load activated; OLTH_SEL = 1	P_5.11.27
Hysteresis	V_{OLhys}	0.1* V_S	–	0.3* V_S	V	IOL_SEL = 1	P_5.11.28
Open load output current	I_{OL_test}	-150	–	-25	µA	IOL_SEL = 0	P_5.11.29
Open load output current	I_{OL_test}	-1.5	–	-0.5	mA	IOL_SEL = 1	P_5.11.30
Cyclic sense mode							
ON-State Resistance	$R_{ON,static}$	–	–	40	Ω	Definition: differential resistance or resistance at 40 mA	P_5.11.31
Output Slew Rate (rising)	SR_{rise} [1]	1	–	–	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω [1]	P_5.11.32
Output Slew Rate (falling)	SR_{fall} [1]	–	–	-1	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω	P_5.11.33
Delay Time CYCLIC_ON-HS	t_{IN-CYC}	–	–	2	µs	ON =1 to 10% of V_S RL=300Ω	P_5.11.34
Turn-ON time	t_{ON}	–	–	15	µs	V_S =13.5V ON=1 to 90% R_L =300Ω	P_5.11.35
Turn-OFF time	t_{OFF}	–	–	15	µs	V_S =13.5V ON=0 to 10% of V_S R_L =300Ω; T_j=25°C	P_5.11.36

1) Not subject to production test, specified by design.

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