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Details	
Product Status	Not For New Designs
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Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	149
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BFQFP
Supplier Device Package	256-QFP (40x28)
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- Bit 5—Counter Start 4 (STR4): Starts and stops free-running counter 4 (TCNT4).

Bit 5: STR4	Description	
0	TCNT4 is halted	(Initial value)
1	TCNT4 counts	

- Bit 4—Counter Start 3 (STR3): Starts and stops free-running counter 3 (TCNT3).

Bit 4: STR3	Description	
0	TCNT3 is halted	(Initial value)
1	TCNT3 counts	

- Bit 3—Counter Start 1B, 2B (STR1B, STR2B): Starts and stops free-running counters 1B and 2B (TCNT1B, TCNT2B).

Bit 3: STR1B, STR2B	Description	
0	TCNT1B and TCNT2B are halted	(Initial value)
1	TCNT1B and TCNT2B count	

- Bit 2—Counter Start 2A (STR2A): Starts and stops free-running counter 2A (TCNT2A).

Bit 2: STR2A	Description	
0	TCNT2A is halted	(Initial value)
1	TCNT2A counts	

- Bit 1—Counter Start 1A (STR1A): Starts and stops free-running counter 1A (TCNT1A).

Bit 1: STR1A	Description	
0	TCNT1A is halted	(Initial value)
1	TCNT1A counts	

- Bit 0—Counter Start 0 (STR0): Starts and stops free-running counter 0 (TCNT0).

Bit 0: STR0	Description	
0	TCNT0 is halted	(Initial value)
1	TCNT0 counts	

- Bit 7—Reserved: This bit is always read as 0. The write value should always be 0.
- Bits 6 to 4—I/O Control 2B2 to 2B0, 2D2 to 2D0, 2F2 to 2F0, 2H2 to 2H0 (IO2B2 to IO2B0, IO2D2 to IO2D0, IO2F2 to IO2F0, IO2H2 to IO2H0): These bits select the general register (GR) function.

Bit 6: IO2x2	Bit 5: IO2x1	Bit 4: IO2x0	Description	
0	0	0	GR is an output compare register	Compare-match disabled; pin output undefined (Initial value)
		1		0 output on GR compare-match
	1	0		1 output on GR compare-match
		1		Toggle output on GR compare-match
1	0	0	GR is an input capture register	Input capture disabled
		1		Input capture in GR on rising edge at TIO2x pin (GR cannot be written to)
	1	0		Input capture in GR on falling edge at TIO2x pin (GR cannot be written to)
		1		Input capture in GR on both rising and falling edges at TIO2x pin (GR cannot be written to)

x = B, D, F, or H

- Bit 6—Count-Up/Count-Down Flag 6C (UD6C): Status flag that indicates the TCNT6C count operation.

Bit 6: UD6C	Description
0	Free-running counter TCNT6C operates as an up-counter
1	Free-running counter TCNT6C operates as a down-counter

- Bit 5—Count-Up/Count-Down Flag 6B (UD6B): Status flag that indicates the TCNT6B count operation.

Bit 5: UD6B	Description
0	Free-running counter TCNT6B operates as an up-counter
1	Free-running counter TCNT6B operates as a down-counter

- Bit 4—Count-Up/Count-Down Flag 6A (UD6A): Status flag that indicates the TCNT6A count operation.

Bit 4: UD6A	Description
0	Free-running counter TCNT6A operates as an up-counter
1	Free-running counter TCNT6A operates as a down-counter

- Bit 3—Cycle Register Compare-Match Flag 6D/7D (CMF6D/CMF7D): Status flag that indicates CYLRxD compare-match.

Bit 3: CMFxD	Description
0	[Clearing condition] (Initial value) When CMFxD is read while set to 1, then 0 is written to CMFxD
1	[Setting conditions] • When TCNTxD = CYLRxD (in non-complementary PWM mode) • When TCNT6D = H'0000 in a down-count (in complementary PWM mode)

x = 6 or 7

Input Capture Register 10AH, AL (ICR10AH, ICR10AL): Input capture register 10AH, AL (comprising ICR10AH and ICR10AL) is a 32-bit read-only register to which the TCNT10AH, AL value is transferred on external input (TI10) (AGCK). At the same time, ICF10A in timer status register 10 (TSR10) is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ICR10A is initialized to H'00000000 by a power-on reset, and in hardware standby mode and software standby mode.

Output Compare Register 10AH, AL (OCR10AH, OCR10AL): Output compare register 10AH, AL (comprising OCR10AH and OCR10AL) is a 32-bit readable/writable register that is constantly compared with free-running counter 10AH, AL (TCNT10AH, TCNT10AL). When both values match, CMF10A in timer status register 10 (TSR10) is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCR10A is initialized to H'FFFFFFFF by a power-on reset, and in hardware standby mode and software standby mode.

after setting H'FFFF in the cycle register, the cycle register's compare-match flag and overflow flag will be set simultaneously.

Note that 0% or 100% duty output is not possible in channel 3 to 5 PWM mode.

An example of channel 3 to 5 PWM mode operation is shown in figure 11.23.

In the example in figure 11.23, H'0008 is set in GR3D, H'0002 is set in GR3A, GR3B, and GR3C, and channel 3 is activated; then, during operation, H'0000 is set in GR3A, GR3B, and GR3C, and output is performed to external pins TIOA3 to TIOC3. Note that 0% duty output is not possible even though H'0000 is set.

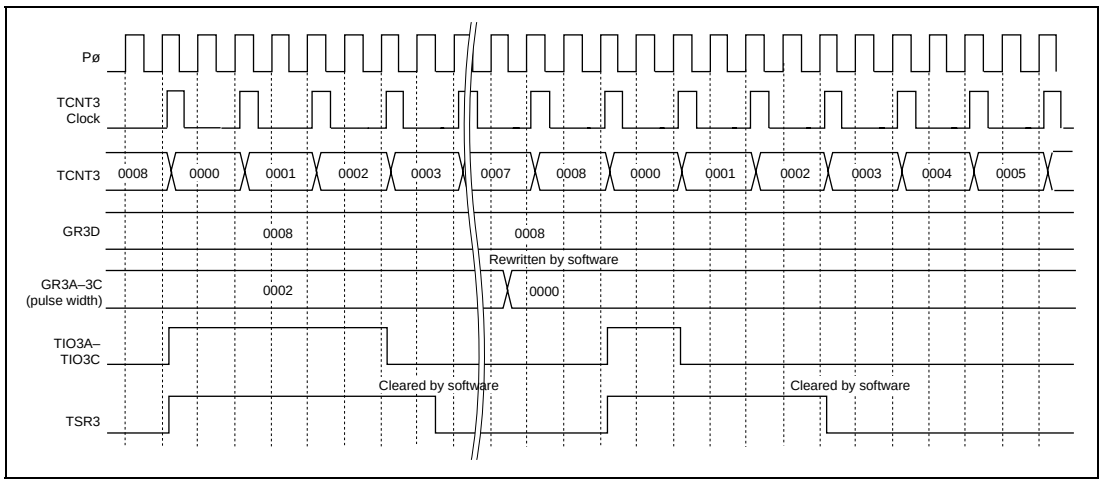

Figure 11.23 Channel 3 to 5 PWM Mode Operation

11.3.11 Event Count Function and Event Cycle Measurement

Channel 9 has six 8-bit event counters (ECNT9A to ECNT9F) and corresponding general registers (GR9A to GR9F). Each event counter has an external pin (TI9A to TI9F).

Each ECNT9 operates unconditionally as an event counter. When an edge is input from the external pin, ECNT9 is incremented. When ECNT9 matches the value set in GR9, it is cleared, and then counts up when an edge is again input at the external pin. By making the appropriate setting in the interrupt enable register (TIER) beforehand, an interrupt request can be sent to the CPU on compare-match.

For ECNT9A to ECNT9D, a trigger can be transmitted to channel 3 when a compare-match occurs. In channel 3, if the channel 9 trigger input is set in the timer I/O control register (TIOR) and the corresponding bit is set to 1 in the timer start register (TSTR), the TCNT3 value is captured in the corresponding general register (GR3A to GR3D) when an ECNT9A to ECNT9D compare-match occurs. This enables the event cycle to be measured.

11.5.5 Registers Requiring 8-Bit Access

The timer mode register (TMDR), prescaler register (PSCR), timer I/O control registers (TIOR0, TIOR10, TIOR11), trigger mode register (TRGMDR), interval interrupt request register (ITVRR), timer control registers (TCR3, TCR4, TCR5, TCR8, TCR9A to TCR9C, TCR10, TCR11), PWM mode register (PMDR), reload enable register (RLDENR), free-running counters (TCNT10B, TCNT10D, TCNT10H), event counter (ECNT), general registers (GR9A to GR9F), output compare register (OCR10B), and noise canceler register (NCR) are 8-bit registers. These registers are connected to the upper 8 bits of the internal 16-bit data bus, and can be read or written a byte at a time.

Figure 11.52 shows the operation when performing individual byte read or write accesses to ITVRR1.

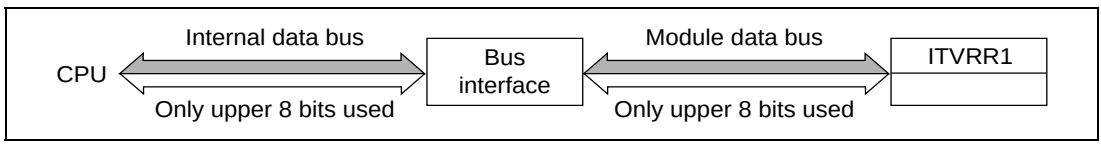

Figure 11.52 Byte Read/Write Access to ITVRR1

11.6 Sample Setup Procedures

Sample setup procedures for activating the various ATU-II functions are shown below.

Sample Setup Procedure for Input Capture: An example of the setup procedure for input capture is shown in figure 11.53.

1. Select the first-stage counter clock ø' in prescaler register (PSCR) and the second-stage counter clock ø" with the CKSEL bit in the timer control register (TCR). When selecting an external clock, also select the external clock edge type with the CKEG bit in TCR.
2. Set the port control register, corresponding to the port for signal input as the input capture trigger, to ATU input capture input.
3. Select rising edge, falling edge, or both edges as the input capture signal input edge(s) with the timer I/O control register (TIOR).

   If necessary, a timer interrupt request can be sent to the CPU on input capture by making the appropriate setting in the interrupt enable register (TIER). In channel 0, setting the DMAC allows DMAC activation to be performed.
4. Set the corresponding bit to 1 in the timer start register (TSTR) to start the free-running counter (TCNT) for the relevant channel.

Note: When input capture occurs, the counter value is always captured, irrespective of free-running counter (TCNT) activation.

Sample Setup Procedure for One-Shot pulse Output: An example of the setup procedure for one-shot pulse output is shown in figure 11.56.

1. Set the first-stage counter clock ø' in prescaler register 1 (PSCR1), and select the second-stage counter clock ø" with the CKSEL bit in timer control register8 TCR8.
2. Set port K control registers H and L (PKCRH, PKCRL) corresponding to the waveform output port to ATU one-shot pulse output. Also set the corresponding bit to 1 in the port K IO register (PKIOR) to specify the output attribute.
3. Set the one-shot pulse width in the down-counter (DCNT) corresponding to the port set in (2). If necessary, a timer interrupt request can be sent to the CPU when the down-counter underflows by making the appropriate setting in the interrupt enable register (TIER8).
4. Set the corresponding bit (DST8A to DST8P) to 1 in the down-count start register (DSTR) to start the down-counter (DCNT).

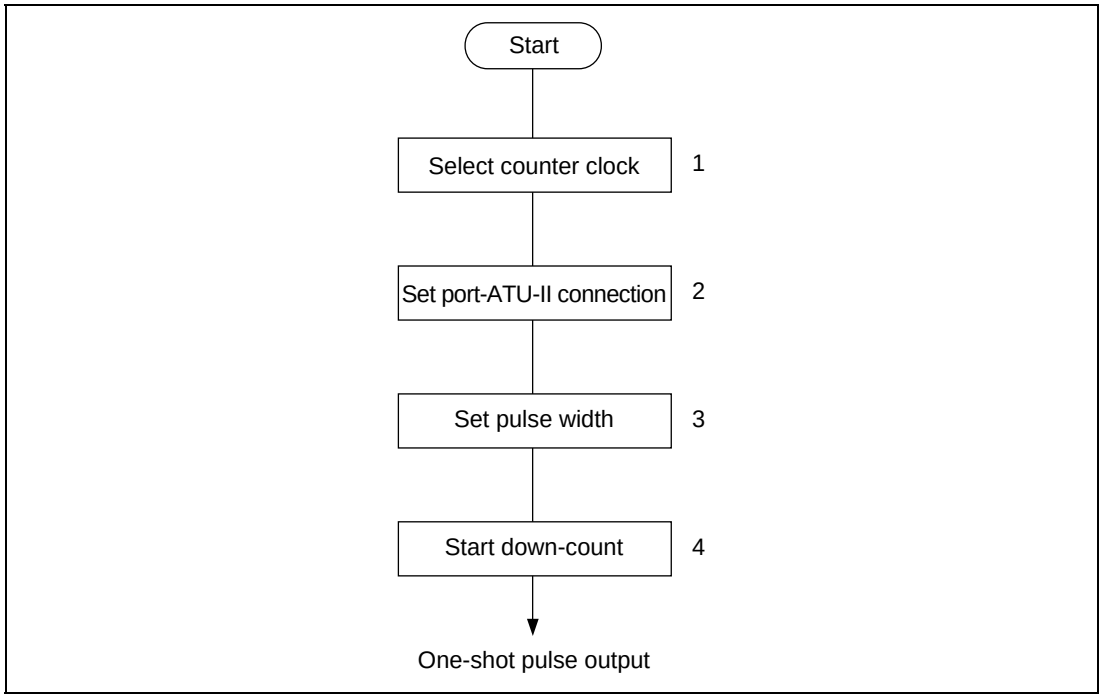

Figure 11.56 Sample Setup Procedure for One-Shot Pulse Output

13.2.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an 8-bit readable/writable register. (RSTCSR differs from other registers in that it is more difficult to write. See section 13.2.4, Register Access, for details.) It controls output of the internal reset signal generated by timer counter (TCNT) overflow. RSTCR is initialized to H'1F by input of a reset signal from the $\overline{\text{RES}}$ pin, but is not initialized by the internal reset signal generated by overflow of the WDT. It is initialized to H'1F in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	WOVF	RSTE	RSTS	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/(W)*	R/W	R/W	R	R	R	R	R

Note: * Only 0 can be written to bit 7 to clear the flag.

- Bit 7—Watchdog Timer Overflow Flag (WOVF): Indicates that TCNT has overflowed (H'FF to H'00) in watchdog timer mode. This flag is not set in interval timer mode.

Bit 7: WOVF	Description	
0	No TCNT overflow in watchdog timer mode	(Initial value)
	[Clearing condition]	
	When 0 is written to WOVF after reading WOVF	
1	Set by TCNT overflow in watchdog timer mode	

- Bit 6—Reset Enable (RSTE): Selects whether to reset the chip internally if TCNT overflows in watchdog timer mode.

Bit 6: RSTE	Description	
0	Not reset when TCNT overflows	(Initial value)
	LSI not reset internally, but TCNT and TCSR reset within WDT.	
1	Reset when TCNT overflows	

- Bit 5—Reset Select (RSTS): Selects the kind of internal reset to be generated when TCNT overflows in watchdog timer mode.

Bit 5: RSTS	Description	
0	Power-on reset	(Initial value)
1	Manual reset	

- Bits 4 to 0—Reserved: These bits are always read as 1. The write value should always be 1.

15.5 Usage Notes

Sections 15.5.1 through 15.5.9 provide information concerning use of the SCI.

15.5.1 TDR Write and TDRE Flag

The TDRE bit in the serial status register (SSR) is a status flag indicating loading of transmit data from TDR into TSR. The SCI sets TDRE to 1 when it transfers data from TDR to TSR. Data can be written to TDR regardless of the TDRE bit status. If new data is written in TDR when TDRE is 0, however, the old data stored in TDR will be lost because the data has not yet been transferred to TSR. Before writing transmit data to TDR, be sure to check that TDRE is set to 1.

15.5.2 Simultaneous Multiple Receive Errors

Table 15.13 indicates the state of the SSR status flags when multiple receive errors occur simultaneously. When an overrun error occurs, the RSR contents cannot be transferred to RDR, so receive data is lost.

Table 15.13 SSR Status Flags and Transfer of Receive Data

	SSR Status Flags				Receive Data Transfer
Receive Error Status	**RDRF**	**ORER**	**FER**	**PER**	**RSR → RDR**
Overrun error	1	1	0	0	X
Framing error	0	0	1	0	O
Parity error	0	0	0	1	O
Overrun error + framing error	1	1	1	0	X
Overrun error + parity error	1	1	0	1	X
Framing error + parity error	0	0	1	1	O
Overrun error + framing error + parity error	1	1	1	1	X

Notes: O: Receive data is transferred from RSR to RDR.
X: Receive data is not transferred from RSR to RDR.

Initialization (after Hardware Reset Only): These settings should be made while the HCAN is in bit configuration mode.

1. IRR0 clearing

   The reset interrupt flag (IRR0) is always set after a power-on reset or recovery from software standby mode. As an HCAN interrupt is initiated immediately when interrupts are enabled, IRR0 should be cleared.

2. HCAN pin port settings

   To prevent erroneous identification of CAN bus data, HCAN pin port settings should be made first. See HCAN Pin Port Settings in section 16.3.2, Initialization after a Hardware Reset, and section 20, Pin Function Controller, for details.

3. Bit rate settings

   Set values relating to the CAN bus communication speed and re-synchronization. See Bit Rate Settings in section 16.3.2, Initialization after a Hardware Reset, for details.

4. Mailbox transmit/receive settings

   Mailbox transmit/receive settings should be made in advance. A total of 30 mailbox can be set for transmission or reception (mailboxes 1 to 15 in HCAN0 and HCAN1). To set a mailbox for transmission, clear the corresponding bit to 0 in the mailbox configuration register (MBCR). See Mailbox Transmit/Receive Settings in section 16.3.2, Initialization after a Hardware Reset, for details.

5. Mailbox initialization

   As message control/data registers (MCx[x], MDx[x]) are configured in RAM, their initial values after powering on are undefined, and so bit initialization is necessary. Write 0s or 1s to the mailboxes. See Mailbox (Message Control/Data (MCx[x], MDx[x]) Initial Settings in section 16.3.2, Initialization after a Hardware Reset, for details.

6. Message transmission method setting

   Set the transmission method for mailboxes designated for transmission. The following two transmission methods can be used. See Setting the Message Transmission Method in section 16.3.2, Initialization after a Hardware Reset, for details.

   a. Transmission order determined by message identifier priority
   b. Transmission order determined by mailbox number priority

HCAN sleep mode is entered by setting the HCAN sleep mode bit (MCR5) to 1 in the master control register (MCR). If the CAN bus is operating, the transition to HCAN sleep mode is delayed until the bus becomes idle.

Either of the following methods of clearing HCAN sleep mode can be selected by making a setting in the MCR7 bit.

1. Clearing by software
2. Clearing by CAN bus operation

Eleven recessive bits must be received after HCAN sleep mode is cleared before CAN bus communication is enabled again.

Clearing by Software: Clearing by software is performed by having the CPU write 0 to MCR5.

Clearing by CAN Bus Operation: Clearing by CAN bus operation occurs automatically when the CAN bus performs an operation and this change is detected. In this case, the first message is not received in the message box; normal reception starts with the second message. When a change is detected on the CAN bus in HCAN sleep mode, the bus operation interrupt flag (IRR12) is set in the interrupt register (IRR). If the bus interrupt mask (IMR12) in the interrupt mask register (IMR) is set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

17.1.4 Register Configuration

Table 17.2 summarizes the A/D converter's registers.

Table 17.2 A/D Converter Registers

Name	Abbreviation	R/W	Initial Value	Address	Access Size*[1]
A/D data register 0 (H/L)	ADDR0 (H/L)	R	H'0000	H'FFFFF800	8, 16
A/D data register 1 (H/L)	ADDR1 (H/L)	R	H'0000	H'FFFFF802	8, 16
A/D data register 2 (H/L)	ADDR2 (H/L)	R	H'0000	H'FFFFF804	8, 16
A/D data register 3 (H/L)	ADDR3 (H/L)	R	H'0000	H'FFFFF806	8, 16
A/D data register 4 (H/L)	ADDR4 (H/L)	R	H'0000	H'FFFFF808	8, 16
A/D data register 5 (H/L)	ADDR5 (H/L)	R	H'0000	H'FFFFF80A	8, 16
A/D data register 6 (H/L)	ADDR6 (H/L)	R	H'0000	H'FFFFF80C	8, 16
A/D data register 7 (H/L)	ADDR7 (H/L)	R	H'0000	H'FFFFF80E	8, 16
A/D data register 8 (H/L)	ADDR8 (H/L)	R	H'0000	H'FFFFF810	8, 16
A/D data register 9 (H/L)	ADDR9 (H/L)	R	H'0000	H'FFFFF812	8, 16
A/D data register 10 (H/L)	ADDR10 (H/L)	R	H'0000	H'FFFFF814	8, 16
A/D data register 11 (H/L)	ADDR11 (H/L)	R	H'0000	H'FFFFF816	8, 16
A/D data register 12 (H/L)	ADDR12 (H/L)	R	H'0000	H'FFFFF820	8, 16
A/D data register 13 (H/L)	ADDR13 (H/L)	R	H'0000	H'FFFFF822	8, 16
A/D data register 14 (H/L)	ADDR14 (H/L)	R	H'0000	H'FFFFF824	8, 16
A/D data register 15 (H/L)	ADDR15 (H/L)	R	H'0000	H'FFFFF826	8, 16
A/D data register 16 (H/L)	ADDR16 (H/L)	R	H'0000	H'FFFFF828	8, 16
A/D data register 17 (H/L)	ADDR17 (H/L)	R	H'0000	H'FFFFF82A	8, 16
A/D data register 18 (H/L)	ADDR18 (H/L)	R	H'0000	H'FFFFF82C	8, 16
A/D data register 19 (H/L)	ADDR19 (H/L)	R	H'0000	H'FFFFF82E	8, 16
A/D data register 20 (H/L)	ADDR20 (H/L)	R	H'0000	H'FFFFF830	8, 16
A/D data register 21 (H/L)	ADDR21 (H/L)	R	H'0000	H'FFFFF832	8, 16
A/D data register 22 (H/L)	ADDR22 (H/L)	R	H'0000	H'FFFFF834	8, 16
A/D data register 23 (H/L)	ADDR23 (H/L)	R	H'0000	H'FFFFF836	8, 16
A/D data register 24 (H/L)	ADDR24 (H/L)	R	H'0000	H'FFFFF840	8, 16
A/D data register 25 (H/L)	ADDR25 (H/L)	R	H'0000	H'FFFFF842	8, 16
A/D data register 26 (H/L)	ADDR26 (H/L)	R	H'0000	H'FFFFF844	8, 16

22.2.4 Flash Memory Configuration

This LSI's flash memory is configured by the 512-kbyte user MAT and 8-kbyte user boot MAT.

The start address is allocated to the same address in the user MAT and user boot MAT. Therefore, when the program execution or data access is performed between the two MATs, the MAT must be switched by using FMATS. The user MAT is divided into two 512-kbyte banks (bank 0 and bank 1).

The user MAT or user boot MAT can be read in all modes if it is in ROM valid mode. However, the user boot MAT can be programmed only in boot mode and programmer mode.

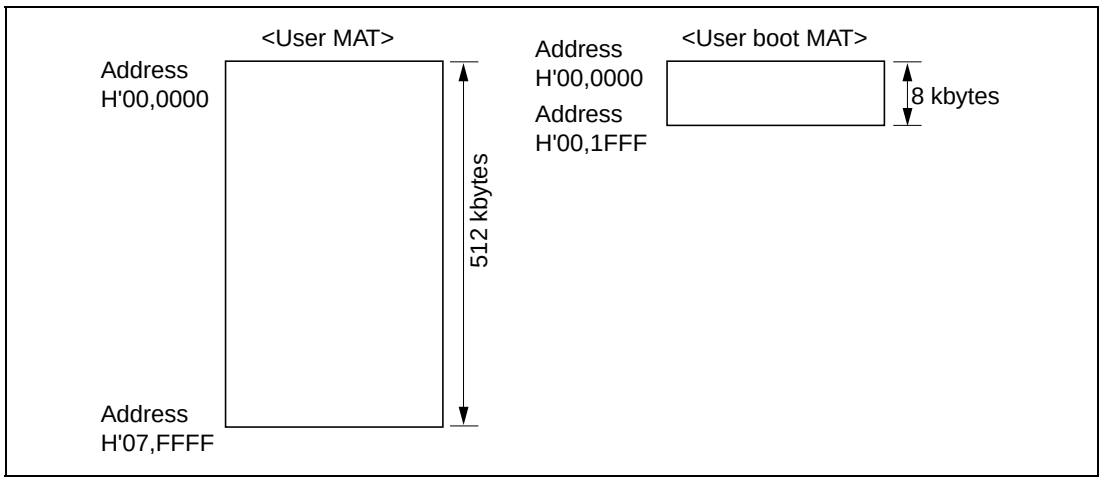

Figure 22.3 Flash Memory Configuration

The user MAT and user boot MAT have different memory sizes. Do not access a user boot MAT that is 8 kbytes or more. When a user boot MAT exceeding 8 kbytes is read from, an undefined value is read.

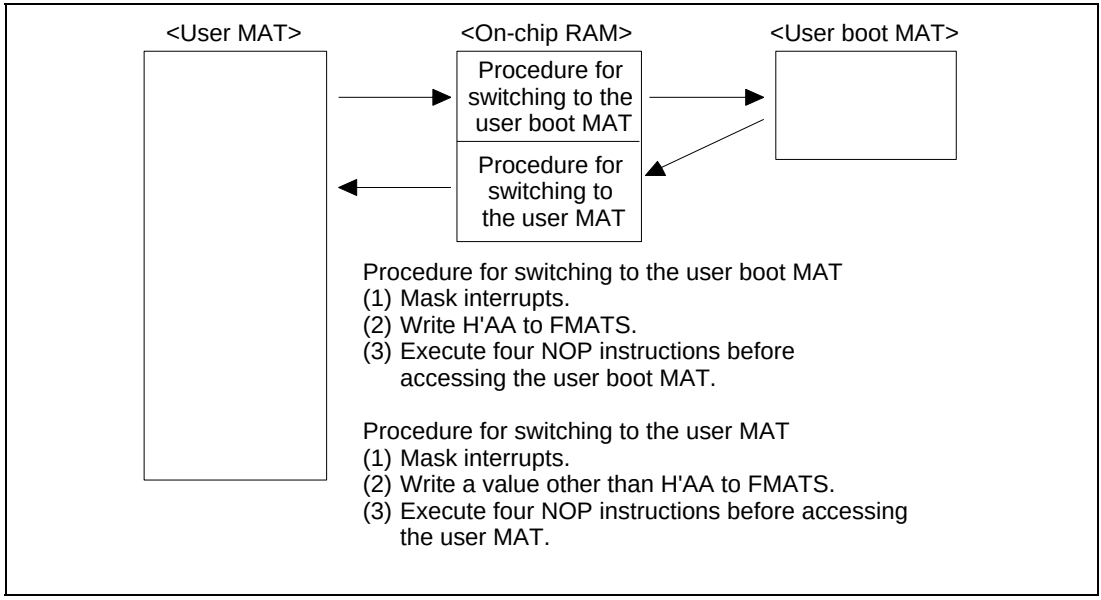

Figure 22.20 Switching between User MAT and User Boot MAT

22.8.2 Interrupts during Programming/Erasing

(1) Download of On-Chip Program

(1.1) VBR setting change

Before downloading the on-chip program, VBR must be set to H'00000000 (initial value). If VBR is set to a value other than the initial value, the interrupt vector table is placed in the user MAT (FMATS is not H'AA) or the user boot MAT (FMATS is H'AA) on initialization of VBR.

When VBR setting change conflicts with interrupt occurrence, whether the vector table before or after VBR is changed is referenced may cause an error.

Therefore, for cases where VBR setting change may conflict with interrupt occurrence, prepare a vector table to be referenced when VBR is H'00000000 at the start of the user MAT or user boot MAT.

(1.2) SCO download request and interrupt request

Download of the on-chip programming/erasing program that is initiated by setting the SCO bit in FCCS to 1 generates a particular interrupt processing accompanied by MAT switchover. Operation when the SCO download request and interrupt request conflicts is described below.

1. Contention between SCO download request and interrupt request
   Figure 22.21 shows the timing of contention between execution of the instruction that sets the SCO bit in FCCS to 1 and interrupt acceptance.

Table 26.2 Correspondence between Power Supply Names and Pins (cont)

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin Function 1	Function 2	Function 3	Function 4	Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
24			PE13	A13			$PV_{cc}1$	$PV_{cc}1+0.3$	
25			PE14	A14			$PV_{cc}1$	$PV_{cc}1+0.3$	
26			PE15	A15			$PV_{cc}1$	$PV_{cc}1+0.3$	
27			PF0	A16			$PV_{cc}1$	$PV_{cc}1+0.3$	
28			PF1	A17			$PV_{cc}1$	$PV_{cc}1+0.3$	
29			PF2	A18			$PV_{cc}1$	$PV_{cc}1+0.3$	
30	V_{CL}								
31			PF3	A19			$PV_{cc}1$	$PV_{cc}1+0.3$	
32	V_{ss}								
33			PF4	A20			$PV_{cc}1$	$PV_{cc}1+0.3$	
34			PF5	A21	$\overline{POD}$		$PV_{cc}1$	$PV_{cc}1+0.3$	
35			PF6	$\overline{WRL}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
36			PF7	$\overline{WRH}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
37			PF8	$\overline{WAIT}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
38			PF9	$\overline{RD}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
39	$PV_{cc}1$								
40			PF10	$\overline{CS0}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
41	V_{ss}								
42			PF11	$\overline{CS1}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
43			PF12	$\overline{CS2}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
44			PF13	$\overline{CS3}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
45			PF14	$\overline{BACK}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
46			PF15	$\overline{BREQ}$			$PV_{cc}1$	$PV_{cc}1+0.3$	
47	V_{ss}								
48			CK				V_{cc}		
49	V_{cc}								
50		MD2						5.5+0.3	
51		EXTAL						$V_{cc}+0.3$	
52	V_{cc}								
53		XTAL					V_{cc}		

26.4 A/D Converter Characteristics

Table 26.19 shows A/D converter characteristics.

Table 26.19 A/D Converter Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = 3.3 V ±0.3 V, $PV_{CC}1$ = 5.0 V ±0.5 V/3.3 V ±0.3 V,
$PV_{CC}2$ = 5.0 V ±0.5 V, AV_{CC} = 5.0 V ±0.5 V, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –40°C to 125°C.
When $PV_{CC}1$ = 3.3 V ±0.3 V, V_{CC} = $PV_{CC}1$.
When writing or erasing on-chip flash memory, T_a = –40°C to 85°C.

	CSK = 0: fop = 10–20 MHz			CSK = 1: fop = 10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bit
A/D conversion time	—	—	13.3	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permitted analog signal source impedance	—	—	3	—	—	3	kΩ
Non-linear error	—	—	±1.5*[1]	—	—	±1.5*[1]	LSB
			±2.5*[2]			±2.5*[2]	
Offset error	—	—	±1.5*[1]	—	—	±1.5*[1]	LSB
			±2.5*[2]			±2.5*[2]	
Full-scale error	—	—	±1.5*[1]	—	—	±1.5*[1]	LSB
			±2.5*[2]			±2.5*[2]	
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute error	—	—	±2.0*[1]	—	—	±2.0*[1]	LSB
			±2.5*[2]			±2.5*[2]	

Note: *1 Ta≤105°C
*2 Ta>105°C

Table A.1 Address (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE488	MC13[1]					DLC3	DLC2	DLC1	DLC0	HCAN (channel 0)
H'FFFFE489	MC13[2]									
H'FFFFE48A	MC13[3]									
H'FFFFE48B	MC13[4]									
H'FFFFE48C	MC13[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE48D	MC13[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE48E	MC13[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE48F	MC13[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE490	MC14[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE491	MC14[2]									
H'FFFFE492	MC14[3]									
H'FFFFE493	MC14[4]									
H'FFFFE494	MC14[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE495	MC14[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE496	MC14[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE497	MC14[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE498	MC15[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE499	MC15[2]									
H'FFFFE49A	MC15[3]									
H'FFFFE49B	MC15[4]									
H'FFFFE49C	MC15[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE49D	MC15[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE49E	MC15[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE49F	MC15[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE4A0 to H'FFFFE4AF	—	—	—	—	—	—	—	—	—	
H'FFFFE4B0	MD0[1]	MSG_DATA_1								
H'FFFFE4B1	MD0[2]	MSG_DATA_2								
H'FFFFE4B2	MD0[3]	MSG_DATA_3								
H'FFFFE4B3	MD0[4]	MSG_DATA_4								
H'FFFFE4B4	MD0[5]	MSG_DATA_5								
H'FFFFE4B5	MD0[6]	MSG_DATA_6								
H'FFFFE4B6	MD0[7]	MSG_DATA_7								
H'FFFFE4B7	MD0[8]	MSG_DATA_8								

Table A.1 Address (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFECD0	SAR1									DMAC (channel 1)
H'FFFFECD1										
H'FFFFECD2										
H'FFFFECD3										
H'FFFFECD4	DAR1									
H'FFFFECD5										
H'FFFFECD6										
H'FFFFECD7										
H'FFFFECD8	DMATCR1	—	—	—	—	—	—	—	—	
H'FFFFECD9										
H'FFFFECDA										
H'FFFFECDB										
H'FFFFECDC	CHCR1	—	—	—	—	—	—	—	—	
H'FFFFECDD		—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFFECDE		—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFFECDF		—	—	TS1	TS0	TM	IE	TE	DE	
H'FFFFECE0	SAR2									DMAC (channel 2)
H'FFFFECE1										
H'FFFFECE2										
H'FFFFECE3										
H'FFFFECE4	DAR2									
H'FFFFECE5										
H'FFFFECE6										
H'FFFFECE7										
H'FFFFECE8	DMATCR2	—	—	—	—	—	—	—	—	
H'FFFFECE9										
H'FFFFECEA										
H'FFFFECEB										
H'FFFFECEC	CHCR2	—	—	—	—	—	—	—	RO	
H'FFFFECED		—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFFECEE		—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFFECEF		—	—	TS1	TS0	TM	IE	TE	DE	

Table A.1 Address (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFF51E	DTR6D									ATU-II (channel 6)
H'FFFFF51F										
H'FFFFF520	TCR6B	—	CKSELD2	CKSELD1	CKSELD0	—	CKSELC2	CKSELC1	CKSELC0	
H'FFFFF521	TCR6A	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0	
H'FFFFF522	TSR6	—	—	—	—	—	—	—	—	
H'FFFFF523		UD6D	UD6C	UD6B	UD6A	CMF6D	CMF6C	CMF6B	CMF6A	
H'FFFFF524	TIER6	—	—	—	—	—	—	—	—	
H'FFFFF525		—	—	—	—	CME6D	CME6C	CME6B	CME6A	
H'FFFFF526	PMDR6	DTSELD	DTSELC	DTSELB	DTSELA	CNTSELD	CNTSELC	CNTSELB	CNTSELA	
H'FFFFF527 to H'FFFFF57F	—	—	—	—	—	—	—	—	—	—
H'FFFFF580	TCNT7A									ATU-II (channel 7)
H'FFFFF581										
H'FFFFF582	TCNT7B									
H'FFFFF583										
H'FFFFF584	TCNT7C									
H'FFFFF585										
H'FFFFF586	TCNT7D									
H'FFFFF587										
H'FFFFF588	CYLR7A									
H'FFFFF589										
H'FFFFF58A	CYLR7B									
H'FFFFF58B										
H'FFFFF58C	CYLR7C									
H'FFFFF58D										
H'FFFFF58E	CYLR7D									
H'FFFFF58F										
H'FFFFF590	BFR7A									
H'FFFFF591										
H'FFFFF592	BFR7B									
H'FFFFF593										
H'FFFFF594	BFR7C									
H'FFFFF595										
H'FFFFF596	BFR7D									
H'FFFFF597										

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