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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	LED, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l812a24dl

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1. GENERAL DESCRIPTION

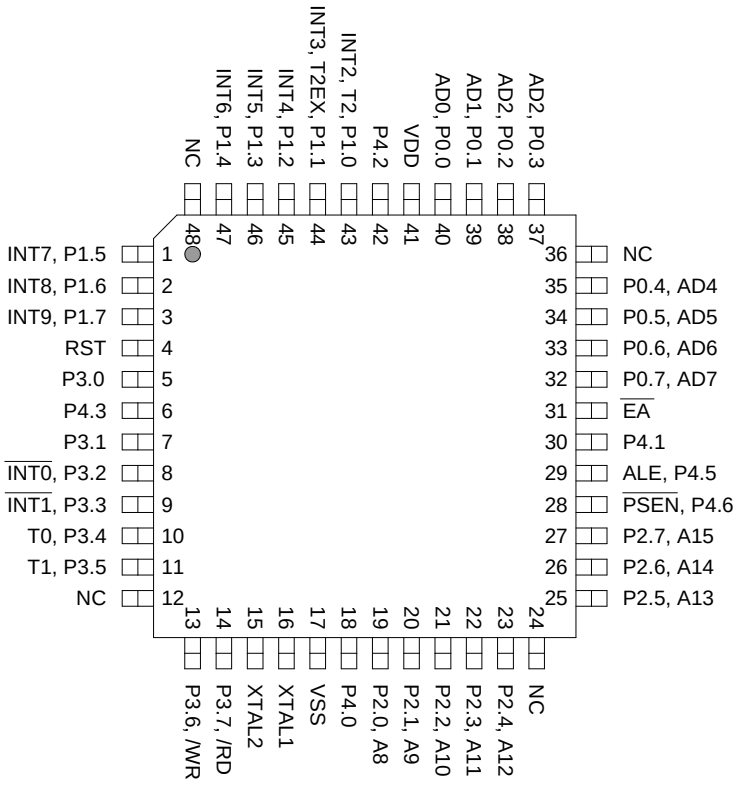
The W78L812 is an 8-bit microcontroller which can accommodate a wide range of supply voltages with low power consumption. The instruction set for the W78L812 is fully compatible with the standard 8051. The W78L812 contains an 8K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 5-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by a fourteen sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L812 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78L812 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 8 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- Three 16-bit timer/counters
- Timer 2 Clock-out
- One full duplex serial port (UART)
- Watchdog Timer
- Direct LED drive outputs
- Fourteen sources, two-level interrupt capability
- Wake-up via external interrupts at Port 1
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - Lead Free (RoHS) DIP 40: W78L812A24DL
  - Lead Free (RoHS) PLCC 44: W78L812A24PL
  - Lead Free (RoHS) PQFP 44: W78L812A24FL
  - Lead Free (RoHS) LQFP 48: W78L812A24LL

48-pin LQFP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34 P0.5, AD5
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31 EA
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29 ALE, P4.5
28 PSEN, P4.6
27 P2.7, A15
26 P2.6, A14
25 P2.5, A13
13 P3.6, /WR
14 P3.7, /RD
15 XTAL2
16 XTAL1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC

4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
$\overline{EA}$	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within on-chip ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin. This pin also serves the alternative function P4.6.
ALE	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	GROUND: Ground potential
VDD	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	PORT 0: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The pins of Port 0 can be individually configured to open-drain or standard port with internal pull-ups.
P1.0 – P1.7	PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control INT2 – INT9 (P1.0 – P1.7): External interrupt 2 to 9
P2.0 – P2.7	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0 – P3.7	PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. The pins P3.4 to P3.7 can be configured with high sink current which can drive LED displays directly. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port receiver input TXD(P3.1): Serial Port transmitter output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe
P4.0 – P4.6	PORT 4: A 5-bit bi-directional I/O port which is bit-addressable. Pins P4.0 to P4.3 are available on 44-pin PLCC/QFP package. P4.6 is the alternative function corresponding to $\overline{PSEN}$.

5.3 I/O Port Options

The Port 0 and Port 3 of W78L812 may be configured with different types by setting the bits of the Port Options Register POR that is located at 86H. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the PUP bit in the POR register is set, the pins of Port 0 will perform a quasi-bi-directional I/O port with internal pull-up that is structurally the same as Port 2. The high nibble of Port 3 (P3.4 to P3.7) can be selected to serve the direct LED displays drive outputs by setting the HDx bit in the PO register. When the HDx bit is set, the corresponding pin P3.x can sink about 20mA current for driving LED display directly. After reset, the POR register is cleared and the pins of Ports 0 and 3 are the same as those of the standard 80C31. The POR register is shown below.

5.3.1 Port Options Register

Bit:	7	6	5	4	3	2	1	0
	EP6	-	-	HD7	HD6	HD5	HD4	PUP

Mnemonic: POR Address: 86H

PUP : Enable Port 0 weak pull-up.

HD4 – 7: Enable pins P3.4 to P3.7 individually with High Drive outputs.

EP6 : Enable P4.6. To set this bit shifts $\overline{\text{PSEN}}$ pin to the alternate function P4.6

5.4 Port 4

The W78L812 has one additional bit-addressable I/O port P4 in which the port address is D8H. The Port 4 contains seven bits; P4.0 to P4.3 are only available on 44-pin PLCC/QFP package; P4.6 is the alternate function corresponding to pin $\overline{\text{PSEN}}$. When program is running in the internal memory without any access to external memory, PSEN may be individually configured to the alternate functions P4.6 that serve as general purpose I/O pins. To enable I/O port P4.6, the bit EP6 in the POR register must be set. During reset, the, $\overline{\text{PSEN}}$ perform as in the standard 80C32. The alternate functions P4.6 must be enabled by software. Care must be taken with the ALE pins when configured as the alternate functions.

5.4.1 Port 4

Bit:	7	6	5	4	3	2	1	0
	-	P4.6	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: D8H

5.5 Interrupt System

The W78L812 has fourteen interrupt sources: $\overline{INT0}$ and $\overline{INT1}$; Timer 0,1 and 2; Serial Port; INT2 to INT9. Each interrupt vectors to a specific location in program memory for its interrupt service routine. Each of these sources can be individually enabled or disabled by setting or clearing the corresponding bit in Special Function Register IE0 and IE1. The individual interrupt priority level depends on the Interrupt Priority Register IP0 and IP1. Additional external interrupts INT2 to INT9 are level sensitive and may be used to awake the device from power down mode. The Port 1 interrupts can be initialized to either active HIGH or LOW via setting the Interrupt Polarity Register IX. The IRQ register contains the flags of Port 1 interrupts. Each flag in IRQ register will be set when a interrupt request is recognized but *must be cleared by software*. Note that the interrupt flags have to be cleared before the interrupt service routine is completed, or else another interrupt will be generated.

5.5.1 Interrupt Enable Register 0

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8H

EA : Global enable. Enable/disable all interrupts.

ET2: Enable Timer 2 interrupt.

ES : Enable Serial Port interrupt.

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

5.5.2 Interrupt Enable Register 1

Bit:	7	6	5	4	3	2	1	0
	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Mnemonic: IE1 Address: E8H

EX9: Enable external interrupt 9 Note: 0 = interrupt disabled, 1 = interrupt enabled.

EX8: Enable external interrupt 8

EX7: Enable external interrupt 7

EX6: Enable external interrupt 6

EX5: Enable external interrupt 5

EX4: Enable external interrupt 4

EX3: Enable external interrupt 3

EX2: Enable external interrupt 2

5.5.6 Interrupt Request Flag Register

Bit:	7	6	5	4	3	2	1	0
	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Mnemonic: IRQ Address: C0H

IQ9: External interrupt 9 request flag.
IQ8: External interrupt 8 request flag.
IQ7: External interrupt 7 request flag.
IQ6: External interrupt 6 request flag.
IQ5: External interrupt 5 request flag.
IQ4: External interrupt 4 request flag.
IQ3: External interrupt 3 request flag.
IQ2: External interrupt 2 request flag.

Table.1 Priority level for simultaneous requests of the same priority interrupt sources

SOURCE	FLAG	PRIORITY LEVEL	VECTOR ADDRESS
External Interrupt 0	IE0	(Highest)	0003H
Serial Port	RI + TI		0023H
External Interrupt 5	IQ5		0053H
Timer 0 Overflow	TF0		000BH
External Interrupt 6	IQ6		005BH
External Interrupt 1	IE1		0013H
External Interrupt 2	IQ2		003BH
External Interrupt 7	IQ7		0063H
Timer 1 Overflow	TF1		001BH
Timer 2 Overflow	TF2 + EXF2		002BH
External Interrupt 3	IQ3		0043H
External Interrupt 8	IQ8		006BH
External Interrupt 4	IQ4		004BH
External Interrupt 9	IQ9	(Lowest)	0073H

5.8.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator.

5.9 AUXR - Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

Mnemonic: AUXR Address: 8Eh

AO: Turn off ALE signal.

5.10 Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

5.11 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L812 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6. ON-CHIP ROM CHARACTERISTICS

The W78L812 has several modes to program the on-chip ROM. All these operations are configured by the pins RST, ALE, $\overline{PSEN}$, A9CTRL (P3.0), A13CTRL (P3.1), A14CTRL (P3.2), OECTRL (P3.3), $\overline{CE}$ (P3.6), $\overline{OE}$ (P3.7), A0 (P1.0) and V_{PP} ($\overline{EA}$). Moreover, the A15 – A0 (P2.7 – P2.0, P1.7 – P1.0) and the D7 – D0 (P0.7 – P0.0) serve as the address and data bus respectively for these operations.

6.1 Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

6.2 Output Disable Condition

When the $\overline{OE}$ is set to high, no data output appears on the D7… D0.

6.3 Program Operation

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the V_{PP} is reach to V_{CP} (12.5V) level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

6.4 Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

6.5 Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the V_{PP} is reach to V_{EP} level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

6.6 Erase Verify Operation

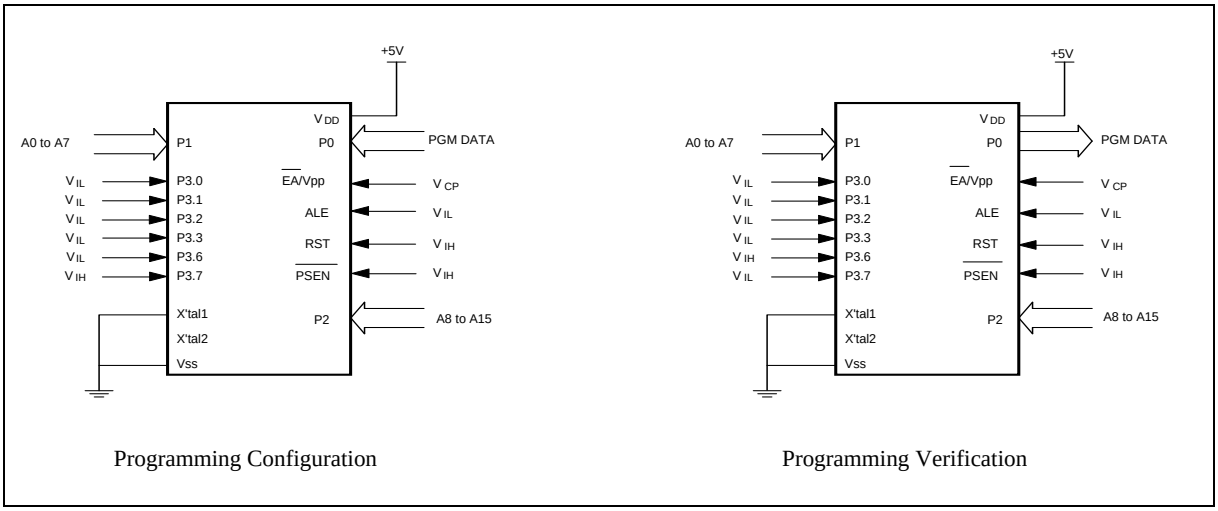
After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if $V_{PP} = V_{EP}$ (14.5V), $\overline{CE}$ is high and $\overline{OE}$ is low.

6.7 Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When P3.6 ($\overline{CE}$) = V_{IH}, P3.7 ($\overline{OE}$) = V_{IH}, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

6.8.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



7. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	VIN	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_a	0	70	°C
Storage Temperature	TST	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. DC CHARACTERISTICS

VSS = 0V, TA = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4	5.5	V	
Operating Current	I_{DD}	-	20	mA	V_{DD} = 5.5V, 20 MHz, no load, RST = 1
		-	3	mA	V_{DD} = 2.4V, 12 MHz, no load, RST = 1
Idle Current	I_{IDLE}	-	7	mA	V_{DD} = 5.5V, 20 MHz, no load
		-	1.5	mA	V_{DD} = 2.4V, 12 MHz, no load
Power Down Current	I_{PWDN}	-	50	µA	V_{DD} = 5.5V, no load
		-	30	µA	V_{DD} = 2.4V, no load
Input					
Input Current P1, P2, P3, P4	I_{IN}	-50	+10	µA	V_{DD} = 5.5V VIN = 0V or V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V VSS < VIN < V_{DD}
Input Current RST	I_{IN2}	-10	+0	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK1}	-60	+300	µA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1-to-0 Transition Current P1, P2, P3, P4		-500	-	µA	V_{DD} = 5.5V V_{IN} = 2V
Input Low Voltage		0	0.8	V	V_{DD} = 5.5V
P1, P2, P3, P4		0	0.5	V	V_{DD} = 2.4V
Input Low Voltage		0	0.8	V	V_{DD} = 5.5V
RST[*3]		0	0.3	V	V_{DD} = 2.4V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8		V_{DD} = 5.5V
		0	0.6	V	V_{DD} = 2.4V
Input High Voltage P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Output					
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA
Output Low Voltage P3[*6]	V_{OL3}	-	0.22	V	V_{DD} = 4.5V, I_{OL} = +2 mA
Sink current P1, P2, P3[5], P4<0:4>	I_{SK1}	4	12	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		1.8	5.4	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P0, ALE, $\overline{PSEN}$, P4.6	I_{SK2}	10	18	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		4.5	9	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P3.4 to P3.7 in High-Drive mode	I_{SK3}	12	24	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, V_{OH} = -100 μA
		1.4	-	V	V_{DD} = 2.4V, V_{OH} = -20 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source current P1, P2, P3, P4<0:4>	I_{SR1}	-120	-250	μA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-20	-40	μA	V_{DD} = 2.4V, V_{OH} = 1.4V
Source current P0, ALE, $\overline{PSEN}$, P4.6	I_{SR2}	-10	-14	mA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-1.9	-3.3	mA	V_{DD} = 2.4V, V_{OH} = 1.4V

Notes:

*1. RST pin has an internal pull-down.

*2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.

*3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.

*4. P0, P2, ALE and $\overline{PSEN}$ are tested in the external access mode.

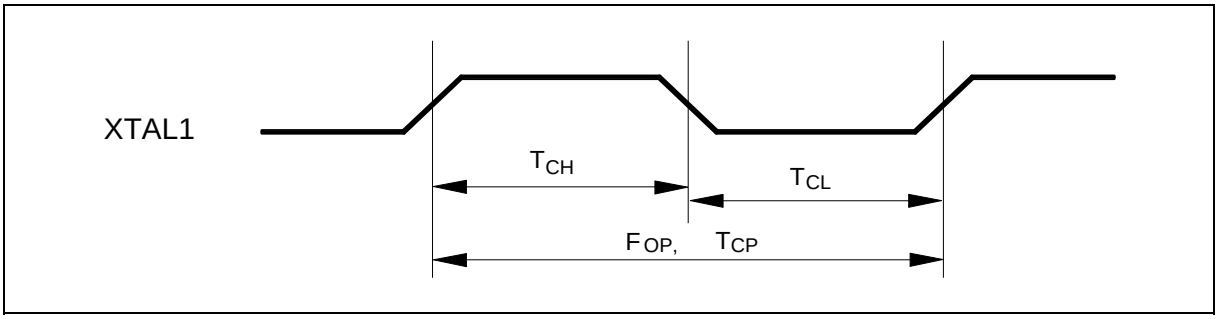
*5. P3.4 to P3.7 are in normal mode.

*6. P3 (P3.4 – P3.7) is used LED driver port by set SFR.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

9.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	20	MHz	1
Clock Period	T_{CP}	50	-	-	nS	2
Clock High	T_{CH}	25	-	-	nS	3
Clock Low	T_{CL}	25	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

9.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP} -Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP} -Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP} -Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP} -Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP} -Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

9.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP} -Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

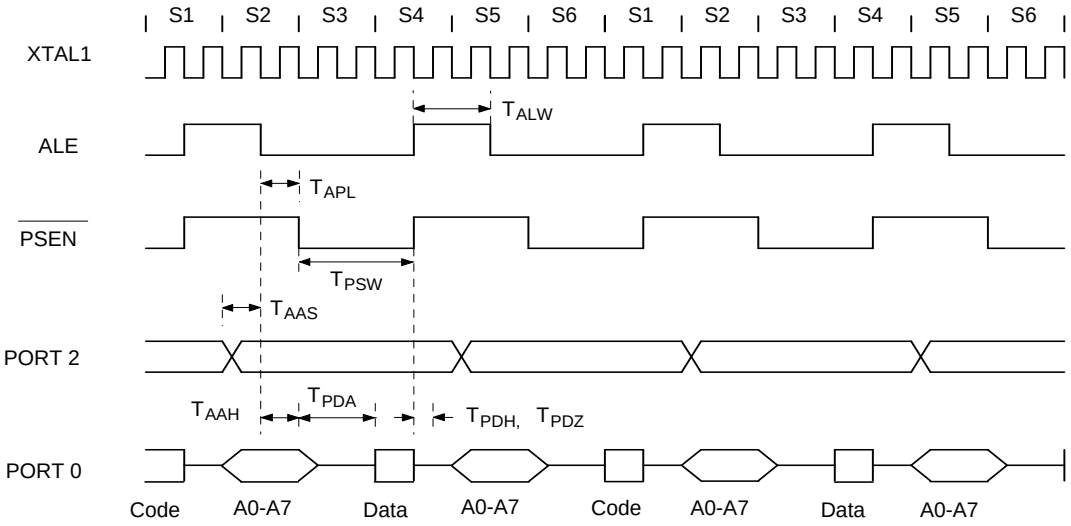
9.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP} -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP} -Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP} -Δ	6 T_{CP}	-	nS

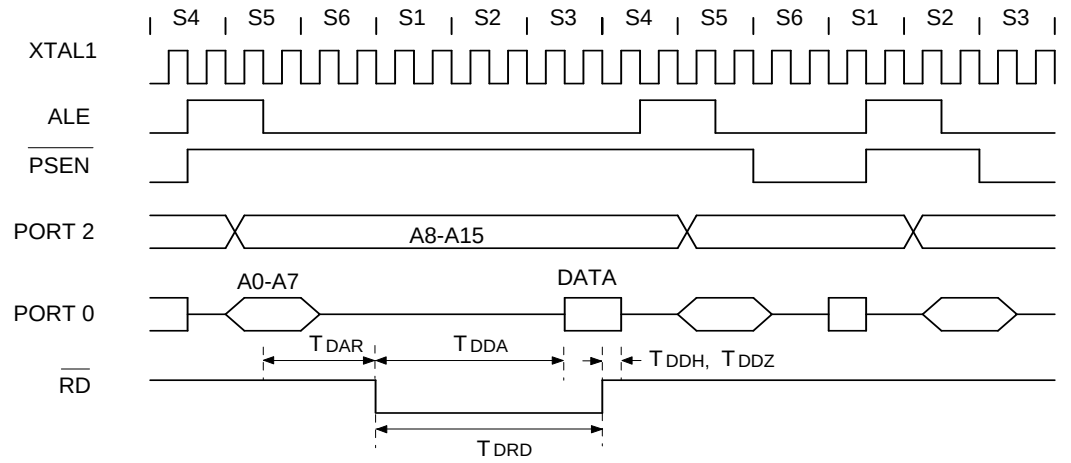
Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

10. TIMING WAVEFORMS

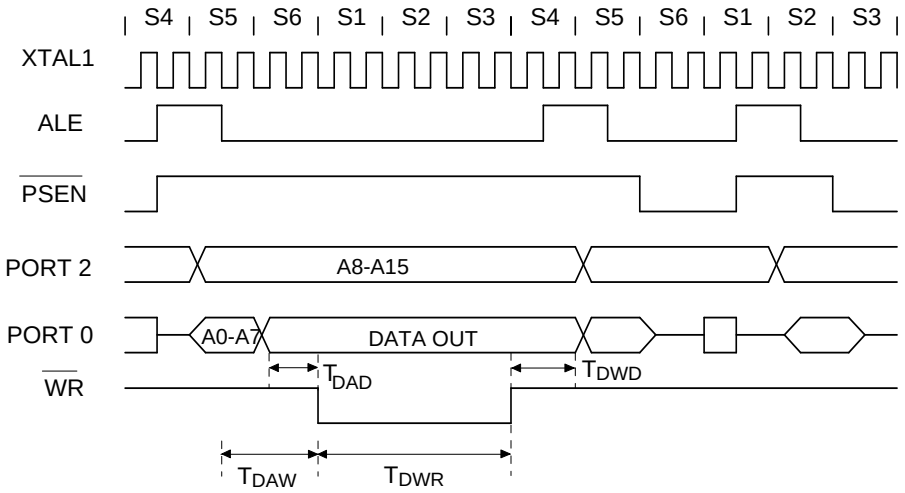
10.1 Program Fetch Cycle



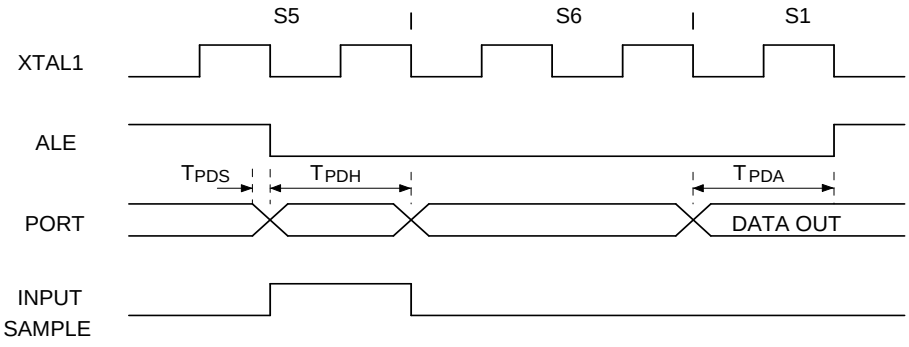
10.2 Data Read Cycle



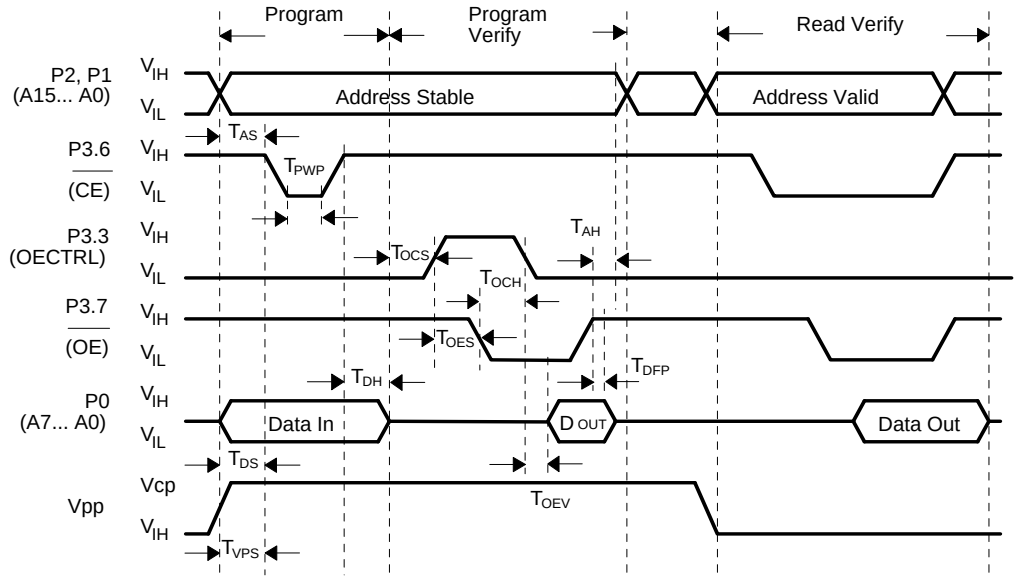
10.3 Data Write Cycle



10.4 Port Access Cycle

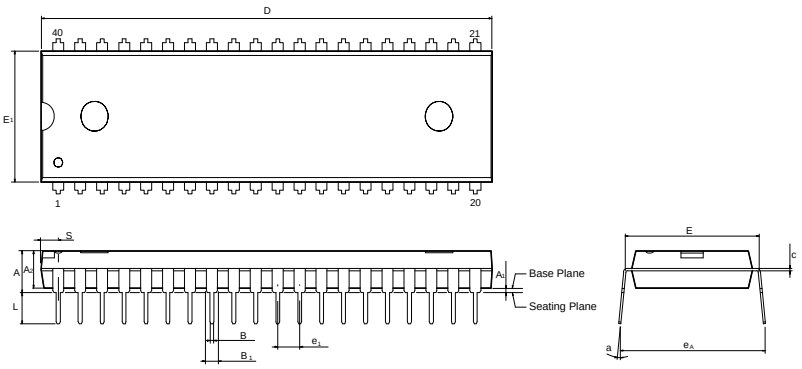


10.5 Program Operation



12. PACKAGE DIMENSIONS

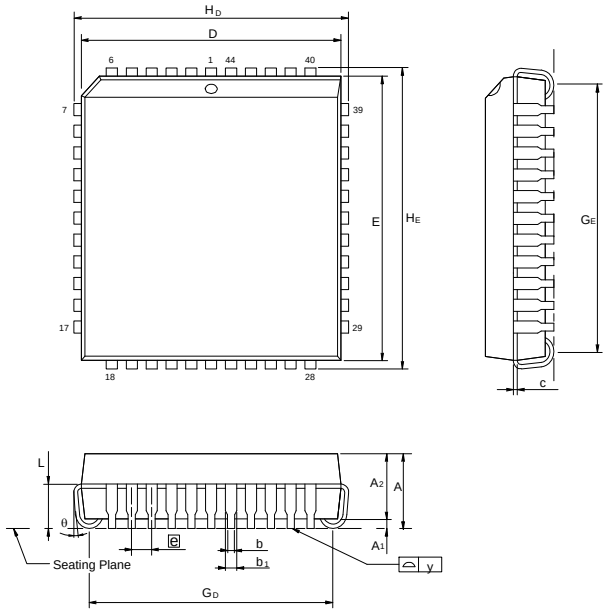
12.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

12.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

13. REVISION HISTORY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A5	October 15, 2001		-
A6	April 19, 2005	26	Add Important Notice
A7	July 1, 2005	3	Add lead free (RoHS) parts
A8	June 19, 2006	3,5	Add a part in 48-pin LQFP part
		31	Add package spec of 48-pin LQFP
		13,14	Correct the watchdog prescale table
A9	November 6, 2006		Remove block diagram
		3	Remove all Leaded package parts
A10	July 29, 2008	5	Correct typo and pin sequence in 48-pin LQFP diagram

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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