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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	LED, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l812a24fl

1. GENERAL DESCRIPTION

The W78L812 is an 8-bit microcontroller which can accommodate a wide range of supply voltages with low power consumption. The instruction set for the W78L812 is fully compatible with the standard 8051. The W78L812 contains an 8K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 5-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by a fourteen sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L812 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

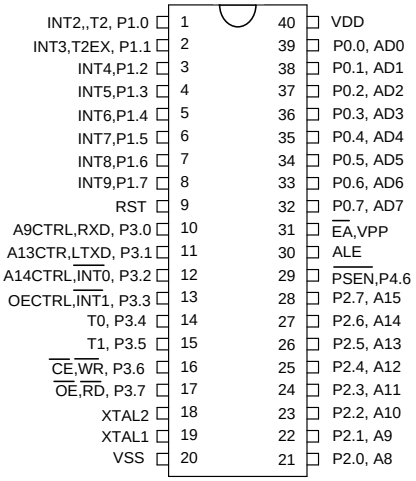
The W78L812 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

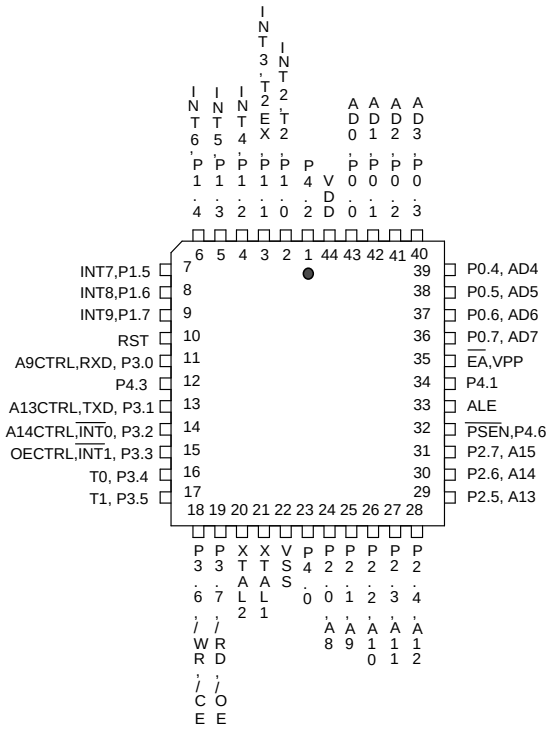
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 8 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- Three 16-bit timer/counters
- Timer 2 Clock-out
- One full duplex serial port (UART)
- Watchdog Timer
- Direct LED drive outputs
- Fourteen sources, two-level interrupt capability
- Wake-up via external interrupts at Port 1
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - Lead Free (RoHS) DIP 40: W78L812A24DL
  - Lead Free (RoHS) PLCC 44: W78L812A24PL
  - Lead Free (RoHS) PQFP 44: W78L812A24FL
  - Lead Free (RoHS) LQFP 48: W78L812A24LL

3. PIN CONFIGURATIONS

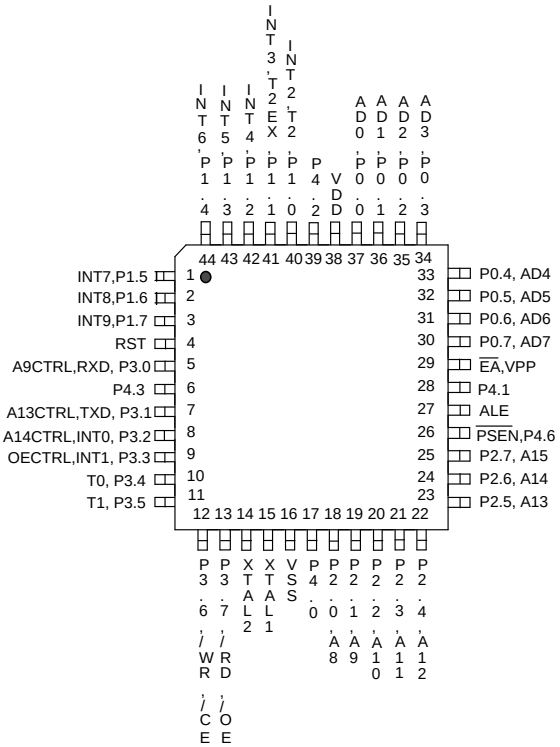
40-Pin DIP



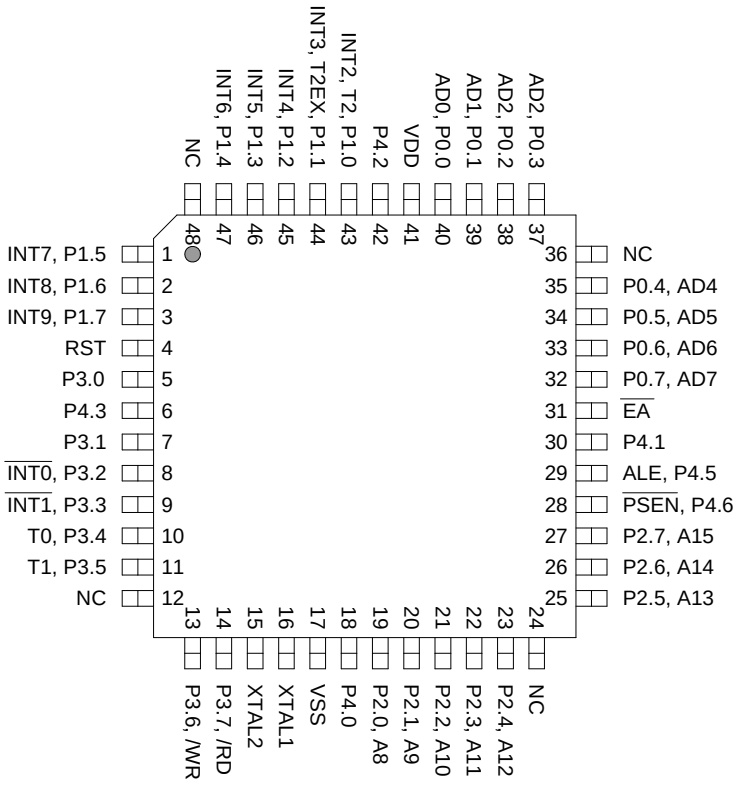
44-Pin PLCC



44-Pin PQFP



48-pin LQFP


NC 48
INT6, P1.4 47
INT5, P1.3 46
INT4, P1.2 45
INT3, T2EX, P1.1 44
INT2, T2, P1.0 43
P4.2 42
VDD 41
AD0, P0.0 40
AD1, P0.1 39
AD2, P0.2 38
AD2, P0.3 37
INT7, P1.5 1
INT8, P1.6 2
INT9, P1.7 3
RST 4
P3.0 5
P4.3 6
P3.1 7
INT0, P3.2 8
INT1, P3.3 9
T0, P3.4 10
T1, P3.5 11
NC 12
36 NC
35 P0.4, AD4
34 P0.5, AD5
33 P0.6, AD6
32 P0.7, AD7
31 EA
30 P4.1
29 ALE, P4.5
28 PSEN, P4.6
27 P2.7, A15
26 P2.6, A14
25 P2.5, A13
13 P3.6, /WR
14 P3.7, /RD
15 XTAL2
16 XTAL1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC

4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
$\overline{EA}$	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within on-chip ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin. This pin also serves the alternative function P4.6.
ALE	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	GROUND: Ground potential
VDD	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	PORT 0: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The pins of Port 0 can be individually configured to open-drain or standard port with internal pull-ups.
P1.0 – P1.7	PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control INT2 – INT9 (P1.0 – P1.7): External interrupt 2 to 9
P2.0 – P2.7	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0 – P3.7	PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. The pins P3.4 to P3.7 can be configured with high sink current which can drive LED displays directly. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port receiver input TXD(P3.1): Serial Port transmitter output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe
P4.0 – P4.6	PORT 4: A 5-bit bi-directional I/O port which is bit-addressable. Pins P4.0 to P4.3 are available on 44-pin PLCC/QFP package. P4.6 is the alternative function corresponding to $\overline{PSEN}$.

5.5 Interrupt System

The W78L812 has fourteen interrupt sources: $\overline{INT0}$ and $\overline{INT1}$; Timer 0,1 and 2; Serial Port; INT2 to INT9. Each interrupt vectors to a specific location in program memory for its interrupt service routine. Each of these sources can be individually enabled or disabled by setting or clearing the corresponding bit in Special Function Register IE0 and IE1. The individual interrupt priority level depends on the Interrupt Priority Register IP0 and IP1. Additional external interrupts INT2 to INT9 are level sensitive and may be used to awake the device from power down mode. The Port 1 interrupts can be initialized to either active HIGH or LOW via setting the Interrupt Polarity Register IX. The IRQ register contains the flags of Port 1 interrupts. Each flag in IRQ register will be set when a interrupt request is recognized but *must be cleared by software*. Note that the interrupt flags have to be cleared before the interrupt service routine is completed, or else another interrupt will be generated.

5.5.1 Interrupt Enable Register 0

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8H

EA : Global enable. Enable/disable all interrupts.

ET2: Enable Timer 2 interrupt.

ES : Enable Serial Port interrupt.

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

5.5.2 Interrupt Enable Register 1

Bit:	7	6	5	4	3	2	1	0
	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Mnemonic: IE1 Address: E8H

EX9: Enable external interrupt 9 Note: 0 = interrupt disabled, 1 = interrupt enabled.

EX8: Enable external interrupt 8

EX7: Enable external interrupt 7

EX6: Enable external interrupt 6

EX5: Enable external interrupt 5

EX4: Enable external interrupt 4

EX3: Enable external interrupt 3

EX2: Enable external interrupt 2

5.5.3 Interrupt Priority Register 0

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

IP.7: Unused.

IP.6: Unused.

PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.

PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.

PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.

PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.

PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.

PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

5.5.4 Interrupt Priority Register 1

Bit:	7	6	5	4	3	2	1	0
	PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Mnemonic: IP1 Address: F8h

PX9: This bit defines the External interrupt 9 priority. PX9 = 1 sets it to higher priority level.

PX8: This bit defines the External interrupt 8 priority. PX8 = 1 sets it to higher priority level.

PX7: This bit defines the External interrupt 7 priority. PX7 = 1 sets it to higher priority level.

PX6: This bit defines the External interrupt 6 priority. PX6 = 1 sets it to higher priority level.

PX5: This bit defines the External interrupt 5 priority. PX5 = 1 sets it to higher priority level.

PX4: This bit defines the External interrupt 4 priority. PX4 = 1 sets it to higher priority level.

PX3: This bit defines the External interrupt 3 priority. PX3 = 1 sets it to higher priority level.

PX2: This bit defines the External interrupt 2 priority. PX2 = 1 sets it to higher priority level.

5.5.5 Interrupt Polarity Register

Bit:	7	6	5	4	3	2	1	0
	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Mnemonic: IX Address: E9H

IL9: External interrupt 9 polarity level.

IL8: External interrupt 8 polarity level.

IL7: External interrupt 7 polarity level.

IL6: External interrupt 6 polarity level.

IL5: External interrupt 5 polarity level.

IL4: External interrupt 4 polarity level.

IL3: External interrupt 3 polarity level.

IL2: External interrupt 2 polarity level.

Note: 0 = active LOW, 1 = active HIGH.

5.5.6 Interrupt Request Flag Register

Bit:	7	6	5	4	3	2	1	0
	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Mnemonic: IRQ Address: C0H

IQ9: External interrupt 9 request flag.
IQ8: External interrupt 8 request flag.
IQ7: External interrupt 7 request flag.
IQ6: External interrupt 6 request flag.
IQ5: External interrupt 5 request flag.
IQ4: External interrupt 4 request flag.
IQ3: External interrupt 3 request flag.
IQ2: External interrupt 2 request flag.

Table.1 Priority level for simultaneous requests of the same priority interrupt sources

SOURCE	FLAG	PRIORITY LEVEL	VECTOR ADDRESS
External Interrupt 0	IE0	(Highest)	0003H
Serial Port	RI + TI		0023H
External Interrupt 5	IQ5		0053H
Timer 0 Overflow	TF0		000BH
External Interrupt 6	IQ6		005BH
External Interrupt 1	IE1		0013H
External Interrupt 2	IQ2		003BH
External Interrupt 7	IQ7		0063H
Timer 1 Overflow	TF1		001BH
Timer 2 Overflow	TF2 + EXF2		002BH
External Interrupt 3	IQ3		0043H
External Interrupt 8	IQ8		006BH
External Interrupt 4	IQ4		004BH
External Interrupt 9	IQ9	(Lowest)	0073H

5.6 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

5.6.1 Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2 – 0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 1 0	4
0 0 1	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

The time-out period is obtained using the following equation:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.

OPERATIONS	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ($\overline{CE}$)	P3.7 ($\overline{OE}$)	$\overline{EA}$ (VPP)	P2, P1 (A15… A0)	P0 (D7… D0)	NOTES
Read	0	0	0	0	0	0	1	Address	Data Out	
Output Disable	0	0	0	0	0	1	1	X	Hi-Z	
Program	0	0	0	0	0	1	VCP	Address	Data In	
Program Verify	0	0	0	0	1	0	VCP	Address	Data Out	@3
Erase	1	0	0	0	0	1	VEP	A0:0, others: X	Data In 0FFH	@4
Erase Verify	1	0	0	0	1	0	VEP	Address	Data Out	@5
Program/ Erase Inhibit	X	0	0	0	1	1	VCP/ VEP	X	X	

Notes:

1. All these operations happen in RST = V_{IH}, ALE = V_{IL} and $\overline{PSEN}$ = V_{IH}.
2. V_{CP} = 12.5V, V_{EP} = 14.5V, V_{IH} = V_{DD}, V_{IL} = V_{SS}.
3. The program verify operation follows behind the program operation.
4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
5. The erase verify operation follows behind the erase operation.

6.8 Security Bits

During the programmer operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78L812 has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The register can only be accessed from the on-chip ROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation.

The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.

8. DC CHARACTERISTICS

VSS = 0V, TA = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4	5.5	V	
Operating Current	I_{DD}	-	20	mA	V_{DD} = 5.5V, 20 MHz, no load, RST = 1
		-	3	mA	V_{DD} = 2.4V, 12 MHz, no load, RST = 1
Idle Current	I_{IDLE}	-	7	mA	V_{DD} = 5.5V, 20 MHz, no load
		-	1.5	mA	V_{DD} = 2.4V, 12 MHz, no load
Power Down Current	I_{PWDN}	-	50	µA	V_{DD} = 5.5V, no load
		-	30	µA	V_{DD} = 2.4V, no load
Input					
Input Current P1, P2, P3, P4	I_{IN}	-50	+10	µA	V_{DD} = 5.5V VIN = 0V or V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V VSS < VIN < V_{DD}
Input Current RST	I_{IN2}	-10	+0	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK1}	-60	+300	µA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1-to-0 Transition Current P1, P2, P3, P4		-500	-	µA	V_{DD} = 5.5V V_{IN} = 2V
Input Low Voltage		0	0.8	V	V_{DD} = 5.5V
P1, P2, P3, P4		0	0.5	V	V_{DD} = 2.4V
Input Low Voltage		0	0.8	V	V_{DD} = 5.5V
RST[*3]		0	0.3	V	V_{DD} = 2.4V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8		V_{DD} = 5.5V
		0	0.6	V	V_{DD} = 2.4V
Input High Voltage P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Output					
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA
Output Low Voltage P3[*6]	V_{OL3}	-	0.22	V	V_{DD} = 4.5V, I_{OL} = +2 mA
Sink current P1, P2, P3[5], P4<0:4>	I_{SK1}	4	12	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		1.8	5.4	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P0, ALE, $\overline{PSEN}$, P4.6	I_{SK2}	10	18	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		4.5	9	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P3.4 to P3.7 in High-Drive mode	I_{SK3}	12	24	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, V_{OH} = -100 μA
		1.4	-	V	V_{DD} = 2.4V, V_{OH} = -20 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source current P1, P2, P3, P4<0:4>	I_{SR1}	-120	-250	μA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-20	-40	μA	V_{DD} = 2.4V, V_{OH} = 1.4V
Source current P0, ALE, $\overline{PSEN}$, P4.6	I_{SR2}	-10	-14	mA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-1.9	-3.3	mA	V_{DD} = 2.4V, V_{OH} = 1.4V

Notes:

*1. RST pin has an internal pull-down.

*2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.

*3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.

*4. P0, P2, ALE and $\overline{PSEN}$ are tested in the external access mode.

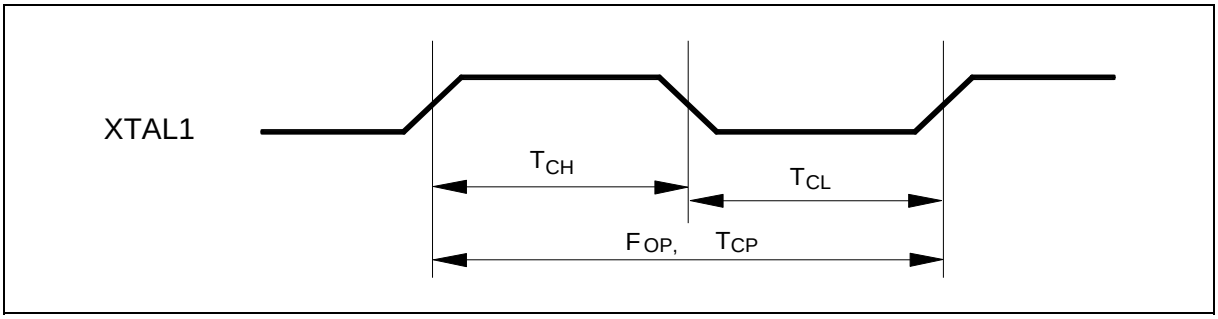
*5. P3.4 to P3.7 are in normal mode.

*6. P3 (P3.4 – P3.7) is used LED driver port by set SFR.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

9.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	20	MHz	1
Clock Period	T_{CP}	50	-	-	nS	2
Clock High	T_{CH}	25	-	-	nS	3
Clock Low	T_{CL}	25	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

9.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP} -Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP} -Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP} -Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP} -Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP} -Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

9.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP} -Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

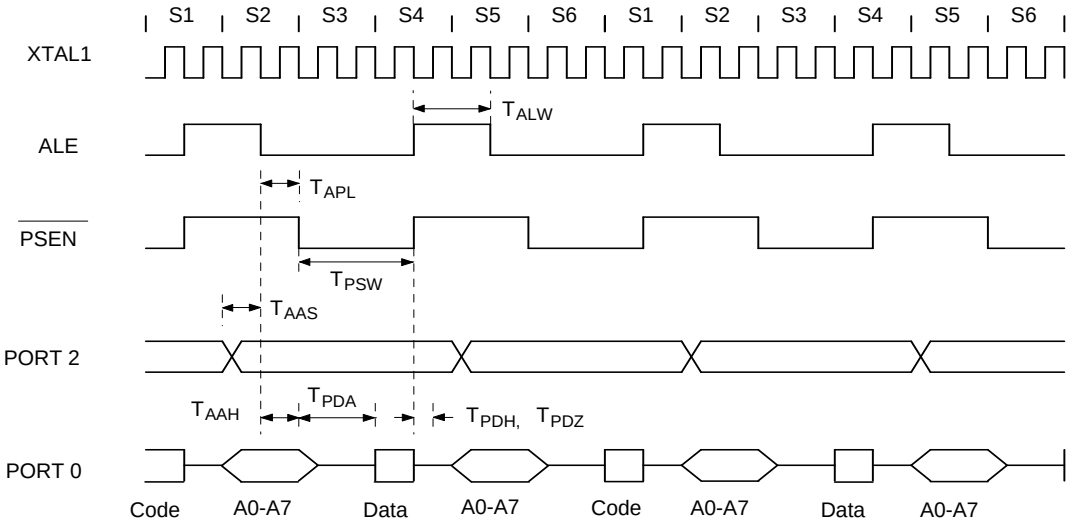
9.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP} -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP} -Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP} -Δ	6 T_{CP}	-	nS

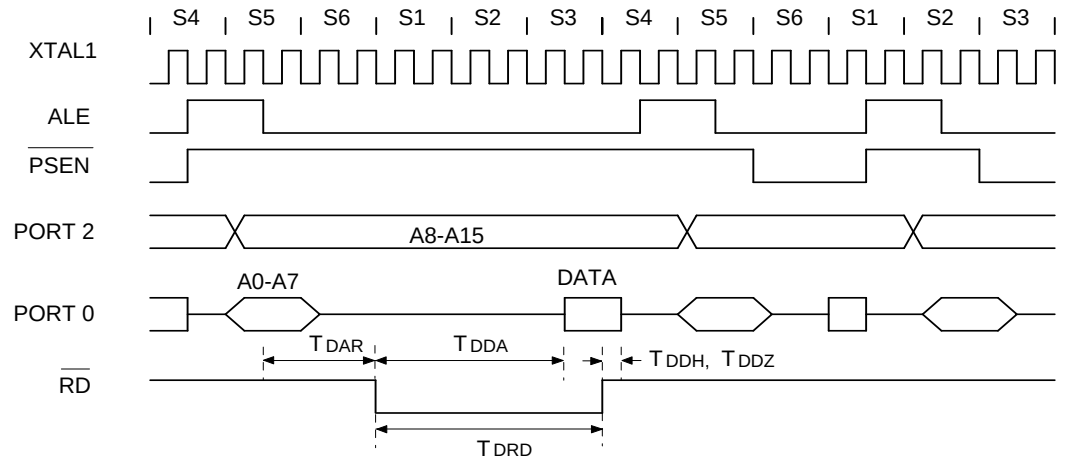
Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

10. TIMING WAVEFORMS

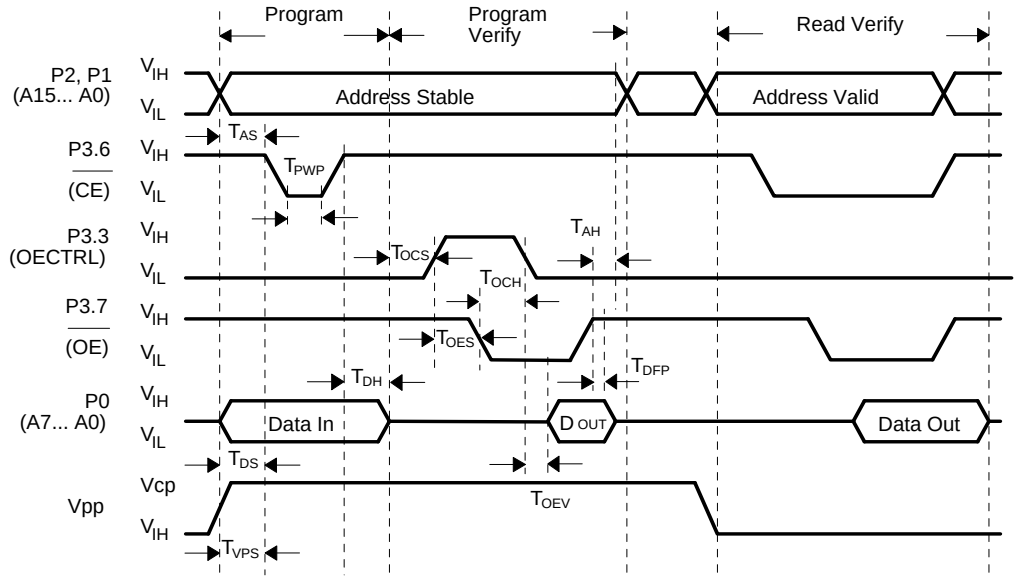
10.1 Program Fetch Cycle



10.2 Data Read Cycle



10.5 Program Operation



Typical Application Circuits, continued

11.2 Expanded External Data Memory and Oscillator

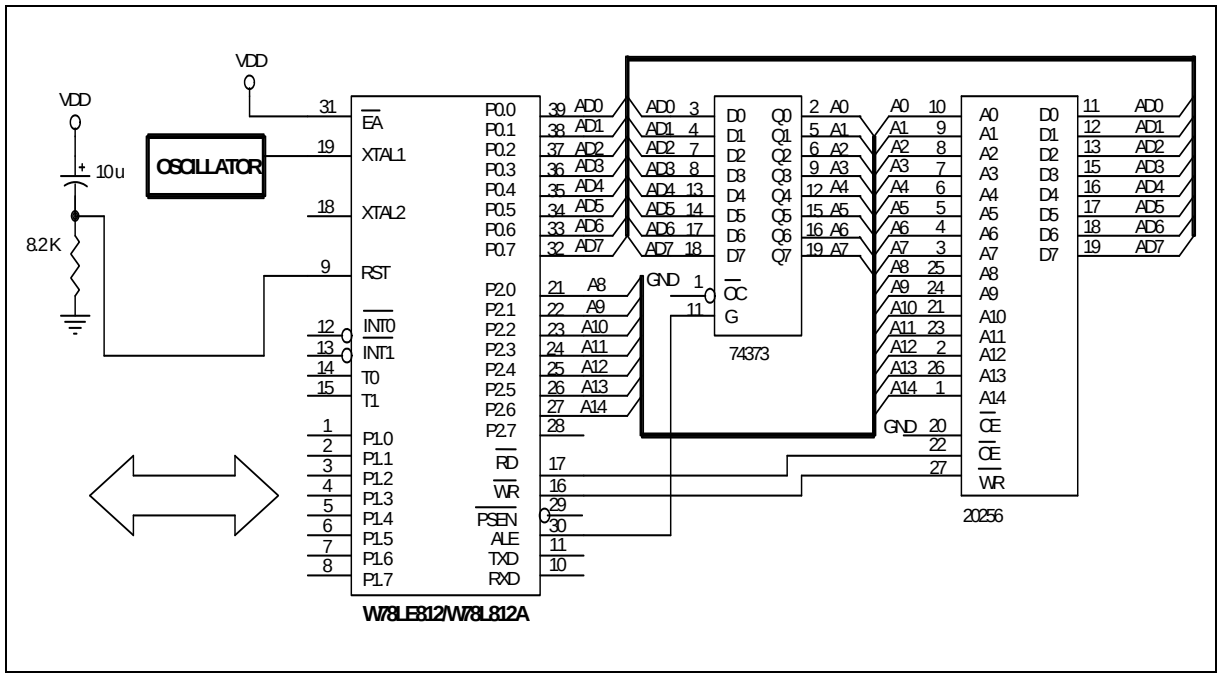
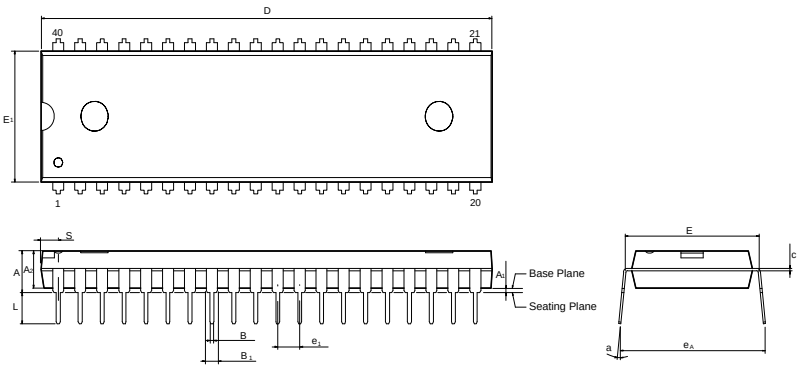


Figure B

12. PACKAGE DIMENSIONS

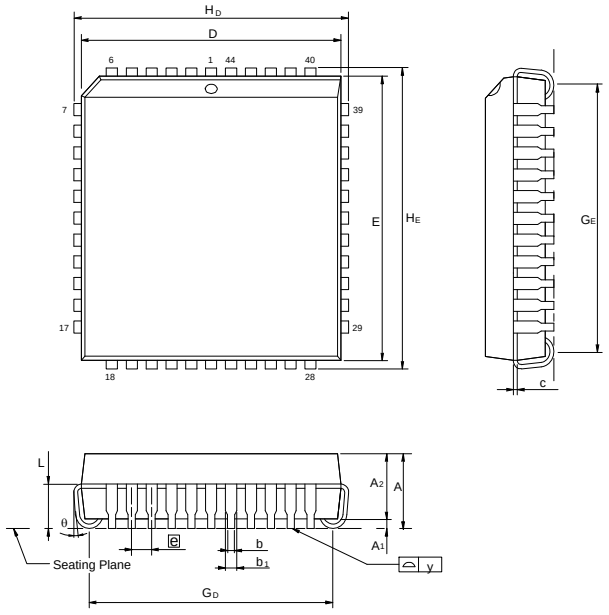
12.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

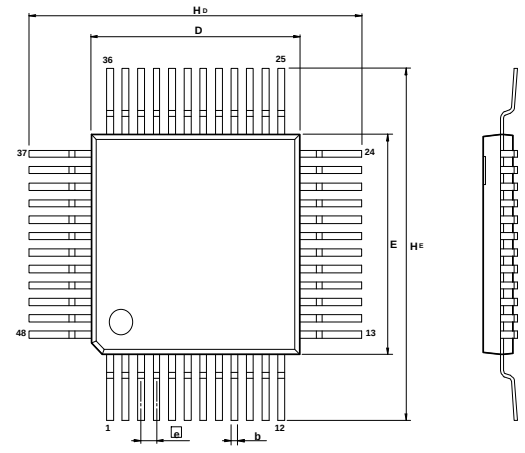
Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

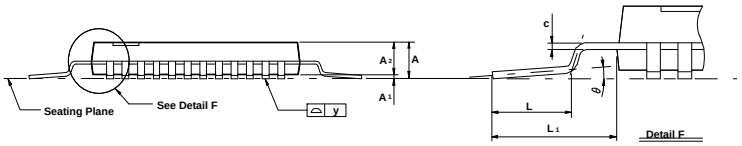
12.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.





Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	---	---	1.60
A_1	0.05	---	0.15
A_2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	---	0.20
D		7.00	
E		7.00	
e		0.50	
H_D		9.00	
H_E		9.00	
L	0.45	0.60	0.75
L_1		1.00	
y	---	0.08	---
θ	0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.