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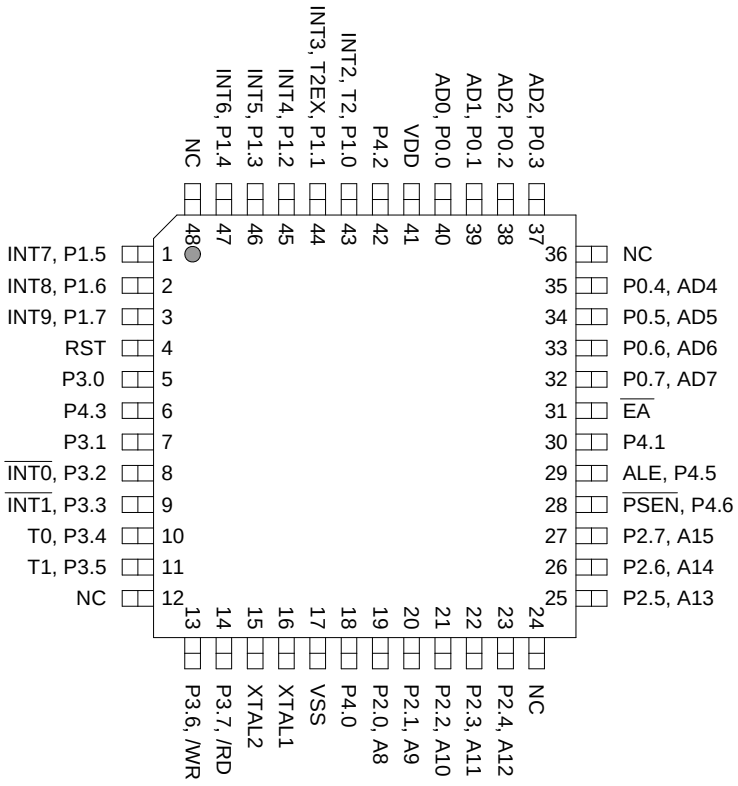
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	LED, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l812a24pl

48-pin LQFP


NC 48
INT6, P1.4 47
INT5, P1.3 46
INT4, P1.2 45
INT3, T2EX, P1.1 44
INT2, T2, P1.0 43
P4.2 42
VDD 41
AD0, P0.0 40
AD1, P0.1 39
AD2, P0.2 38
AD2, P0.3 37
INT7, P1.5 1
INT8, P1.6 2
INT9, P1.7 3
RST 4
P3.0 5
P4.3 6
P3.1 7
INT0, P3.2 8
INT1, P3.3 9
T0, P3.4 10
T1, P3.5 11
NC 12
36 NC
35 P0.4, AD4
34 P0.5, AD5
33 P0.6, AD6
32 P0.7, AD7
31 EA
30 P4.1
29 ALE, P4.5
28 PSEN, P4.6
27 P2.7, A15
26 P2.6, A14
25 P2.5, A13
13 P3.6, /WR
14 P3.7, /RD
15 XTAL2
16 XTAL1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC

4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
$\overline{EA}$	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within on-chip ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin. This pin also serves the alternative function P4.6.
ALE	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	GROUND: Ground potential
VDD	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	PORT 0: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The pins of Port 0 can be individually configured to open-drain or standard port with internal pull-ups.
P1.0 – P1.7	PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control INT2 – INT9 (P1.0 – P1.7): External interrupt 2 to 9
P2.0 – P2.7	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0 – P3.7	PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. The pins P3.4 to P3.7 can be configured with high sink current which can drive LED displays directly. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port receiver input TXD(P3.1): Serial Port transmitter output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe
P4.0 – P4.6	PORT 4: A 5-bit bi-directional I/O port which is bit-addressable. Pins P4.0 to P4.3 are available on 44-pin PLCC/QFP package. P4.6 is the alternative function corresponding to $\overline{PSEN}$.

5.3 I/O Port Options

The Port 0 and Port 3 of W78L812 may be configured with different types by setting the bits of the Port Options Register POR that is located at 86H. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the PUP bit in the POR register is set, the pins of Port 0 will perform a quasi-bi-directional I/O port with internal pull-up that is structurally the same as Port 2. The high nibble of Port 3 (P3.4 to P3.7) can be selected to serve the direct LED displays drive outputs by setting the HDx bit in the PO register. When the HDx bit is set, the corresponding pin P3.x can sink about 20mA current for driving LED display directly. After reset, the POR register is cleared and the pins of Ports 0 and 3 are the same as those of the standard 80C31. The POR register is shown below.

5.3.1 Port Options Register

Bit:	7	6	5	4	3	2	1	0
	EP6	-	-	HD7	HD6	HD5	HD4	PUP

Mnemonic: POR Address: 86H

PUP : Enable Port 0 weak pull-up.

HD4 – 7: Enable pins P3.4 to P3.7 individually with High Drive outputs.

EP6 : Enable P4.6. To set this bit shifts $\overline{\text{PSEN}}$ pin to the alternate function P4.6

5.4 Port 4

The W78L812 has one additional bit-addressable I/O port P4 in which the port address is D8H. The Port 4 contains seven bits; P4.0 to P4.3 are only available on 44-pin PLCC/QFP package; P4.6 is the alternate function corresponding to pin $\overline{\text{PSEN}}$. When program is running in the internal memory without any access to external memory, PSEN may be individually configured to the alternate functions P4.6 that serve as general purpose I/O pins. To enable I/O port P4.6, the bit EP6 in the POR register must be set. During reset, the, $\overline{\text{PSEN}}$ perform as in the standard 80C32. The alternate functions P4.6 must be enabled by software. Care must be taken with the ALE pins when configured as the alternate functions.

5.4.1 Port 4

Bit:	7	6	5	4	3	2	1	0
	-	P4.6	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: D8H

5.5 Interrupt System

The W78L812 has fourteen interrupt sources: $\overline{INT0}$ and $\overline{INT1}$; Timer 0,1 and 2; Serial Port; INT2 to INT9. Each interrupt vectors to a specific location in program memory for its interrupt service routine. Each of these sources can be individually enabled or disabled by setting or clearing the corresponding bit in Special Function Register IE0 and IE1. The individual interrupt priority level depends on the Interrupt Priority Register IP0 and IP1. Additional external interrupts INT2 to INT9 are level sensitive and may be used to awake the device from power down mode. The Port 1 interrupts can be initialized to either active HIGH or LOW via setting the Interrupt Polarity Register IX. The IRQ register contains the flags of Port 1 interrupts. Each flag in IRQ register will be set when a interrupt request is recognized but *must be cleared by software*. Note that the interrupt flags have to be cleared before the interrupt service routine is completed, or else another interrupt will be generated.

5.5.1 Interrupt Enable Register 0

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8H

EA : Global enable. Enable/disable all interrupts.

ET2: Enable Timer 2 interrupt.

ES : Enable Serial Port interrupt.

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

5.5.2 Interrupt Enable Register 1

Bit:	7	6	5	4	3	2	1	0
	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Mnemonic: IE1 Address: E8H

EX9: Enable external interrupt 9 Note: 0 = interrupt disabled, 1 = interrupt enabled.

EX8: Enable external interrupt 8

EX7: Enable external interrupt 7

EX6: Enable external interrupt 6

EX5: Enable external interrupt 5

EX4: Enable external interrupt 4

EX3: Enable external interrupt 3

EX2: Enable external interrupt 2

5.5.6 Interrupt Request Flag Register

Bit:	7	6	5	4	3	2	1	0
	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Mnemonic: IRQ Address: C0H

IQ9: External interrupt 9 request flag.
IQ8: External interrupt 8 request flag.
IQ7: External interrupt 7 request flag.
IQ6: External interrupt 6 request flag.
IQ5: External interrupt 5 request flag.
IQ4: External interrupt 4 request flag.
IQ3: External interrupt 3 request flag.
IQ2: External interrupt 2 request flag.

Table.1 Priority level for simultaneous requests of the same priority interrupt sources

SOURCE	FLAG	PRIORITY LEVEL	VECTOR ADDRESS
External Interrupt 0	IE0	(Highest)	0003H
Serial Port	RI + TI		0023H
External Interrupt 5	IQ5		0053H
Timer 0 Overflow	TF0		000BH
External Interrupt 6	IQ6		005BH
External Interrupt 1	IE1		0013H
External Interrupt 2	IQ2		003BH
External Interrupt 7	IQ7		0063H
Timer 1 Overflow	TF1		001BH
Timer 2 Overflow	TF2 + EXF2		002BH
External Interrupt 3	IQ3		0043H
External Interrupt 8	IQ8		006BH
External Interrupt 4	IQ4		004BH
External Interrupt 9	IQ9	(Lowest)	0073H

5.6 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

5.6.1 Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

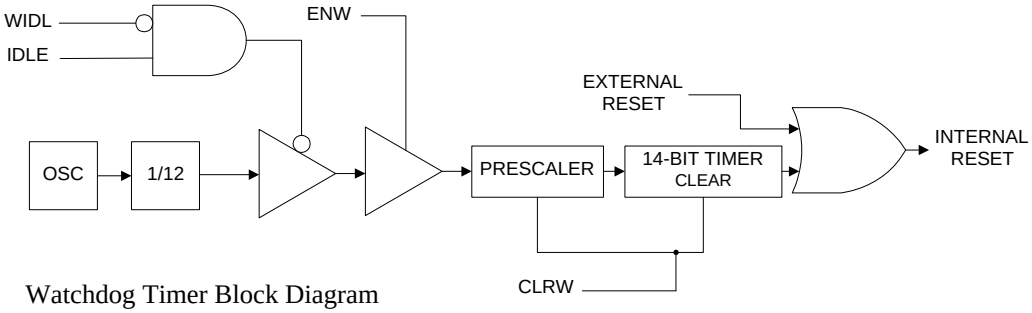
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2 – 0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 1 0	4
0 0 1	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

The time-out period is obtained using the following equation:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 1 0	39.32 mS
0 0 1	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57 mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

5.7 Clock

The W78L812 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L812 relatively insensitive to duty cycle variations in the clock. The W78L812 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

5.8 Power Management

5.8.1 Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

5.8.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator.

5.9 AUXR - Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

Mnemonic: AUXR Address: 8Eh

AO: Turn off ALE signal.

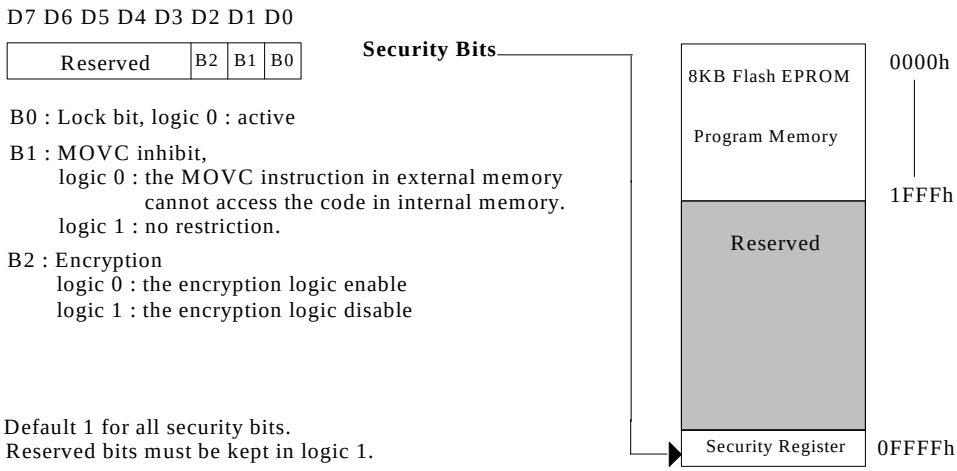
5.10 Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

5.11 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L812 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.



Special Setting Register

6.8.1 Lock Bit

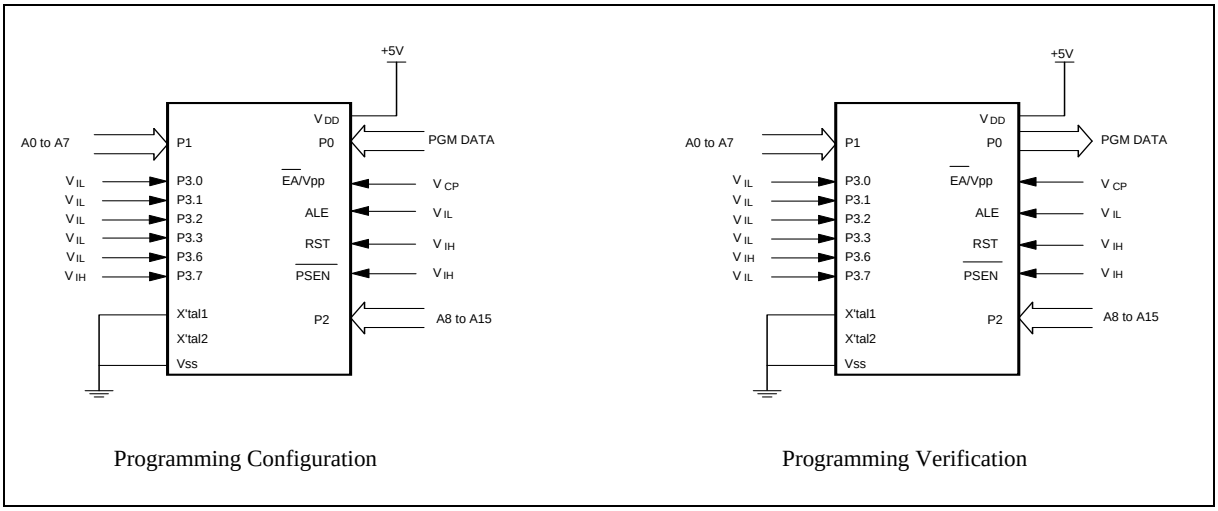
This bit is used to protect the customer's program code in the W78L812. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the on-chip ROM data and Special Setting Registers can not be accessed again.

6.8.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

6.8.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



7. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	VIN	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_a	0	70	°C
Storage Temperature	TST	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Output					
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA
Output Low Voltage P3[*6]	V_{OL3}	-	0.22	V	V_{DD} = 4.5V, I_{OL} = +2 mA
Sink current P1, P2, P3[5], P4<0:4>	I_{SK1}	4	12	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		1.8	5.4	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P0, ALE, $\overline{PSEN}$, P4.6	I_{SK2}	10	18	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
		4.5	9	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Sink current P3.4 to P3.7 in High-Drive mode	I_{SK3}	12	24	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, V_{OH} = -100 μA
		1.4	-	V	V_{DD} = 2.4V, V_{OH} = -20 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source current P1, P2, P3, P4<0:4>	I_{SR1}	-120	-250	μA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-20	-40	μA	V_{DD} = 2.4V, V_{OH} = 1.4V
Source current P0, ALE, $\overline{PSEN}$, P4.6	I_{SR2}	-10	-14	mA	V_{DD} = 4.5V, V_{OH} = 2.4V
		-1.9	-3.3	mA	V_{DD} = 2.4V, V_{OH} = 1.4V

Notes:

*1. RST pin has an internal pull-down.

*2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.

*3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.

*4. P0, P2, ALE and $\overline{PSEN}$ are tested in the external access mode.

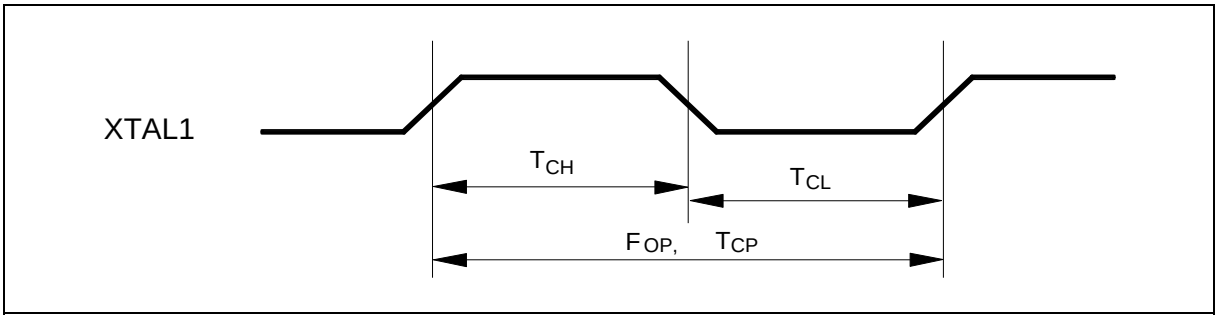
*5. P3.4 to P3.7 are in normal mode.

*6. P3 (P3.4 – P3.7) is used LED driver port by set SFR.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

9.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	20	MHz	1
Clock Period	T_{CP}	50	-	-	nS	2
Clock High	T_{CH}	25	-	-	nS	3
Clock Low	T_{CL}	25	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

9.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 T_{CP}	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 T_{CP}	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

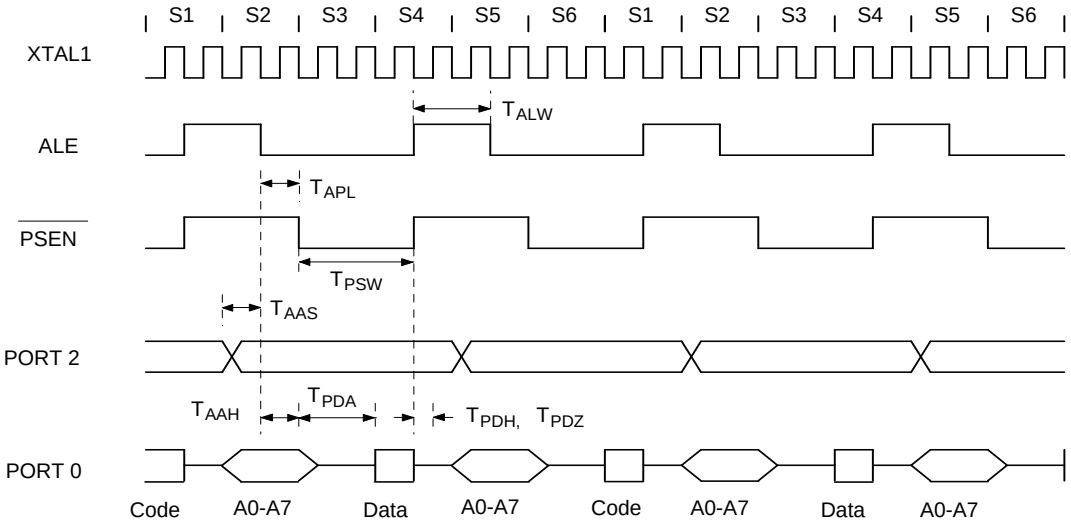
9.6 Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{PP} Setup Time	T_{VPS}	2.0	-	-	µS
Data Setup Time	T_{DS}	2.0	-	-	µS
Data Hold Time	T_{DH}	2.0	-	-	µS
Address Setup Time	T_{AS}	2.0	-	-	µS
Address Hold Time	T_{AH}	0	-	-	µS
$\overline{CE}$ Program Pulse Width for Program Operation	T_{PWP}	290	300	310	µS
OECTRL Setup Time	T_{OCS}	2.0	-	-	µS
OECTRL Hold Time	T_{OCH}	2.0	-	-	µS
$\overline{OE}$ Setup Time	T_{OES}	2.0	-	-	µS
$\overline{OE}$ High to Output Float	T_{DFP}	0	-	130	nS
Data Valid from $\overline{OE}$	T_{OEV}	-	-	150	nS

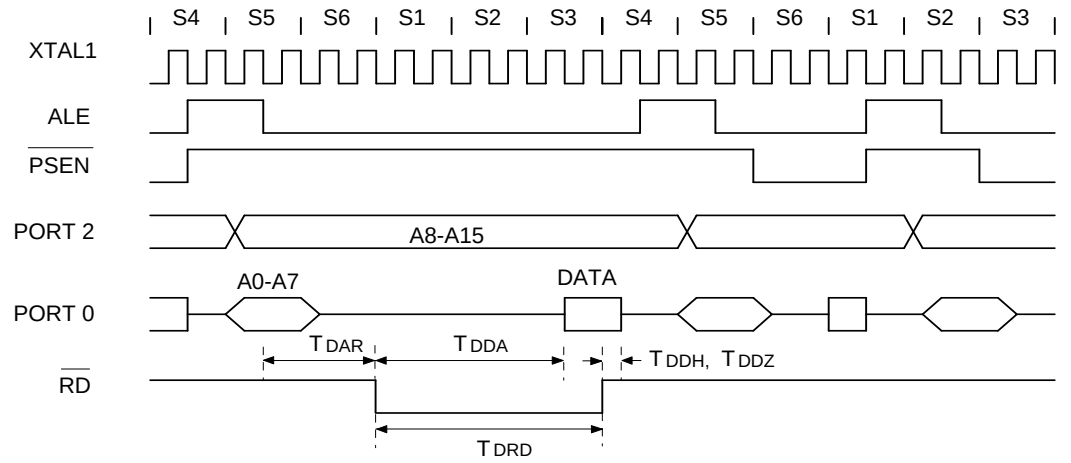
Note: Flash data can be accessed only in flash mode. The RST pin must pull in V_{IH} status, the ALE pin must pull in V_{IL} status, and the $\overline{PSEN}$ pin must pull in V_{IH} status.

10. TIMING WAVEFORMS

10.1 Program Fetch Cycle



10.2 Data Read Cycle



11. TYPICAL APPLICATION CIRCUITS

11.1 Expanded External Program Memory and Crystal

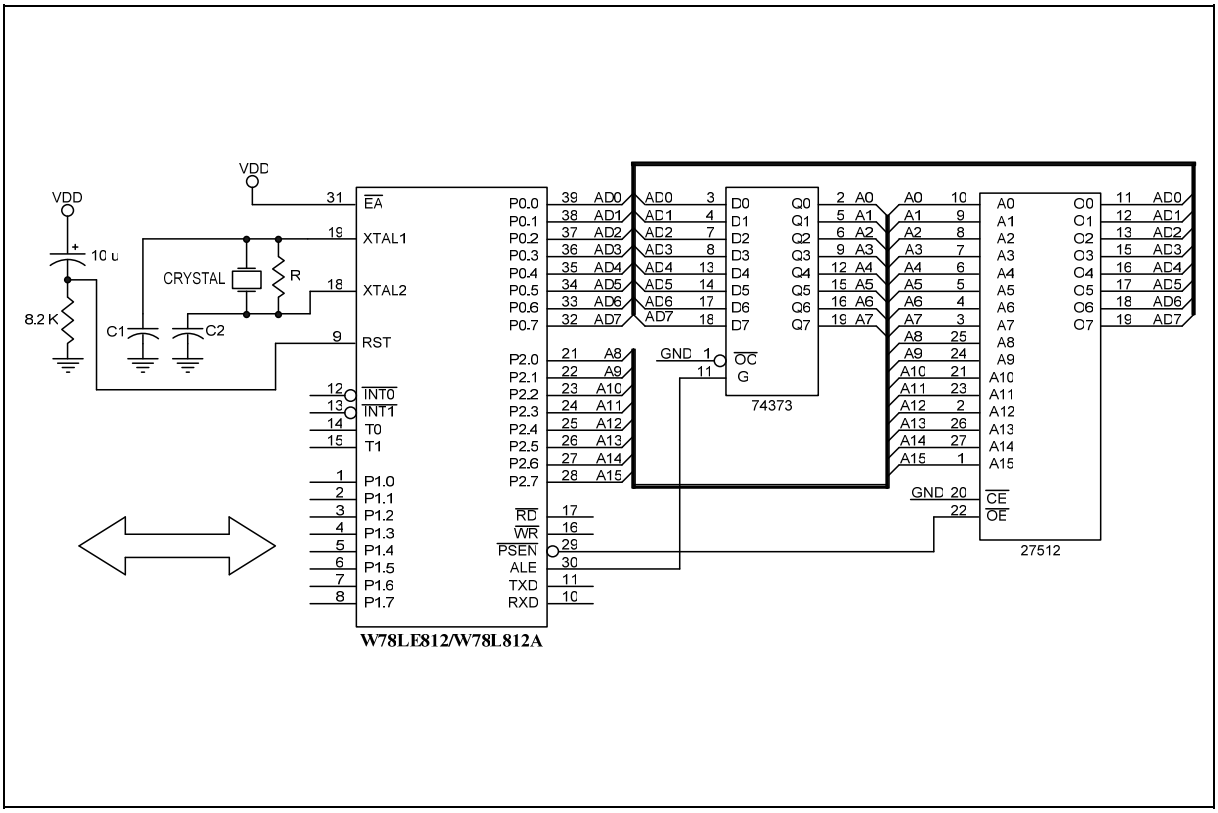


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
20 MHz	15P	15P	-

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Typical Application Circuits, continued

11.2 Expanded External Data Memory and Oscillator

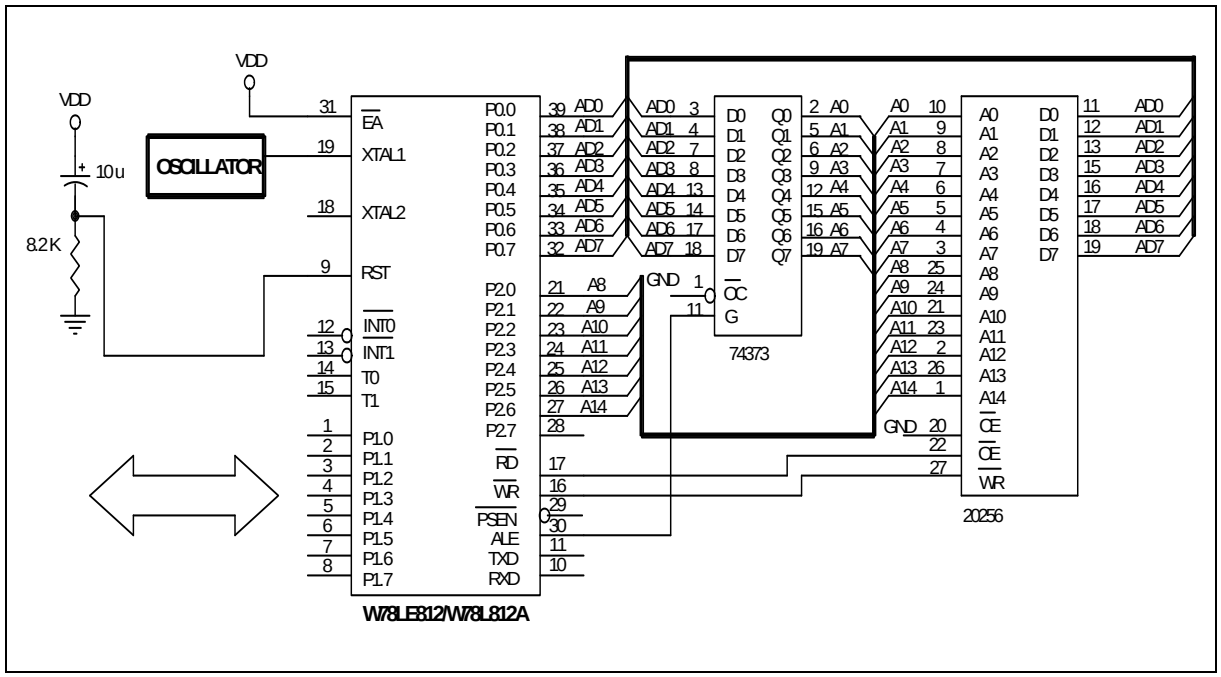
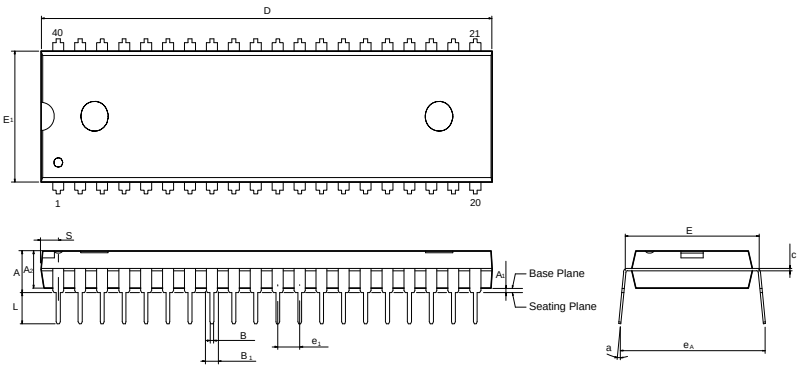


Figure B

12. PACKAGE DIMENSIONS

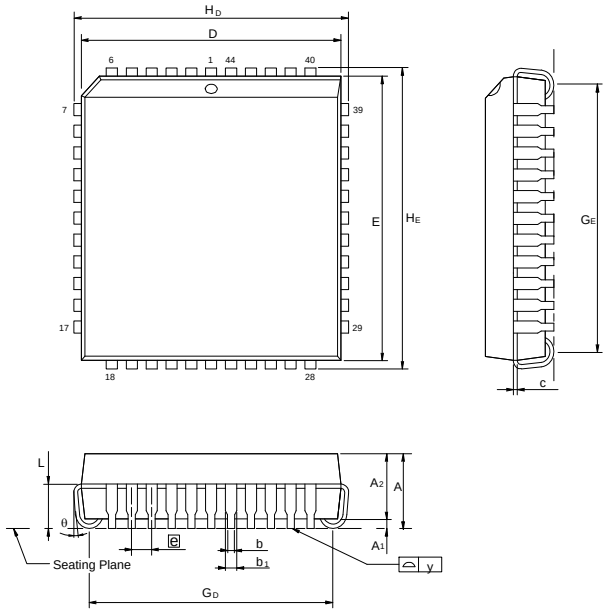
12.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

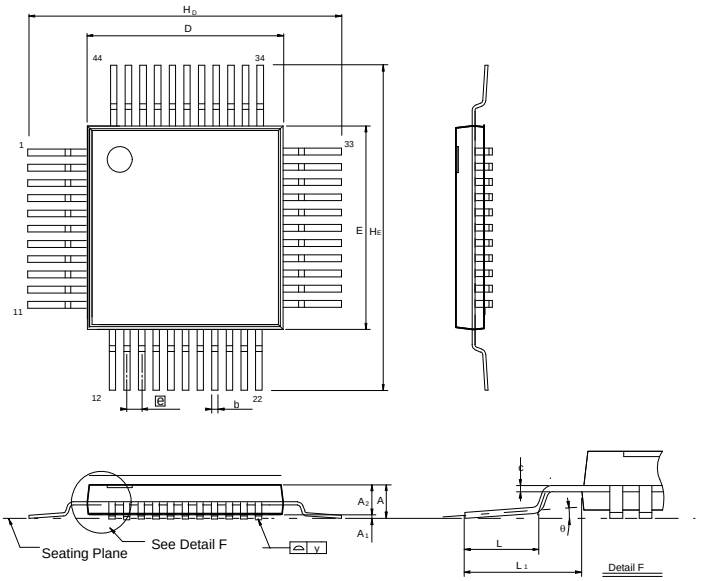
12.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

12.3 44-pin PQFP

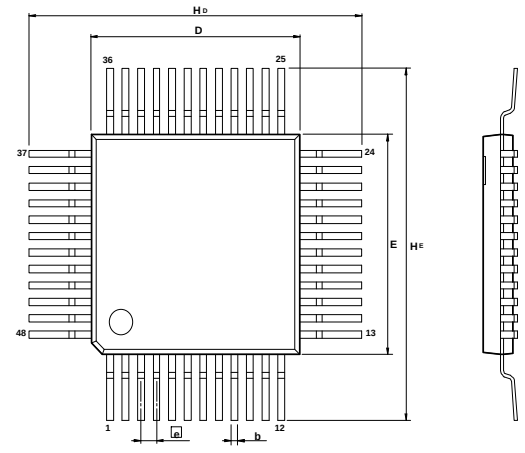


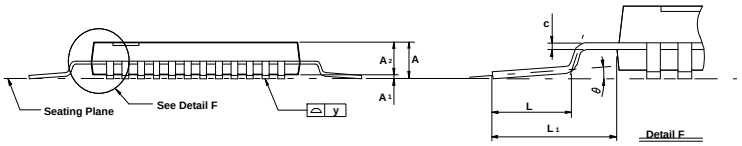
Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

12.4 48-pin LQFP





Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	---	---	1.60
A_1	0.05	---	0.15
A_2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	---	0.20
D		7.00	
E		7.00	
e		0.50	
H_D		9.00	
H_E		9.00	
L	0.45	0.60	0.75
L_1		1.00	
y	---	0.08	---
θ	0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.