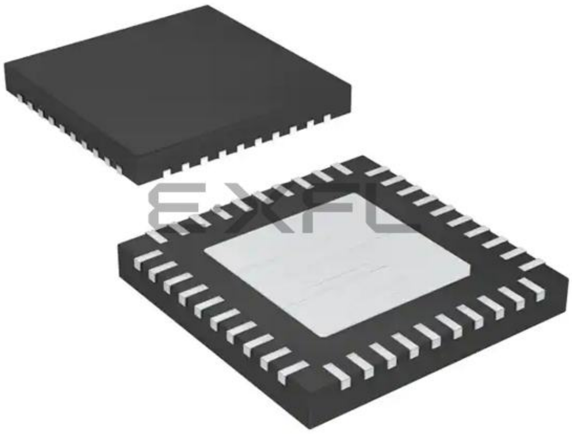
Analog Devices Inc./Maxim Integrated - MAXQ610B-0000+ Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq610b-0000

LIST OF FIGURES

LIST OF TABLES

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} with Respect to GND ....-0.3V to +3.6V
Voltage Range on Any Lead with Respect
to GND except V_{DD} ....-0.3V to (V_{DD} + 0.5V)
Continuous Power Dissipation (Multilayer Board, T_A = +70°C)
32 TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
40 TQFN (derate 35.7mW/°C above +70°C) 2963mW
44 TQFN (derate 37mW/°C above +70°C) 2758.6mW
Operating Temperature Range...............................0°C to +70°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			V_{RST}		3.6	V
1.8V Internal Regulator	V_{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply (Notes 2, 3)	V_{PFW}	Monitors V_{DD}		1.75	1.8	1.85	V
Power-Fail Reset Voltage (Note 4)	V_{RST}	Monitors V_{DD}		1.64	1.67	1.70	V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}		1.0		1.42	V
RAM Data-Retention Voltage	V_{DRV}	(Note 5)		1.0			V
Active Current (Note 6)	I_{DD_1}	Sysclk = 12MHz			3.75	5.1	mA
Stop-Mode Current	I_{S1}	Power-Fail Off	T_A = +25°C		0.2	2.0	µA
			T_A = 0°C to +70°C		0.2	12	
	I_{S2}	Power-Fail On	T_A = +25°C		22	29.5	
			T_A = 0°C to +70°C		27.6	42	
Current Consumption During Power-Fail	I_{PFR}	(Notes 5, 7)			[(3 x I_{S2}) + ((PCI - 3) x (I_{S1} + I_{NANO}))]/PCI		µA
Power Consumption During Power-On Reset	I_{POR}	(Note 8)			100		nA
Stop-Mode Resume Time	t_{ON}				375 + 8192t_{HFXIN}		µs
Power-Fail Monitor Startup Time	t_{PRM_ON}	(Note 5)				150	µs
Power-Fail Warning Detection Time	t_{PFW}	(Notes 5, 9)		10			µs
Input Low Voltage for IRTX, IRRX, $\overline{\text{RESET}}$, and All Port Pins	V_{IL}			V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRTX, IRRX, $\overline{\text{RESET}}$, and All Port Pins	V_{IH}			0.7 x V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}				300		mV
Input Low Voltage for HFXIN	V_{IL_HFXIN}			V_{GND}		0.3 x V_{DD}	V

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for HFXIN	V_{IH_HFXIN}		0.7 x V_{DD}		V_{DD}	V
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for IRTX	V_{OL_IRTX}	V_{DD} = 3.6V, I_{OL} = 25mA (Note 5)			1.0	V
		V_{DD} = 2.35V, I_{OL} = 10mA (Note 5)			1.0	
		V_{DD} = 1.85V, I_{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{\text{RESET}}$ and All Port Pins (Note 10)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA (Note 5)		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA (Note 5)		0.4	0.5	
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5		V_{DD}	V
Input/Output Pin Capacitance for All Port Pins	C_{IO}	(Note 5)			15	pF
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{\text{RESET}}$, IRTX, IRRX, and All Port Pins	R_{PU}	V_{DD} = 3.0V, V_{OL} = 0.4V (Note 5)	16	28	39	kΩ
		V_{DD} = 2.0V, V_{OL} = 0.4V	17	30	41	
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f_{HFXIN}		1		12	MHz
Crystal/Resonator Period	t_{HFXIN}			1/f_{HFXIN}		ns
Crystal/Resonator Warmup Time	t_{XTAL_RDY}	From initial oscillation		8192 x t_{HFXIN}		ms
Oscillator Feedback Resistor	R_{OSCF}	(Note 5)	0.5	1.0	1.5	MΩ
EXTERNAL CLOCK INPUT						
External Clock Frequency	f_{XCLK}		DC		12	MHz
External Clock Period	t_{XCLK}			1/f_{XCLK}		ns
External Clock Duty Cycle	t_{XCLK_DUTY}		45		55	%
System Clock Frequency	f_{CK}			f_{HFIN}		MHz
		HFXOUT = GND		f_{XCLK}		
System Clock Period	t_{CK}			1/f_{CK}		MHz
NANOPOWER RING OSCILLATOR						
Nanopower Ring Oscillator Frequency	f_{NANO}	T_A = +25°C	3.0	8.0	20.0	kHz
		T_A = +25°C, V_{DD} = POR voltage (Note 5)	1.7	2.4		
Nanopower Ring Oscillator Duty Cycle	t_{NANO}	(Note 5)	40		60	%
Nanopower Ring Oscillator Current	I_{NANO}	Typical at V_{DD} = 1.64V, T_A = +25°C (Note 5)		40	400	nA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65{,}535/f_{NANO}$	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$		6			MHz
Flash Erase Time	t_{ME}	Mass erase	20		40	ms
	t_{ERASE}	Page erase	20		40	
Flash Programming Time per Word	t_{PROG}	(Note 11)	20		100	µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years
IR						
Carrier Frequency	f_{IR}	(Note 5)			$f_{CK}/2$	Hz

Note 1: Specifications to 0°C are guaranteed by design and are not production tested.

Note 2: It is not recommended to write to flash memory when the supply voltage drops below the power-fail warning levels as there is uncertainty in the duration of continuous power supply. The user application should check the status of the power-fail warning flag before writing to flash to ensure complete write operations.

Note 3: The power-fail warning monitor and the power-fail reset monitor track each other with a minimum delta between the two of 0.11V.

Note 4: The power-fail reset and power-on-reset (POR) detectors operate in tandem to ensure that one or both signals are active at all times when $V_{DD} < V_{RST}$. Doing so ensures the device maintains the reset state until the minimum operating voltage is achieved.

Note 5: Guaranteed by design and not production tested.

Note 6: Measured on the V_{DD} pin and the part not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. Part is executing code from flash memory.

Note 7: The power-check interval (PCI) can be set to always on, 1024, 2048, or 4096 nanopower ring oscillator clock cycles.

Note 8: Current consumption during POR when powering up while $V_{DD} < V_{POR}$.

Note 9: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected.

Note 10: The maximum total current, I_{OH} (max) and I_{OL} (max), for all listed outputs combined should not exceed 32mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

Note 11: Programming time does not include overhead associated with utility ROM interface.

Pin Description

PIN			NAME	FUNCTION
32 TQFN	40 TQFN	44 TQFN		
		POWER PINS		
15, 29	18, 38	19, 41	V_{DD}	**Supply Voltage**
13, 22, 30	—	17, 20, 28, 42	GND	**Ground.** These pins must be directly connected to the ground plane. The 40-pin TQFN package does not have any ground pins and connects to ground through the exposed pad.
14	17	18	REGOUT	**Regulator Capacitor.** This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.
—	—	—	EP	**Exposed Pad.** For the 32-pin TQFN package, leave unconnected. For the 40-pin TQFN package, the exposed pad is internally connected to GND. Connect to the ground plane. For the 44-pin TQFN package, the EP has no internal connection to the device. Leave unconnected. Not intended as an electrical connection point.
		RESET PINS		
28	37	40	$\overline{\text{RESET}}$	**Digital, Active-Low, Reset Input/Output.** The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
		CLOCK PINS		
18	21	23	HFXIN	**High-Frequency Crystal Input.** Connect external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is unconnected.
19	22	24	HFXOUT	
		IR FUNCTION PINS		
31	39	43	IRTX	**IR Transmit Output.** IR transmit pin capable of sinking 25mA. This pin defaults to high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.
32	40	44	IRRX	**IR Receive Input.** IR receive pin. This pin defaults to high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.

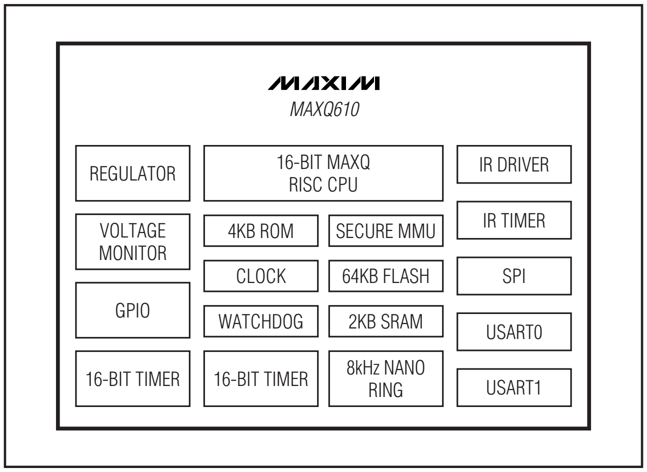
Pin Description (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="5" rowspan="2">FUNCTION</th></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th></tr>
<tr><th colspan="9">GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS</th></tr>
<tr><td rowspan="10">1–8</td><td rowspan="10">1, 3, 5–10</td><td rowspan="10">1, 3, 5–10</td><td rowspan="10">P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, TBA0/TBA1, TBB0/TBB1</td><td colspan="5">General-Purpose, Digital, I/O, Type-C Port. These port pins function as bidirectional I/O pins. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All alternate functions must be enabled from software.</td></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>P0.0</td><td>IRTXM</td></tr>
<tr><td>2</td><td>3</td><td>3</td><td>P0.1</td><td>RX0</td></tr>
<tr><td>3</td><td>5</td><td>5</td><td>P0.2</td><td>TX0</td></tr>
<tr><td>4</td><td>6</td><td>6</td><td>P0.3</td><td>RX1</td></tr>
<tr><td>5</td><td>7</td><td>7</td><td>P0.4</td><td>TX1</td></tr>
<tr><td>6</td><td>8</td><td>8</td><td>P0.5</td><td>TBA0/TBA1</td></tr>
<tr><td>7</td><td>9</td><td>9</td><td>P0.6</td><td>TBB0</td></tr>
<tr><td>8</td><td>10</td><td>10</td><td>P0.7</td><td>TBB1</td></tr>
<tr><td rowspan="10">9–12, 16, 17, 20, 21</td><td rowspan="10">11–14, 19, 20, 23, 24</td><td rowspan="10">11–14, 21, 22, 25, 26</td><td rowspan="10">P1.0–P1.7; INT0–INT7</td><td colspan="5">General-Purpose, Digital, I/O, Type-D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All interrupt functions must be enabled from software.</td></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>9</td><td>11</td><td>11</td><td>P1.0</td><td>INT0</td></tr>
<tr><td>10</td><td>12</td><td>12</td><td>P1.1</td><td>INT1</td></tr>
<tr><td>11</td><td>13</td><td>13</td><td>P1.2</td><td>INT2</td></tr>
<tr><td>12</td><td>14</td><td>14</td><td>P1.3</td><td>INT3</td></tr>
<tr><td>16</td><td>19</td><td>21</td><td>P1.4</td><td>INT4</td></tr>
<tr><td>17</td><td>20</td><td>22</td><td>P1.5</td><td>INT5</td></tr>
<tr><td>20</td><td>23</td><td>25</td><td>P1.6</td><td>INT6</td></tr>
<tr><td>21</td><td>24</td><td>26</td><td>P1.7</td><td>INT7</td></tr>
</table>

Pin Description (continued)

<table>
<tr><th colspan="2">PIN</th><th></th><th rowspan="2">NAME</th><th colspan="5" rowspan="2">FUNCTION</th></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th></tr>
<tr><td rowspan="10">24–27</td><td rowspan="10">25, 26,
29–32,
35, 36</td><td rowspan="10">27, 29,
32–35,
38, 39</td><td rowspan="10">P2.0–
P2.7;
MOSI,
MISO,
SCLK,
$\overline{\text{SSEL}}$,
TCK, TDI,
TMS,
TDO</td><td colspan="5">**General-Purpose, Digital, I/O, Type-C Port.** These port pins function as bidirectional I/O pins. P2.0–P2.3 default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All alternate functions must be enabled from software. Enabling the pin’s special function disables the general-purpose I/O on the pin.
The JTAG pins (P2.4–P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP’s Shift_IR or Shift_DR states.</td></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>25</td><td>27</td><td>P2.0</td><td>MOSI</td></tr>
<tr><td>—</td><td>26</td><td>29</td><td>P2.1</td><td>MISO</td></tr>
<tr><td>—</td><td>29</td><td>32</td><td>P2.2</td><td>SCLK</td></tr>
<tr><td>—</td><td>30</td><td>33</td><td>P2.3</td><td>$\overline{\text{SSEL}}$</td></tr>
<tr><td>24</td><td>31</td><td>34</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>25</td><td>32</td><td>35</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>26</td><td>35</td><td>38</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>27</td><td>36</td><td>39</td><td>P2.7</td><td>TDO</td></tr>
<tr><td rowspan="10">—</td><td rowspan="10">2, 4, 15,
16, 27,
28, 33, 34</td><td rowspan="10">2, 4, 15,
16, 30,
31, 36,
37</td><td rowspan="10">P3.0–
P3.7;
INT8–
INT15</td><td colspan="5">**General-Purpose, Digital, I/O, Type-D Port; External Edge-Selectable Interrupt.** These port pins function as bidirectional I/O pins or as interrupts. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All interrupt functions must be enabled from software.</td></tr>
<tr><th>32 TQFN</th><th>40 TQFN</th><th>44 TQFN</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>2</td><td>2</td><td>P3.0</td><td>INT8</td></tr>
<tr><td>—</td><td>4</td><td>4</td><td>P3.1</td><td>INT9</td></tr>
<tr><td>—</td><td>15</td><td>15</td><td>P3.2</td><td>INT10</td></tr>
<tr><td>—</td><td>16</td><td>16</td><td>P3.3</td><td>INT11</td></tr>
<tr><td>—</td><td>27</td><td>30</td><td>P3.4</td><td>INT12</td></tr>
<tr><td>—</td><td>28</td><td>31</td><td>P3.5</td><td>INT13</td></tr>
<tr><td>—</td><td>33</td><td>36</td><td>P3.6</td><td>INT14</td></tr>
<tr><td>—</td><td>34</td><td>37</td><td>P3.7</td><td>INT15</td></tr>
<tr><th colspan="9">NO CONNECTION PINS</th></tr>
<tr><td>23</td><td>—</td><td>—</td><td>N.C.</td><td colspan="5">**No Connection.** Reserved for future use. Leave this pin unconnected.</td></tr>
</table>

Block Diagram



Detailed Description

The MAXQ610 microcontroller provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ 16-bit RISC core, 64KB of flash memory, 2KB data RAM, a soft stack, 16 general-purpose registers, and three data pointers. The MAXQ core offers the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Combining lower active-mode current with the MAXQ610 stop-mode current (0.2µA typical) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation, a high-current IR drive pin capable of sinking up to 25mA current, and output pins capable of sinking up to 5mA ideal for IR applications, general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the minimum operating voltage of the microcontroller.

At the heart of the MAXQ610 is the MAXQ 16-bit RISC core. The MAXQ610 operates from DC to 12MHz and almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software resulting in quiescent current consumption of less than 0.2µA typical and 2.0µA maximum. The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The MAXQ610 is based on Maxim's MAXQ core. The MAXQ is a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the MAXQ610 family is implemented as a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit-switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that is important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with automatic increment/decrement support.

Memory

The MAXQ610 incorporates several memory types that include the following:

- 64KB program flash
- 2KB SRAM data memory
- 5.25KB utility ROM
- Soft stack

Table 1. Memory Areas and Associated Maximum Privilege Levels

AREA	PAGE ADDRESS	MAXIMUM PRIVILEGE LEVEL
System	0 to ULDR-1	High
User Loader	ULDR to UAPP-1	Medium
User Application	UAPP to top	Low
Utility ROM	N/A	High
Other (RAM)	N/A	Low

Memory Protection

The optional memory-protection feature separates code memory into three areas: system, user loader, and user application. Code in the system area can be kept confidential. Code in the user areas can be prevented from reading and writing system code. The user loader can also be protected from user application code.

Memory protection is implemented using privilege levels for code. Each area has an associated privilege level. RAM/ROM are assigned privilege levels as well. Refer to the *MAXQ610 User's Guide* for a more thorough explanation of the topic. See Table 1.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and can also be used general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM is a 5.25KB block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include the following:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of system code, or to one of the special routines mentioned. Routines within the utility ROM are user accessible and can be called as subroutines by the application software. More information on the utility ROM functions is contained in the *MAXQ610 User's Guide*.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

Three password locks are provided for protection of up to three different program memory segments. When the PWL is set to 1 (POR default) and the contents of the memory at addresses 0010h to 001Fh are any value other than FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without password. The password is automatically set to all ones following a mass erase.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or ESD upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

Table 2. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (µs)
00	Sysclk/2^{15}	2.7ms	42.7
01	Sysclk/2^{18}	21.9ms	42.7
10	Sysclk/2^{21}	174.7ms	42.7
11	Sysclk/2^{24}	1.4s	42.7

The watchdog timer functions as the source of both the watchdog-timer timeout and the watchdog-timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog-timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 2.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed IR communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of two separate timing entities: a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR Carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR Modulator Time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

$$\text{IR Input Clock } (f_{IRCLK}) = f_{SYS}/2^{IRDIV[1:0]}$$

$$\text{Carrier Frequency } (f_{CARRIER}) = f_{IRCLK}/(IRCAH + IRCAL + 2)$$

$$\text{Carrier High Time} = IRCAH + 1$$

$$\text{Carrier Low Time} = IRCAL + 1$$

$$\text{Carrier Duty Cycle} = (IRCAH + 1)/(IRCAH + IRCAL + 2)$$

During transmission, the IRCA register is latched for each IRV downcount interval and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next, which is illustrated in Figure 1.

Figure 2 illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV downcounter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV downcounter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

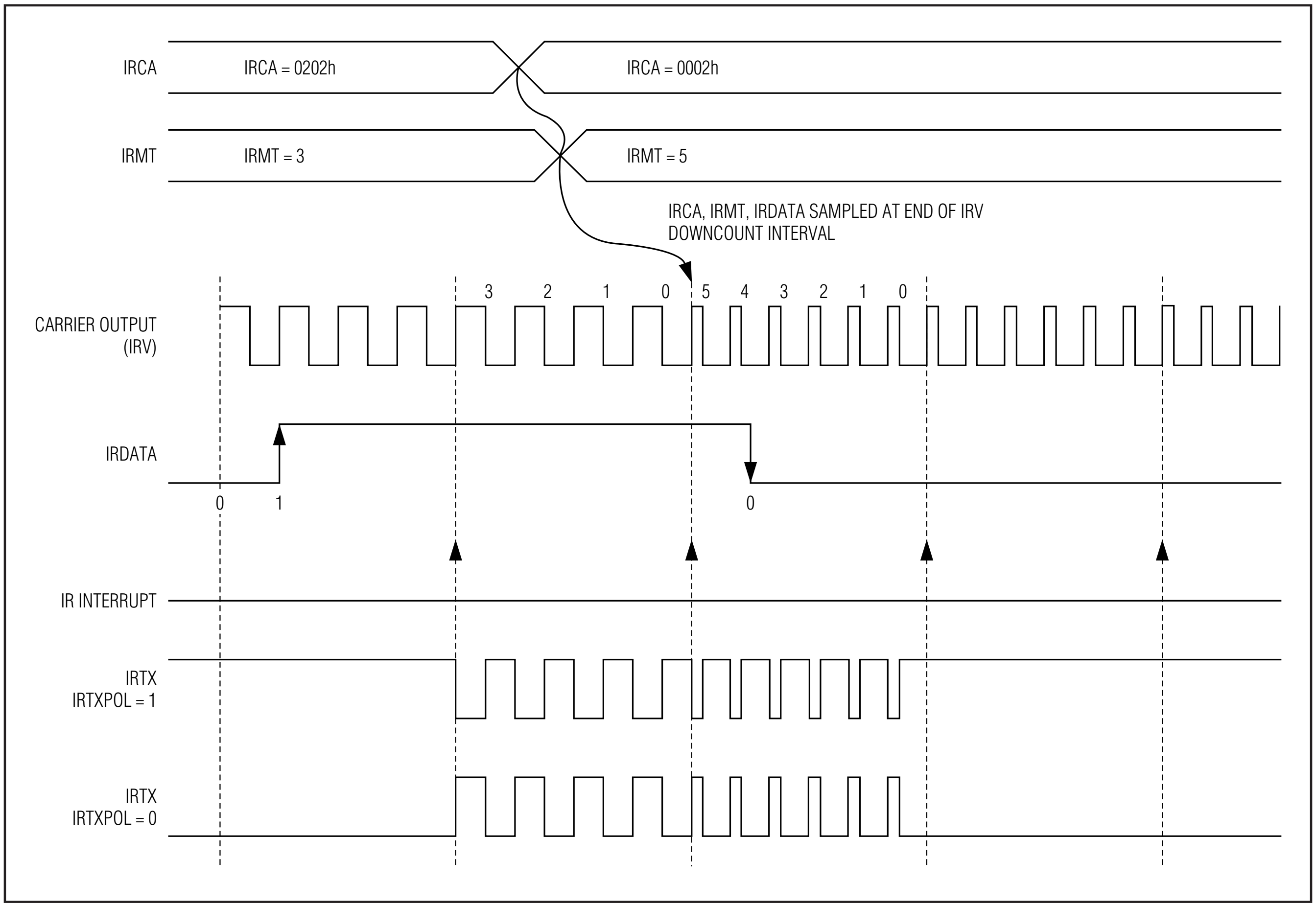


Figure 1. IR Transmit Frequency Shifting Example (IRCFME = 0)

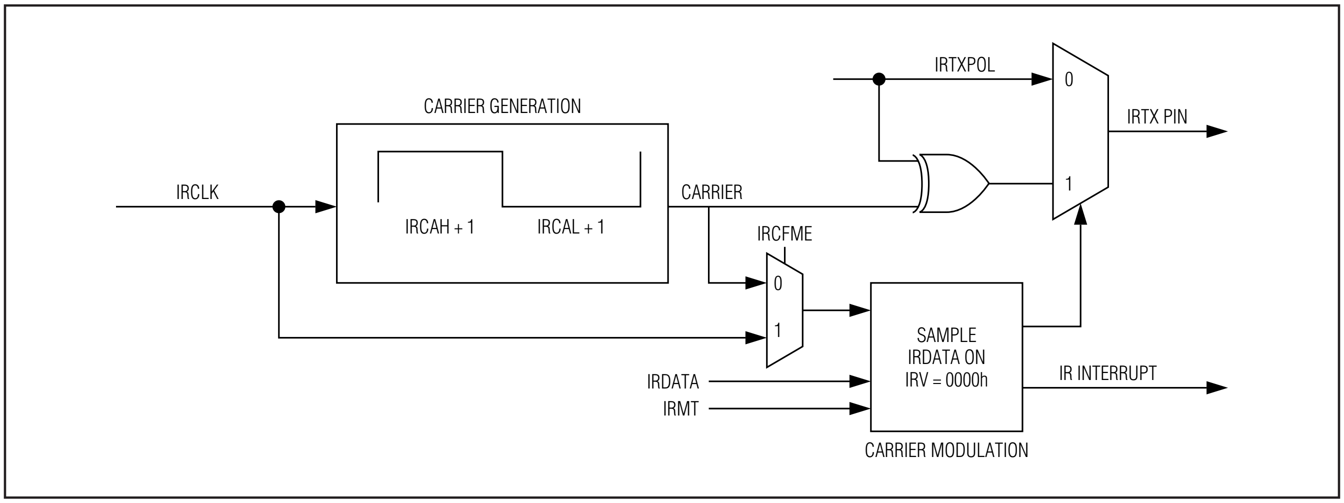


Figure 2. IR Transmit Carrier Generation and Carrier Modulator Control

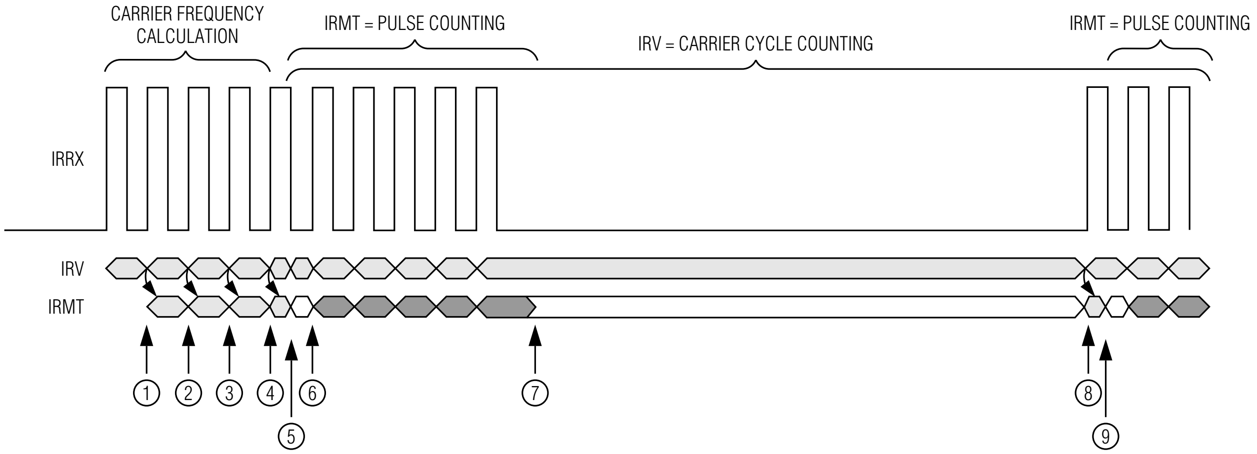
On the next qualified event, the IR module does the following:

1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.
2) Transfers its current IRV value to the IRMT.
3) Resets IRV content to 0000h (if IRXRL = 1).
4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt generated if enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode (IRMODE = 1) or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place.



① TO ④ CAPTURE INTERRUPT (IRIF = 1).
IRV ≥ IRMT.
IRV = 0 (IF IRXRL = 1).

⑤ SOFTWARE SETS IRCA = CARRIER FREQUENCY.
SOFTWARE SETS RXBCNT = 1 (WHICH CLEARS IRMT = 0001 IN HARDWARE).
SOFTWARE CLEARS IRCFME = 0 SO THAT IRV COUNTS CARRIER CYCLES. IRV IS RESET TO 0 ON QUALIFIED EDGE DETECTION IF IRXRL = 1.
SOFTWARE ADDS TO IRMT THE NUMBER OF PULSES USED FOR CARRIER MEASUREMENT.
IRCA x 2x COUNTER FOR SPACE CAN BEGIN IMMEDIATELY (QUALIFIED EDGE RESETS).

⑥ QUALIFIED EDGE DETECTED: IRMT++
IRV RESET TO 0 IF IRXRL = 1.

⑦ IRCA x 2 PERIOD ELAPSES: IRIF = 1; CARRIER ABSENCE = SPACE.
BURST MARK = IRMT PULSES.
SOFTWARE CLEARS RXBCNT = 0 SO THAT WE CAPTURE ON THE NEXT QUALIFIED EDGE.

⑧ QUALIFIED EDGE DETECTED: IRIF = 1, CAPTURE IRV ≥ IRMT AS THE BURST SPACE (PLUS UP TO ONE CARRIER CYCLE).

⑨ SOFTWARE SET RXBCNT = 1 AS IN (5).
CONTINUE (5) TO (8) UNTIL LEARNING SPACE EXCEEDS SOME DURATION. IRV ROLLOVERS CAN BE USED.

Figure 6. Receive Burst-Count Example

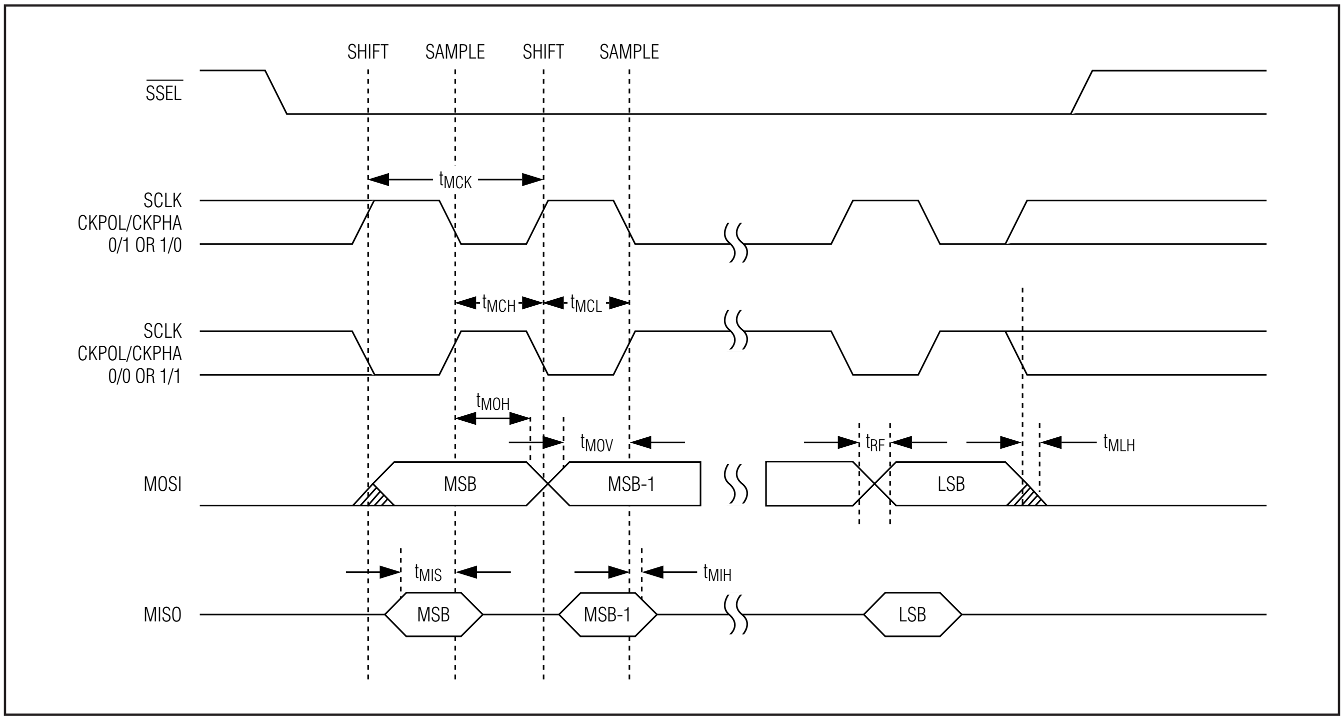


Figure 7. SPI Master Communication Timing

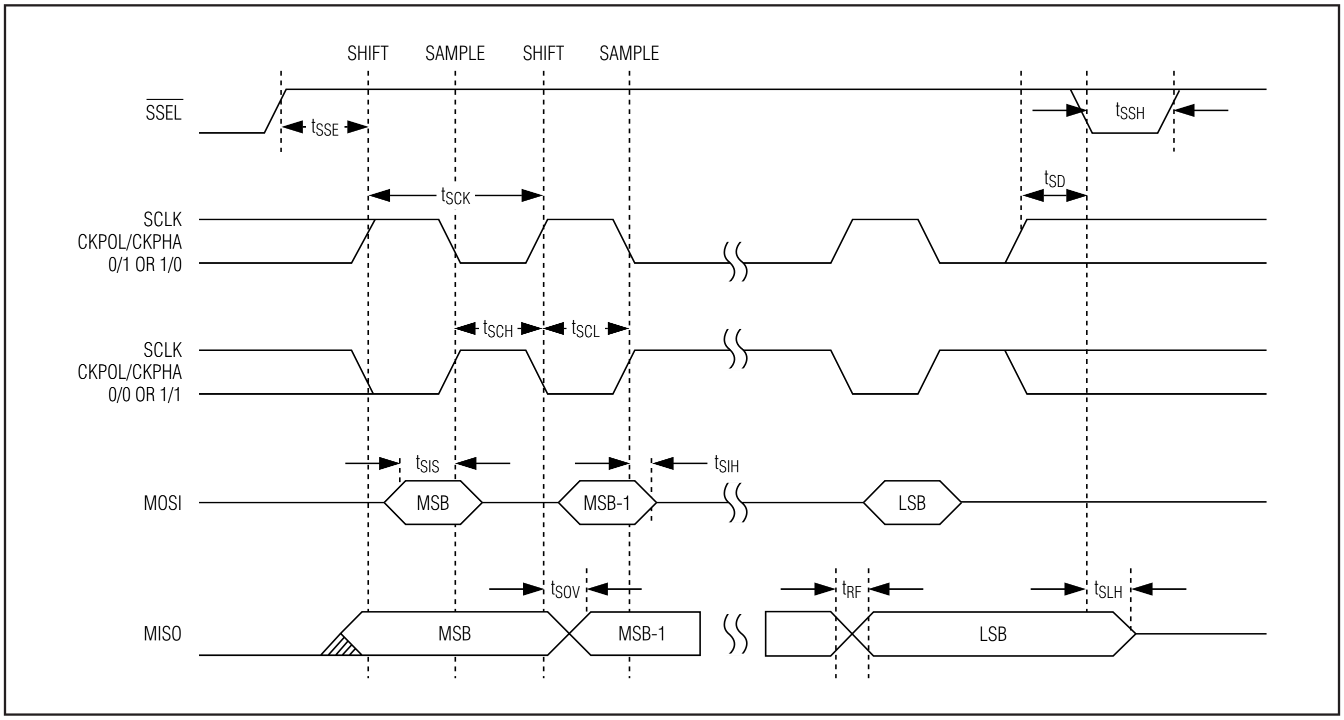


Figure 8. SPI Slave Communication Timing

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT on the MAXQ610, as illustrated in Figure 9.

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors near the oscillator circuitry and connect HFXIN and HFXOUT to ground with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used and should be initially selected based on the load capacitance as suggested by the crystal manufacturer.

ROM Loader

The MAXQ610 includes a ROM loader. The loader denies access to the system, user loader, or user-application memories unless an area-specific password is provided. The ROM loader is not available in ROM-only versions of the MAXQ610.

Loading Flash Memory

An internal bootstrap loader allows the device to be reloaded over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter, such as the MAXQJTAG-001 available from Maxim Integrated Products. If in-system programmability is not required, a commercial gang programmer can be used for mass programming. Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to 1 during reset through the JTAG interface executes the bootstrap-loader-mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

In addition, the ROM loader also enforces the memory-protection policies. 16-word passwords are required to access the ROM loader interface.

Loading memory is not possible for ROM-only versions of the MAXQ610 family.

In-Application Flash Programming

From user-application code, flash can be programmed using the ROM utility functions from either C or assembly language. The function declarations that follow show examples of some of the ROM utility functions provided for in-application flash programming.

```
/* Write one 16-bit word to code address 'dest'.
* Dest must be aligned to 16 bits.
* Returns 0 = failure, 1 = OK.
*/
int flash_write (uint16_t dest, uint16_t data);
```

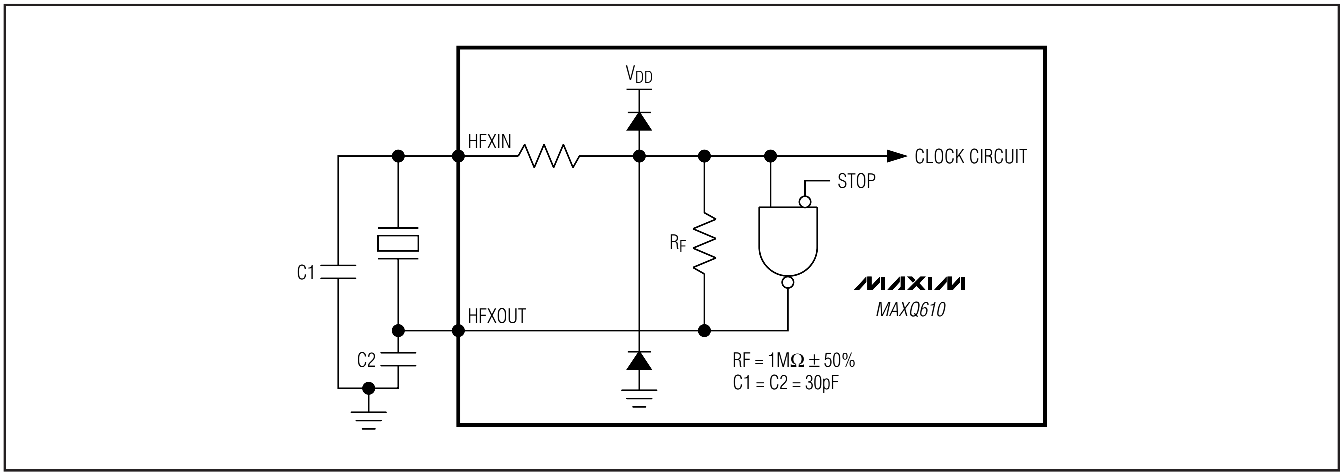


Figure 9. On-Chip Oscillator

To erase, the following function would be used:

```
/* Erase the given Flash page
* addr: Flash offset (anywhere within page)
*/
int flash_erasepage(uint16_t addr);
```

The in-application flash programming must call ROM utility functions to erase and program any of the flash memory. Memory protection is enforced by the ROM utilty functions.

In-application programming is not available in ROM-only versions of the MAXQ610 family.

In-Circuit Debug and JTAG Interface

Embedded debug hardware and software are developed and integrated into the MAXQ610 to provide full in-circuit debugging capability in a user application environment. These hardware and software features include:

- A debug engine.
- A set of registers providing the ability to set breakpoints on register, code, or data using debug service routines stored in ROM.

Collectively, these hardware and software features support two modes of in-circuit debug functionality:

1) Background Mode
    - CPU is executing the normal user program.
    - Allows the host to configure and set up the in-circuit debugger.
2) Debug Mode
    - The debugger takes over the control of the CPU.
    - Read/write accesses to internal registers and memory.
    - Single-step of the CPU for trace operation.

The interface to the debug engine is the TAP controller. The interface allows for communication with a bus master that can either be automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP that is compatible to the JTAG IEEE Std 1149. The TAP provides an independent serial channel to communicate synchronously with the host system.

To prevent unauthorized access of the protected memory regions through the JTAG interface, the debug engine prevents modification of the privilege registers and disallows all access to system memory, unless memory protection is disabled. In addition, all services (such as register display or modification) are denied when code is executing inside the system area.

The debugger is not available for ROM-only versions of the MAXQ610 family.

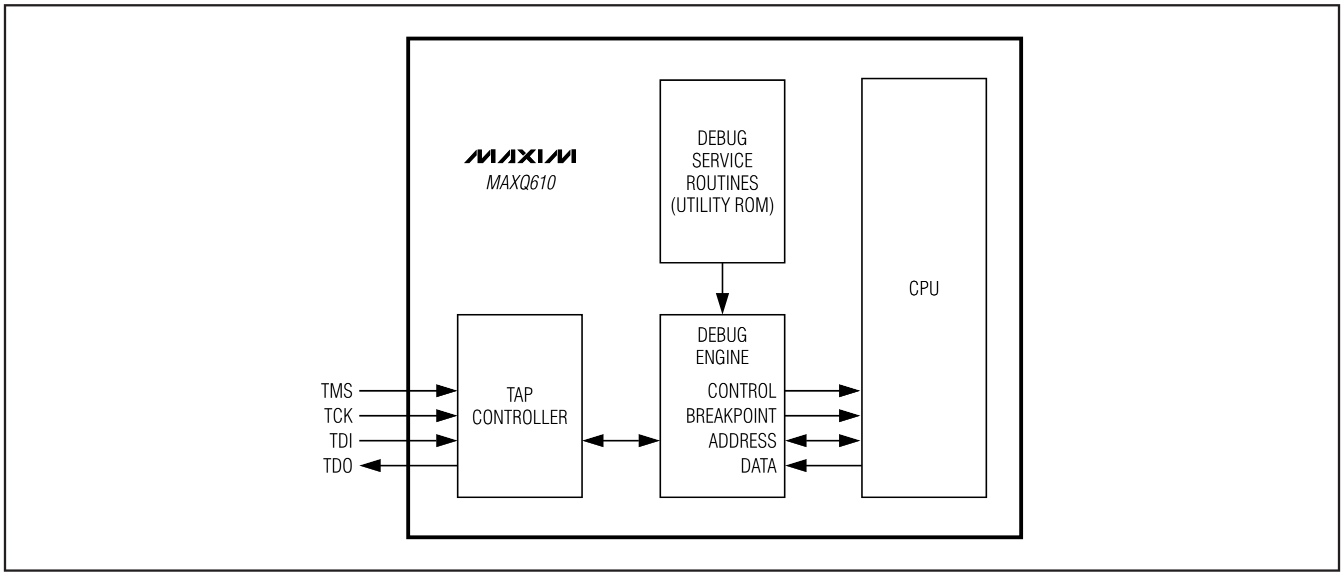


Figure 10. In-Circuit Debugger

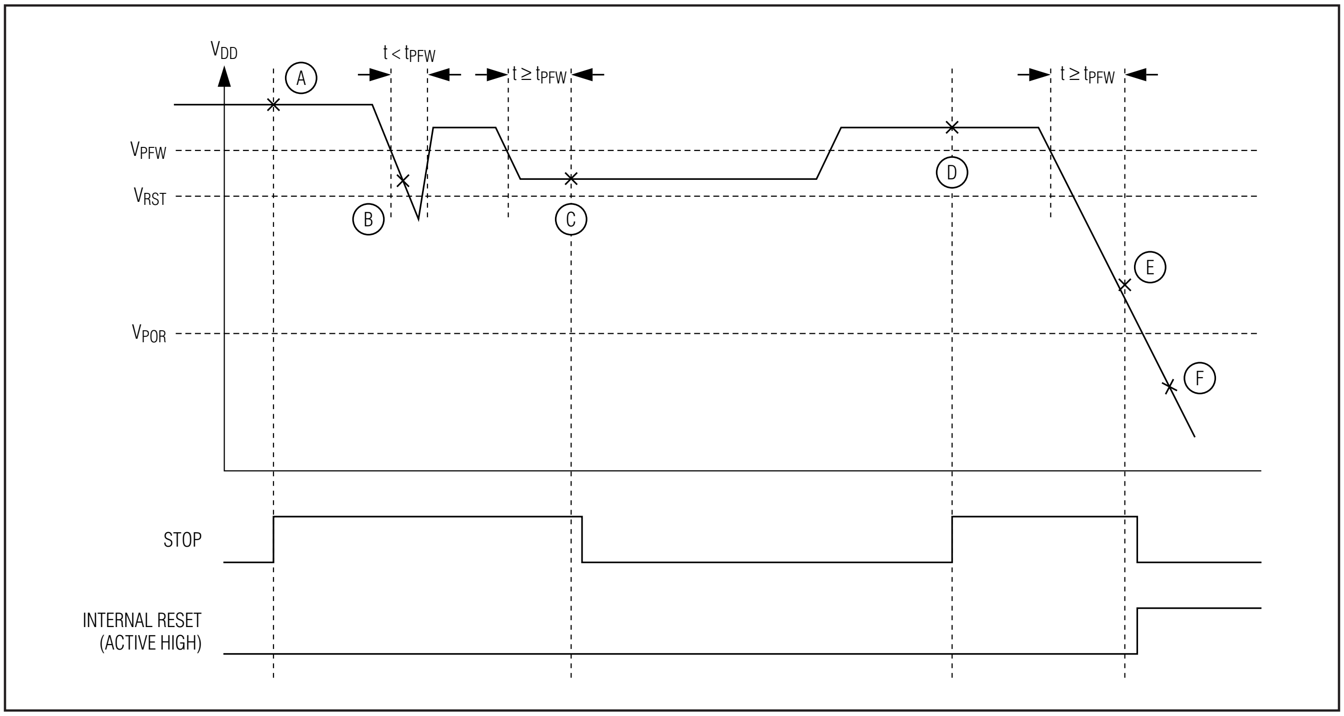


Figure 12. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

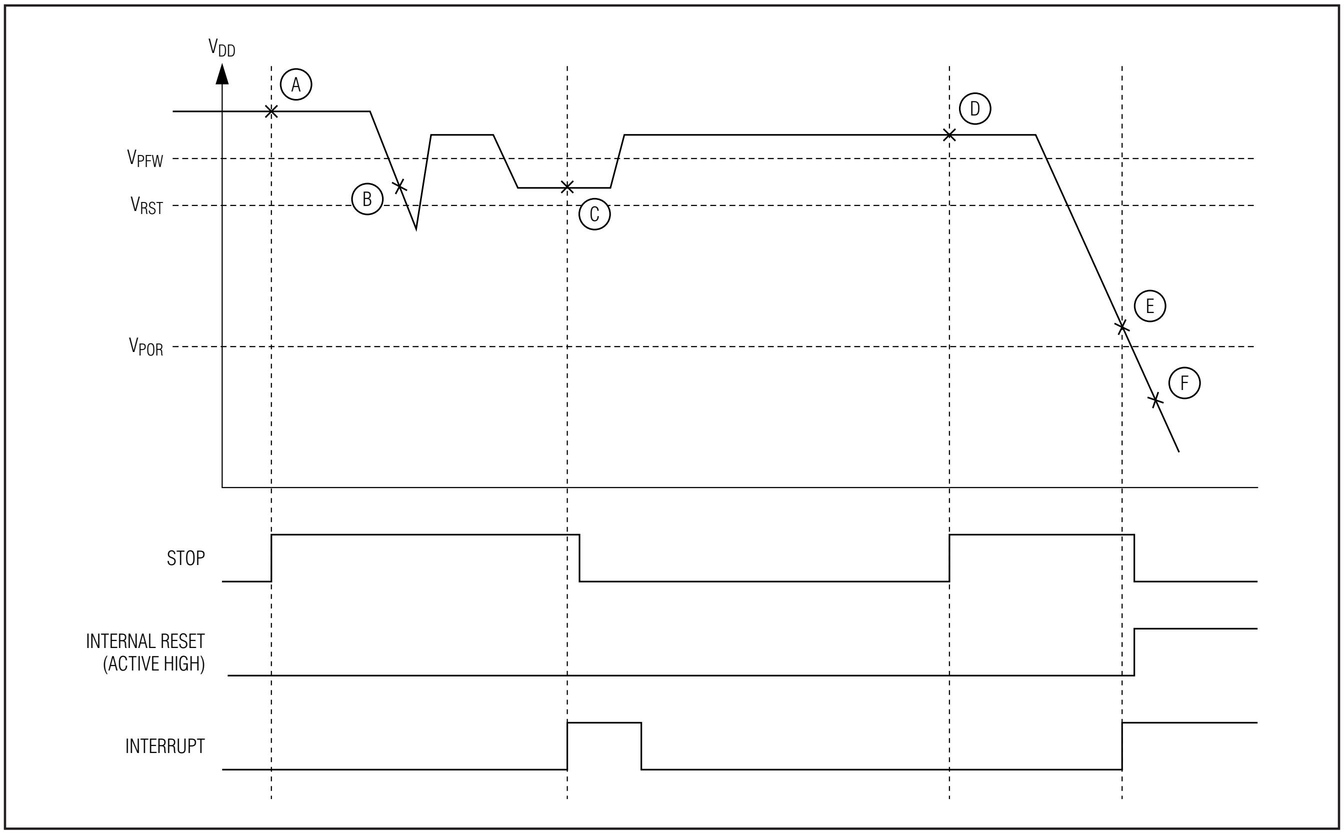


Figure 13. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$ Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Differences for ROM Versions

The ROM-only versions of the MAXQ610 family devices operate in the same manner as their flash counterparts with the following exceptions:

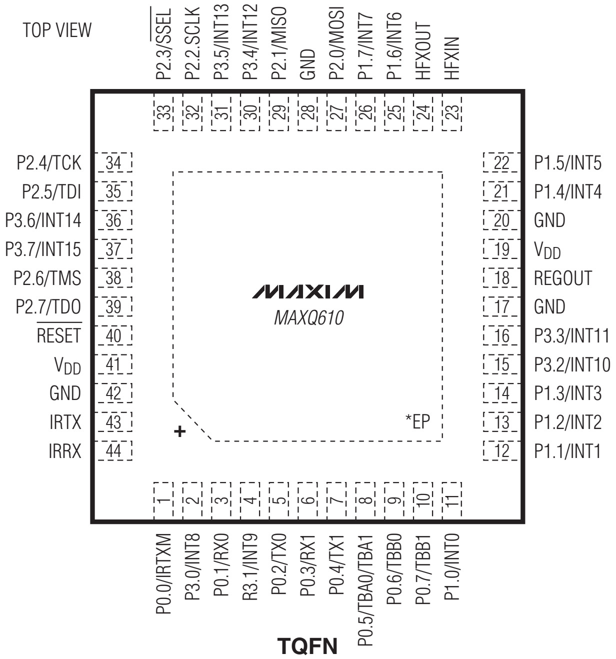
- The ROM loader is not available in the ROM version.
- Loading memory and in-application programming are not supported.
- The debugger is not available in the ROM version.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maxim-ic.com/microcontrollers**.

- This MAXQ610 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ610 revision-specific errata sheet (**www.maxim-ic.com/errata**).
- The *MAXQ610 User's Guide*, which contains detailed information on core features and operation, including programming.

Pin Configurations (continued)



TQFN

*EXPOSED PAD = GND.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	**21-0140**	**90-0001**
40 TQFN-EP	T4066+2	**21-0141**	**90-0053**
44 TQFN-EP	T4477+2	**21-0144**	**90-0127**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	11/08	Removed the Sysclk = 1MHz condition for the Active Current parameter, changed the R_{PU} min values from 18kΩ and 19kΩ to 16kΩ and 17kΩ, and changed the f_{NANO} T_A = +25°C min and max values from 4.2kHz and 14.0kHz to 3.0kHz and 20.0kHz, respectively, in the *Recommended DC Operating Conditions* table	4, 5
		Added the sentence "Software must configure this pin after release from reset to remove the high-impedance input condition." to the IRRX, P0.x, P1.x, P2.x, and P3.x descriptions in the *Pin Description* table	8, 9
2	1/09	Added future status to the 32 TQFN package in the *Ordering Information* table	1
		Changed the REGOUT pin series resistance from 1Ω to 2Ω to 10Ω in the *Pin Description* table	8
3	7/09	Changed the t_{IRRX_A} minimum spec from 200ns to 300ns in the *Recommended DC Operating Conditions* table	5
		Removed the statement about the use of multilayer boards from the *Grounds and Bypassing* section	25
4	10/09	Adjusted the minimum resonator frequency from DCMHz to 1MHz and the minimum programming frequency from 5MHz to 6MHz in the *Recommended DC Operating Conditions* table	5, 6
5	2/10	Added the 44-pin TQFN package	1, 8, 9, 10, 26, 27, 28
6	7/11	Removed future status from the MAXQ610A-0000+ in the *Ordering Information* table; added the continuous power dissipation, lead temperature, and soldering temperature information to the *Absolute Maximum Ratings* section	1, 4