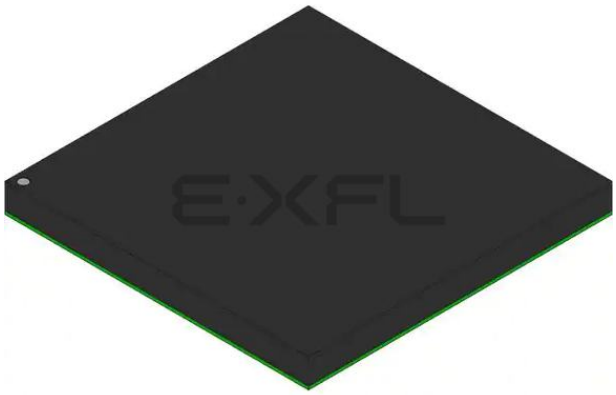

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	708
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k1000cf33c7

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

Table 7. APEX 20KC Device Features (Part 1 of 2)

Feature	APEX 20KC Devices
MultiCore system integration	Full support
Hot-socketing support	Full support
SignalTap logic analysis	Full support
32-/64-bit, 33-MHz PCI	Full compliance
32-/64-bit, 66-MHz PCI	Full compliance in -7 and -8 speed grades in selected devices
MultiVolt I/O	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected bank by bank 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift circuitry LVDS support Up to four PLLs ClockShift clock phase adjustment
Dedicated clock and input pins	Eight

Figure 6. APEX 20KC Carry Chain

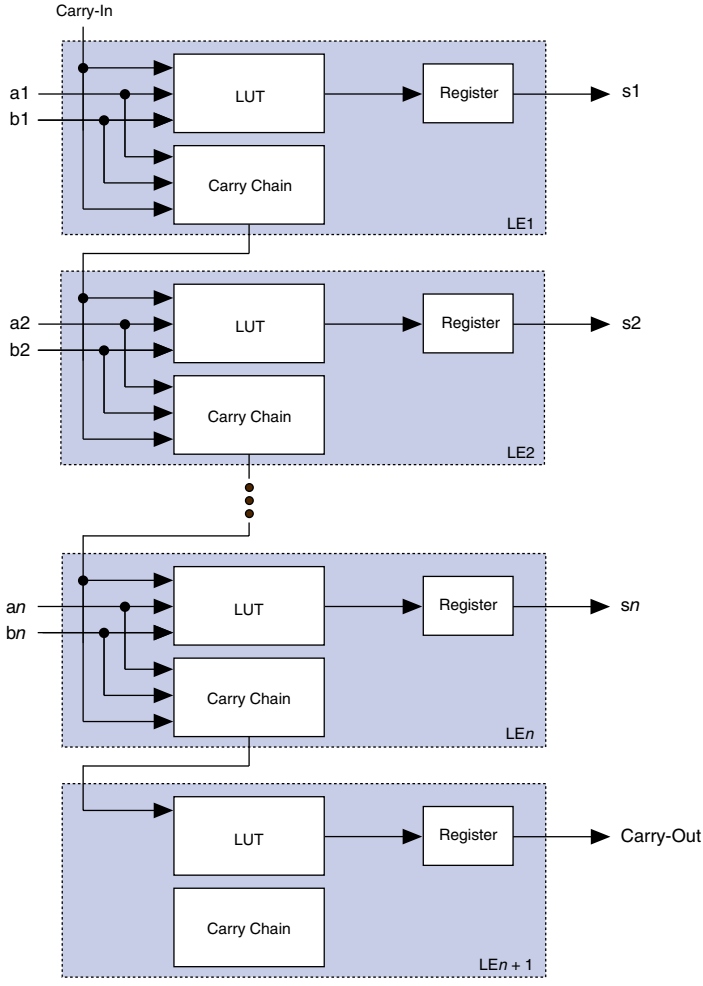
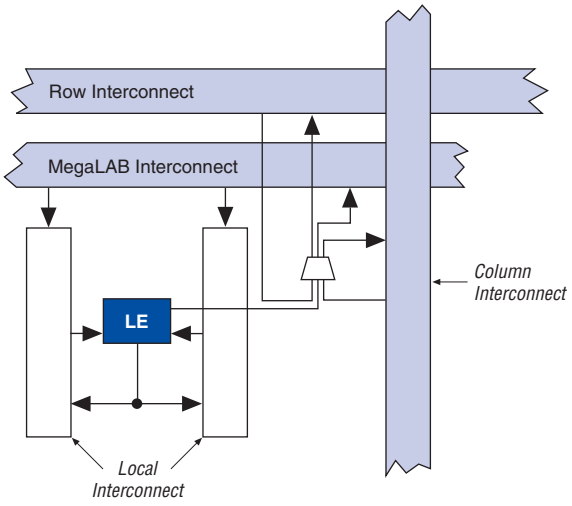


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect

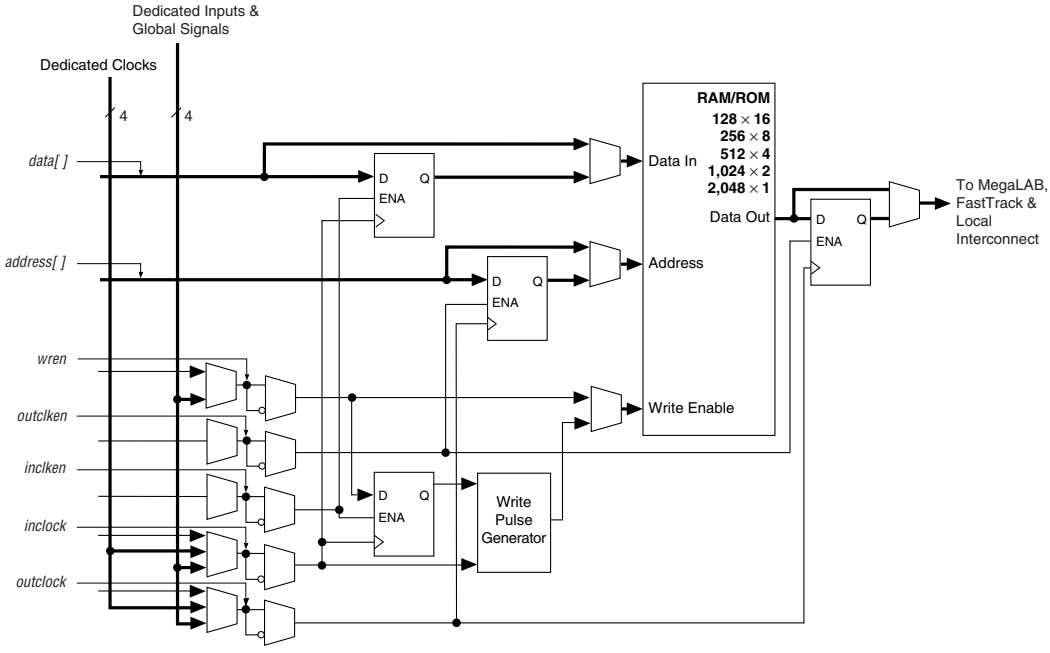


APEX 20KC devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. The FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K400C and larger devices, the FastRow interconnect drives the two MegaLAB structures in the top left corner, the two MegaLAB structures in the two right corner, the two MegaLAB structures in the bottom left corner, and the two MegaLAB structures in the bottom right corner. On EP20K200C and smaller devices, FastRow interconnect drives the two MegaLAB structures on the top and the two MegaLAB structures on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLAB structures except the end local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



Note to Figure 22:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

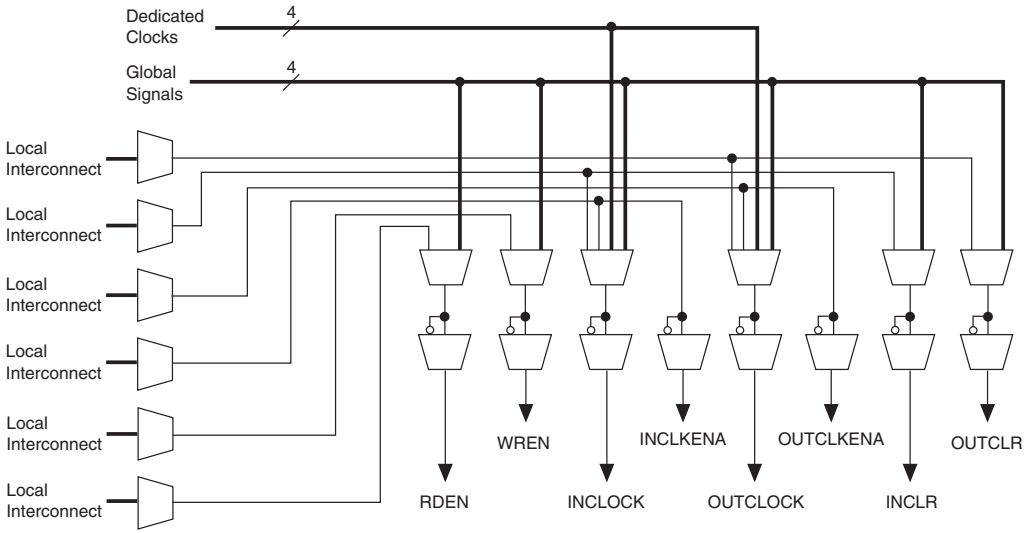
In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

For more information on APEX 20KC devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20KC ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20KC device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20KC IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

Table 9. APEX 20KC Programmable Delay Chains

Programmable Delay	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin
Clock enable delay	Increase clock enable delay

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

Notes to Figure 25:
(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

Figure 26. Row IOE Connection to the Interconnect

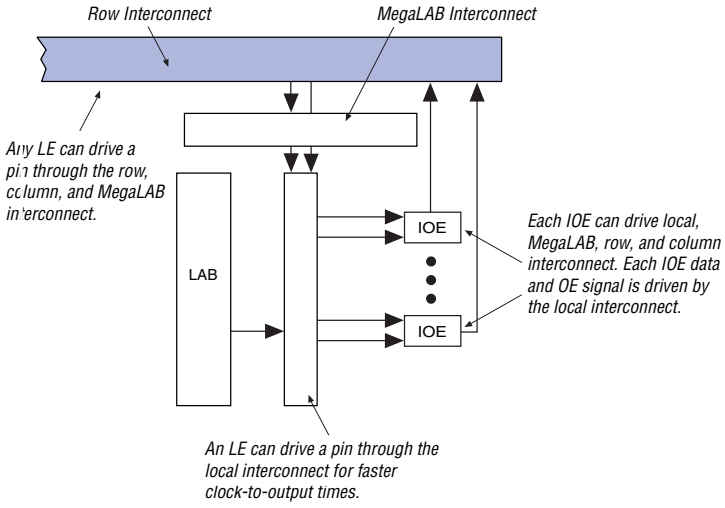
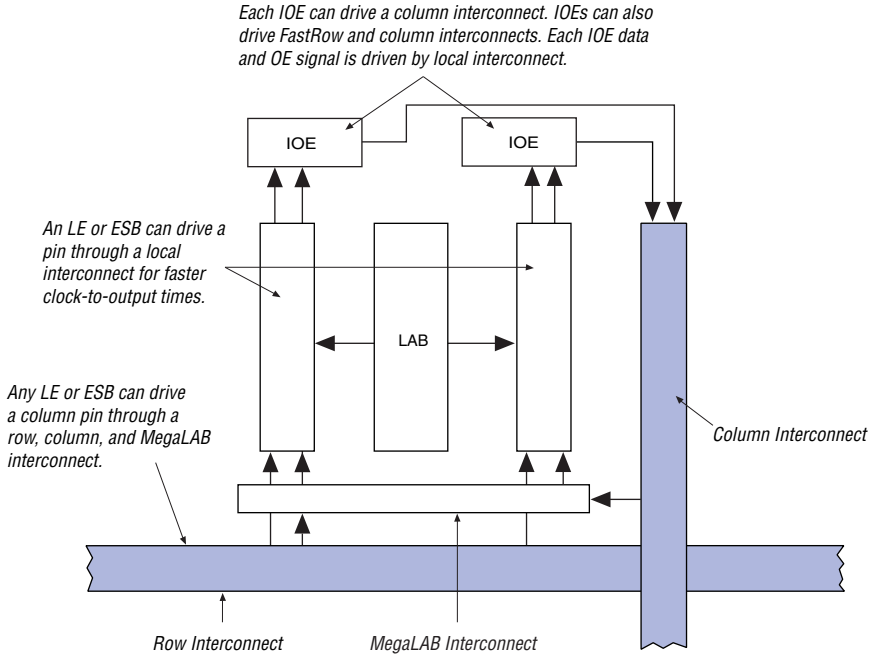


Figure 27 shows how a column IOE connects to the interconnect.

Figure 27. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ *(1)*	✓ *(1)*		✓			
2.5		✓	✓ *(1)*			✓		
3.3		✓	✓	✓ *(2)*		✓ *(3)*	✓	✓

Notes to Table 10:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Figure 30. APEX 20KC JTAG Waveforms

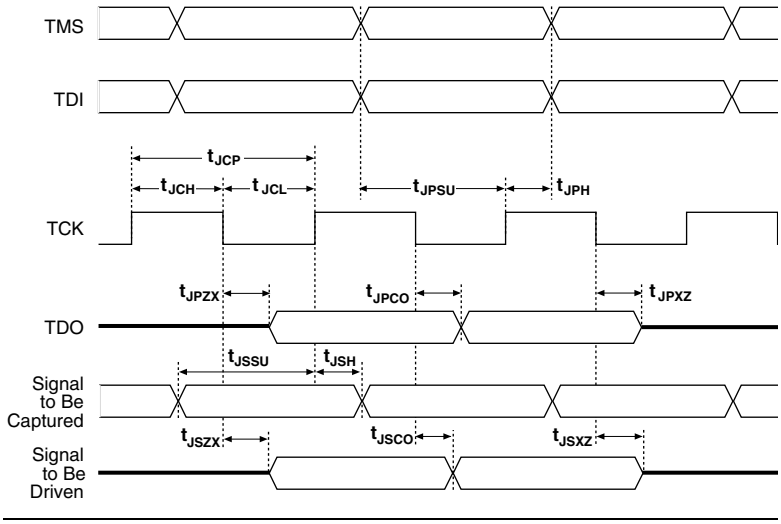


Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

Table 16. APEX 20KC JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*

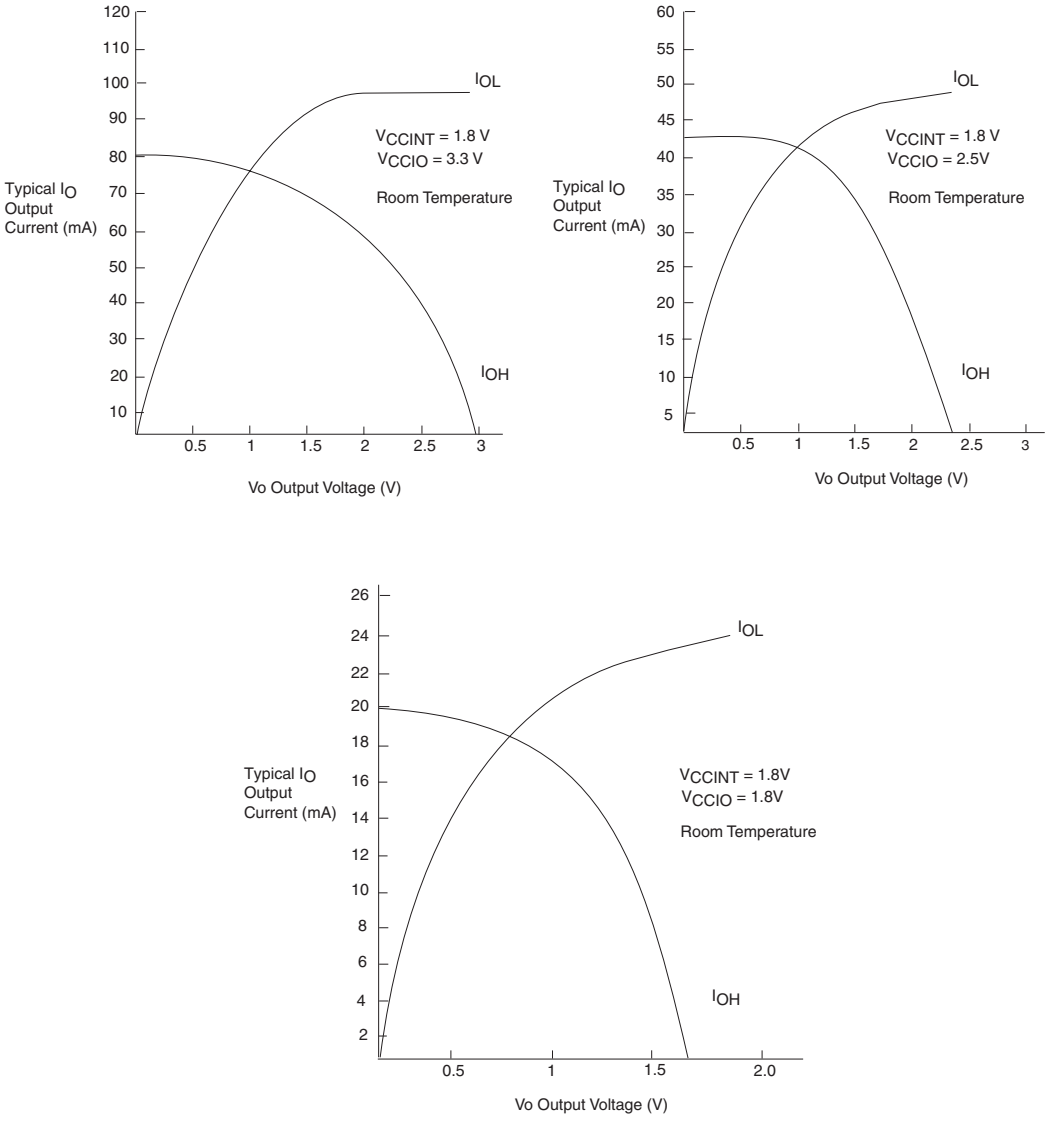
Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(2)*			0.65	V

Table 29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(2)*			V_{TT} – 0.57	V

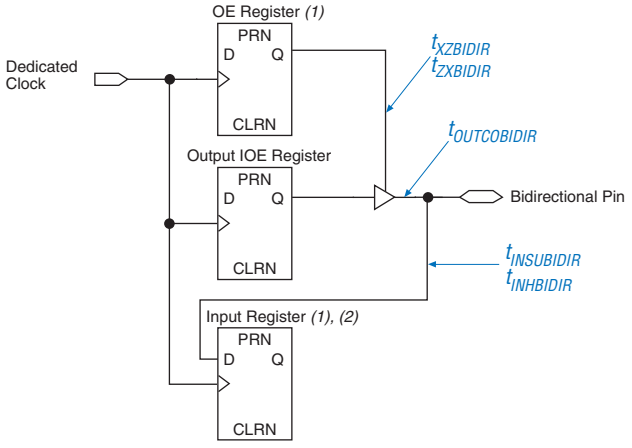
Figure 31. Output Drive Characteristics of APEX 20KC Devices *Note (1)*



Note to Figure 31:

(1) These are transient (AC) currents.

Figure 35. Synchronous Bidirectional Pin External Timing



Notes to Figure 35:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the "Output Enable Routing = Single-Pin" option in the Quartus II software to set the output enable register.

(2) Use the "Decrease Input Delay to Internal Cells = OFF" option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set "Decrease Input Delay to Internal Cells = ON" and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 36 to 38 describes the f_{MAX} timing parameters shown in Figure 32. Table 39 describes the functional timing parameters.

Table 36. APEX 20KC f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 55. EP20K400C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.29		1.67		1.92		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.25	2.00	4.61	2.00	5.03	ns
$t_{XZBIDIR}$		6.55		6.97		7.35	ns
$t_{ZXBIDIR}$		6.55		6.97		7.36	ns
$t_{INSUBIDIRPLL}$	3.22		3.80		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.27	0.50	2.55	-	-	ns
$t_{XZBIDIRPLL}$		4.62		4.84		-	ns
$t_{ZXBIDIRPLL}$		4.62		4.84		-	ns

Table 56. EP20K600C f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.65		0.78		0.92	ns

Table 57. EP20K600C f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.30		1.51		1.69	ns
t_{ESBSRC}		2.35		2.49		2.72	ns
t_{ESBAWC}		2.92		3.46		3.86	ns
t_{ESBSWC}		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
t_{ESBWAH}	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
t_{ESBWDH}	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
t_{ESBRAH}	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	–0.20		–0.24		–0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		–0.02		ns
$t_{ESBDATACO1}$		1.09		1.28		1.43	ns
$t_{ESBDATACO2}$		2.10		2.52		2.82	ns
t_{ESBDD}		2.50		2.97		3.32	ns
t_{PD}		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

Table 58. EP20K600C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.16		0.18	ns
t_{F5-20}		0.94		1.05		1.20	ns
t_{F20+}		1.76		1.98		2.23	ns

Table 61. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.03		2.57		2.97		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{XZBIDIR}$		8.31		9.14		9.76	ns
$t_{ZXBIDIR}$		8.31		9.14		9.76	ns
$t_{INSUBIDIRPLL}$	3.99		4.77		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.37	0.50	2.63	-	-	ns
$t_{XZBIDIRPLL}$		6.35		6.94		-	ns
$t_{ZXBIDIRPLL}$		6.35		6.94		-	ns

Table 62. EP20K1000C f_{MAX} LE Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.66		0.79		0.92	ns

Table 67. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.86		2.54		3.15		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.63	2.00	5.26	2.00	5.69	ns
$t_{XZBIDIR}$		8.98		9.89		10.67	ns
$t_{ZXBIDIR}$		8.98		9.89		10.67	ns
$t_{INSUBIDIRPLL}$	4.17		5.27		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.32	0.50	2.55	-	-	ns
$t_{XZBIDIRPLL}$		6.67		7.18		-	ns
$t_{ZXBIDIRPLL}$		6.67		7.18		-	ns

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 68. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		0.04		0.11		0.14	ns
PCI		0.00		0.04		0.03	ns
GTL+		–0.30		0.25		0.23	ns
SSTL-3 Class I		–0.19		–0.13		–0.13	ns
SSTL-3 Class II		–0.19		–0.13		–0.13	ns
SSTL-2 Class I		–0.19		–0.13		–0.13	ns
SSTL-2 Class II		–0.19		–0.13		–0.13	ns
LVDS		–0.19		–0.17		–0.16	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		–0.52		–0.53		–0.56	ns
GTL+		–0.18		–0.29		–0.39	ns
SSTL-3 Class I		–0.67		–0.71		–0.75	ns
SSTL-3 Class II		–0.67		–0.71		–0.75	ns
SSTL-2 Class I		–0.67		–0.71		–0.75	ns
SSTL-2 Class II		–0.67		–0.71		–0.75	ns
LVDS		–0.69		–0.70		–0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.