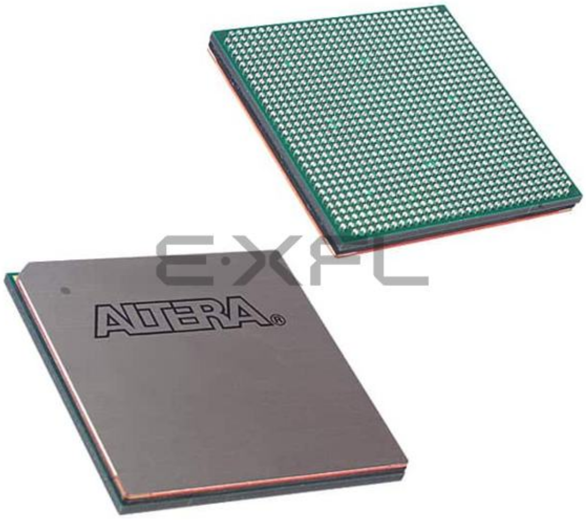
Intel - EP20K1000CF33C8ES Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

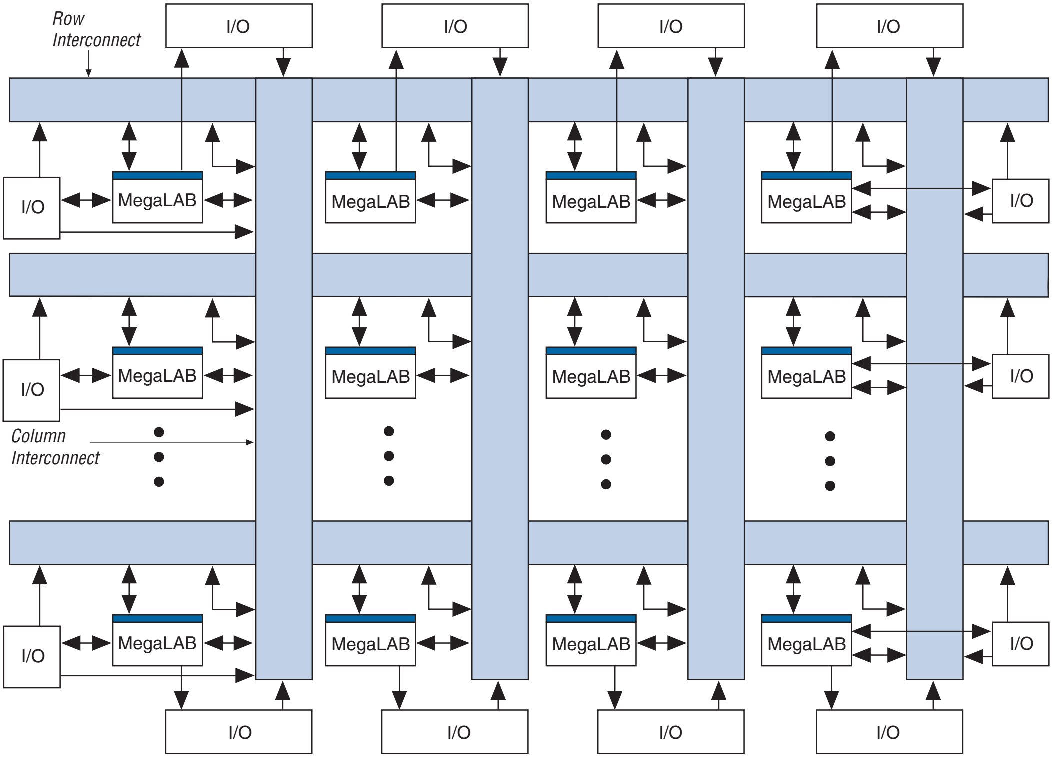
Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	708
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1000cf33c8es

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP & BGA Package Options & I/O Count *Notes (1), (2)*

Device	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K200C	136	168	271	
EP20K400C				488
EP20K600C				488
EP20K1000C				488

Figure 9. APEX 20KC Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 12. APEX 20KC FastRow Interconnect

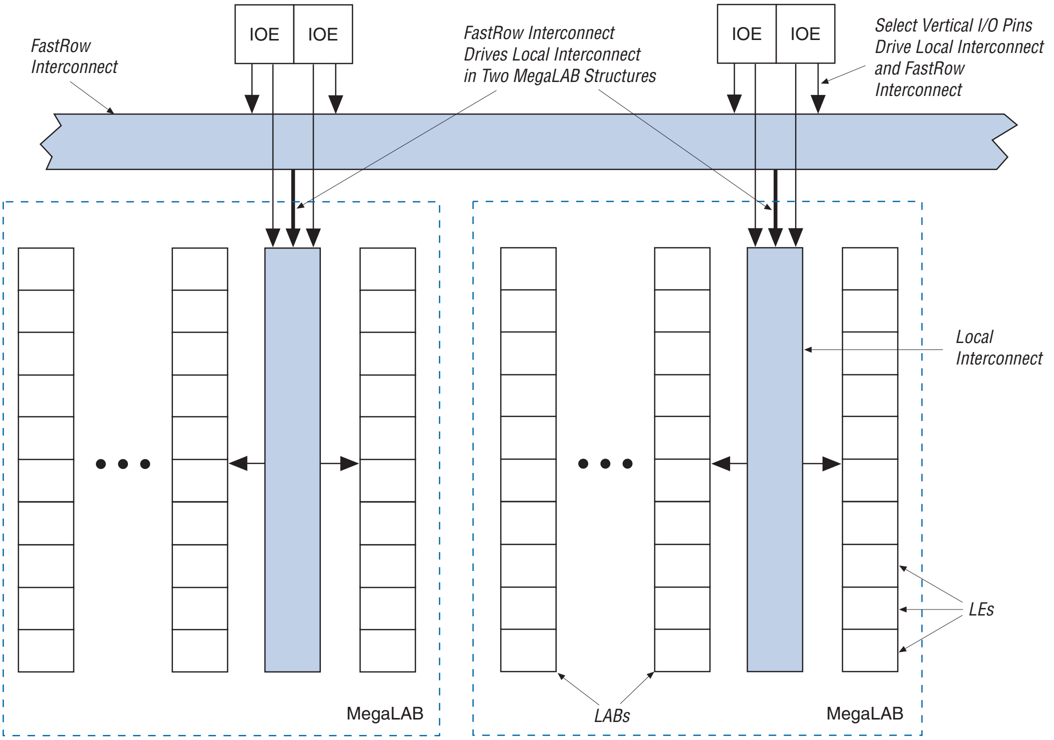
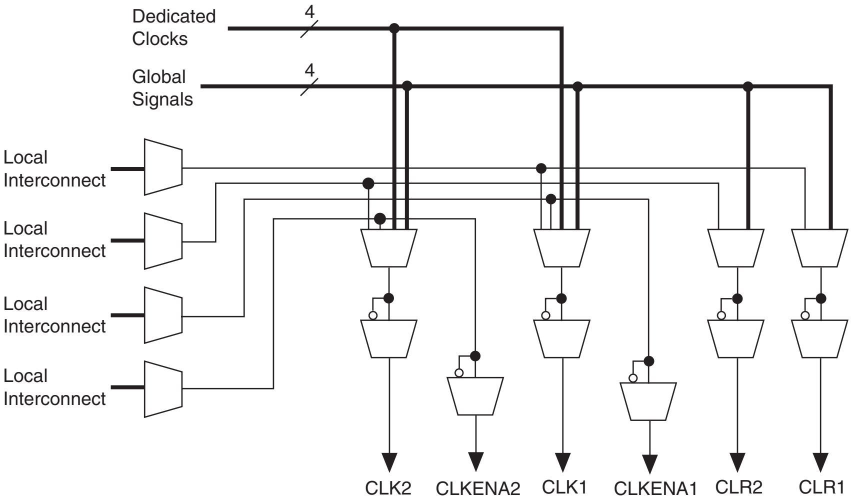


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

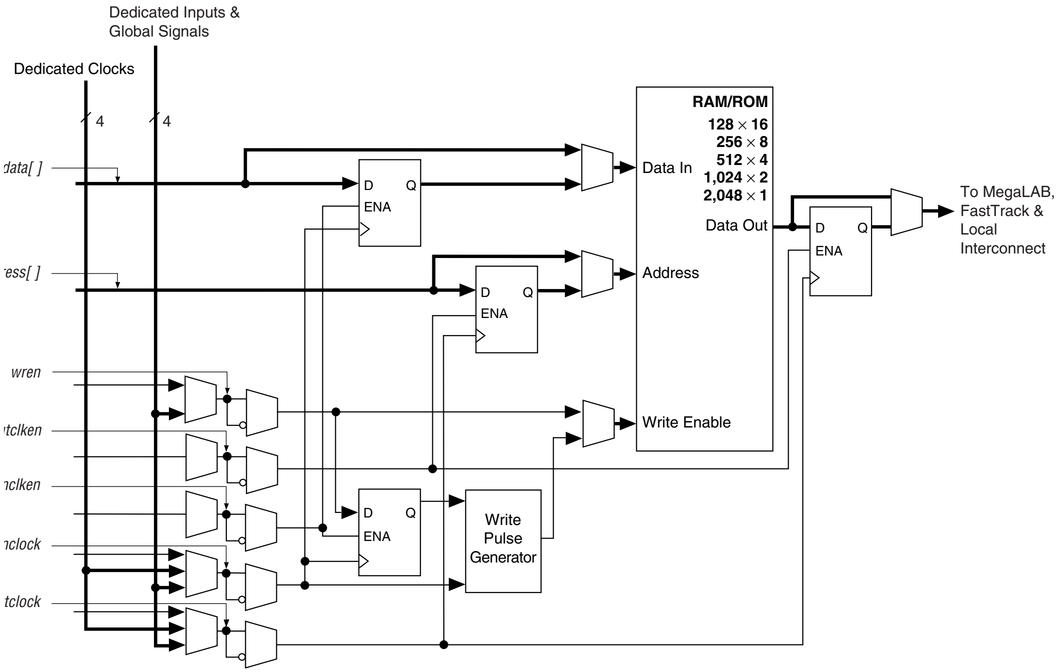
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, `WE`, and write address. The other clock controls all registers associated with reading: read enable (`RE`), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*

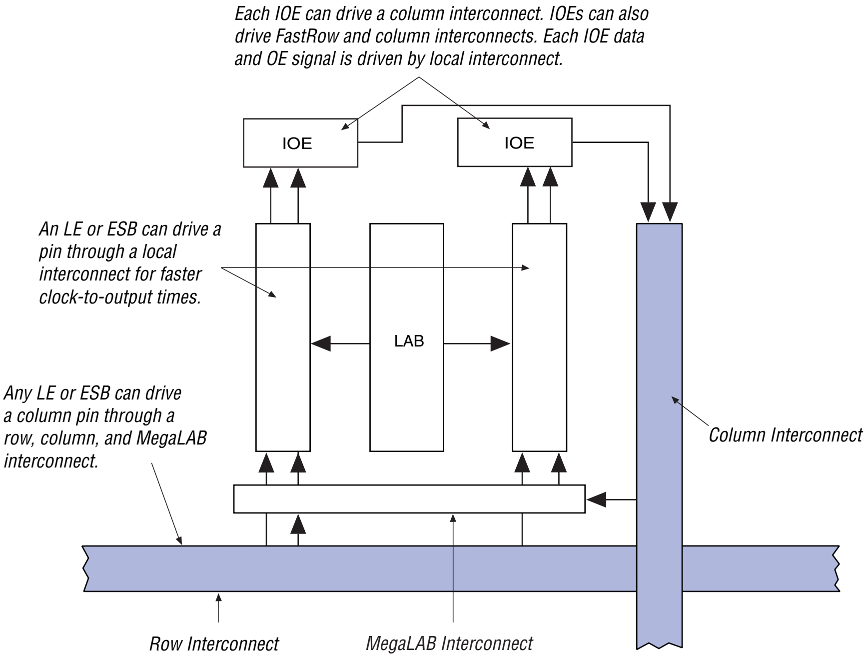


Note to Figure 20:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Figure 27 shows how a column IOE connects to the interconnect.

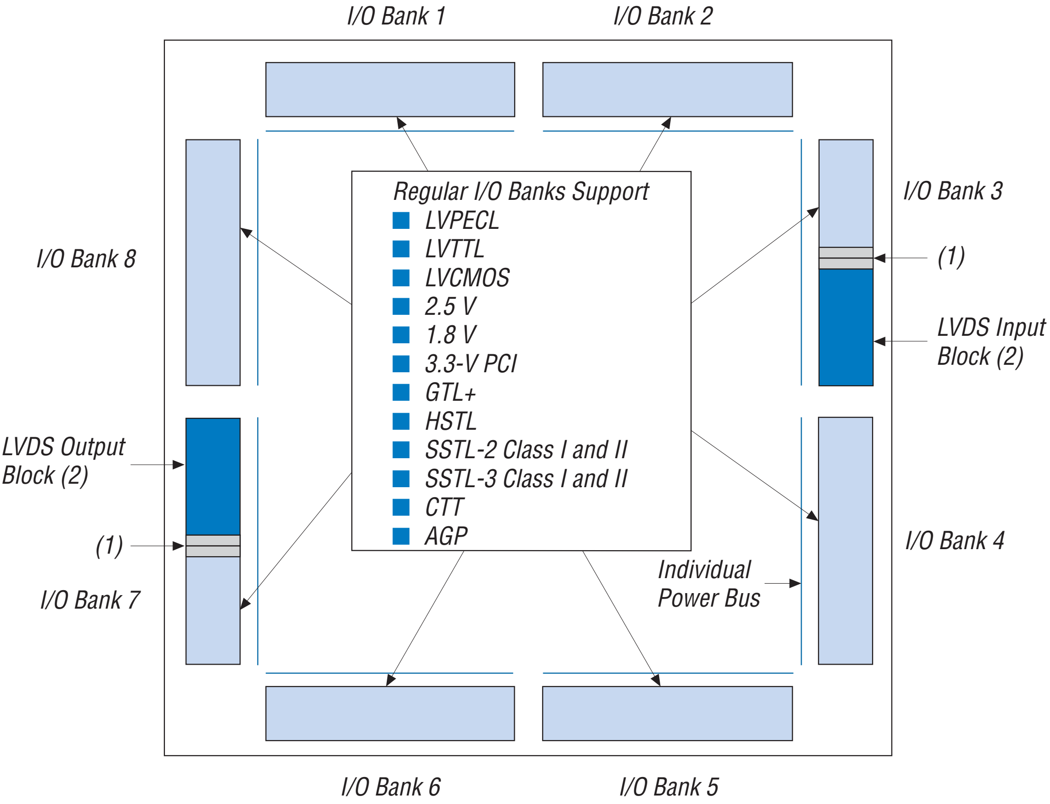
Figure 27. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Figure 28. APEX 20KC I/O Banks



Notes to Figure 28:

(1) For more information on placing I/O pins in LVDS blocks, refer to the "Guidelines for Using LVDS Blocks" section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20KC devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2) Note (1)

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz
f_{IN}	Input clock frequency	3.3-V LVTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

Notes to Tables 11 and 12:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz $\leq f_{VCO} \leq$ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

Table 14. APEX 20KC Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K200C	1,164
EP20K400C	1,506
EP20K600C	1,806
EP20K1000C	2,190

Table 15. 32-Bit APEX 20KC Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K200C	`0000`	`1000 0010 0000 0000`	`000 0110 1110`	`1`
EP20K400C	`0000`	`1000 0100 0000 0000`	`000 0110 1110`	`1`
EP20K600C	`0000`	`1000 0110 0000 0000`	`000 0110 1110`	`1`
EP20K1000C	`0000`	`1001 0000 0000 0000`	`000 0110 1110`	`1`

Notes to Table 15:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

Figure 30. APEX 20KC JTAG Waveforms

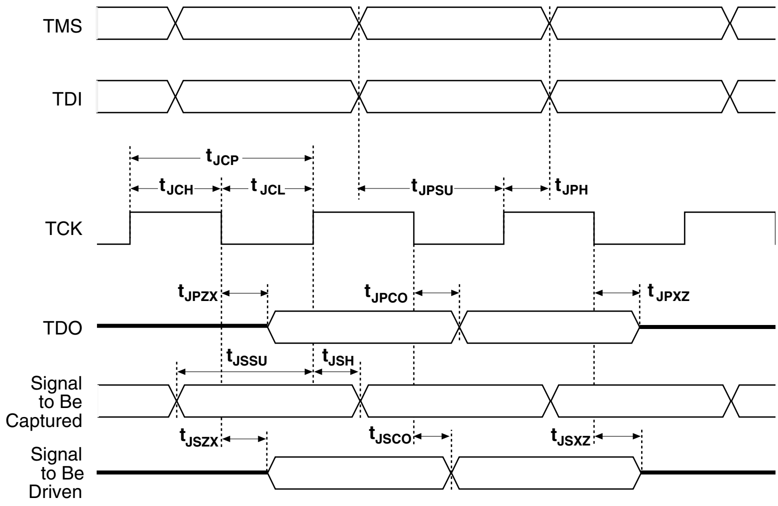


Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

Table 16. APEX 20KC JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	`TCK` clock period	100		ns
t_{JCH}	`TCK` clock high time	50		ns
t_{JCL}	`TCK` clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*

- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those defined in the "Timing Model" section on page 65. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

Table 17. APEX 20KC Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 22. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0 V I_{OH} = –0.1 mA *(1)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0 V I_{OL} = 0.1 mA *(2)*		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA *(1)*	2.1		V
		I_{OH} = –1 mA *(1)*	2.0		V
		I_{OH} = –2 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA *(2)*		0.2	V
		I_{OL} = 1 mA *(2)*		0.4	V
		I_{OL} = 2 mA *(2)*		0.7	V

Table 24. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage			$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	$V_{IN} = 0$ V or 3.3 V	–10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = –2$ mA *(1)*	$V_{CCIO} – 0.45$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA *(2)*		0.45	V

Table 25. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	μA
V_{OH}	High-level output voltage	$I_{OUT} = –500$ μA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1,500$ μA			$0.1 \times V_{CCIO}$	V

Table 30. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		–0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -15.2$ mA *(1)*	$V_{TT} + 0.76$			V
V_{OL}	Low-level output voltage	$I_{OL} = 15.2$ mA *(2)*			$V_{TT} - 0.76$	V

Table 31. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		–0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA *(1)*	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(2)*			$V_{TT} - 0.6$	V

Table 34. 3.3-V AGP I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -500\ \mu A$	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1{,}500\ \mu A$			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 35. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(3)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.2$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA *(1)*	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(2)*			$V_{REF} - 0.4$	V
I_O	Output leakage current (when output is high Z)	$GND \leq V_{OUT} \leq V_{CCIO}$	–10		10	µA

Notes to Tables 21 through 35:

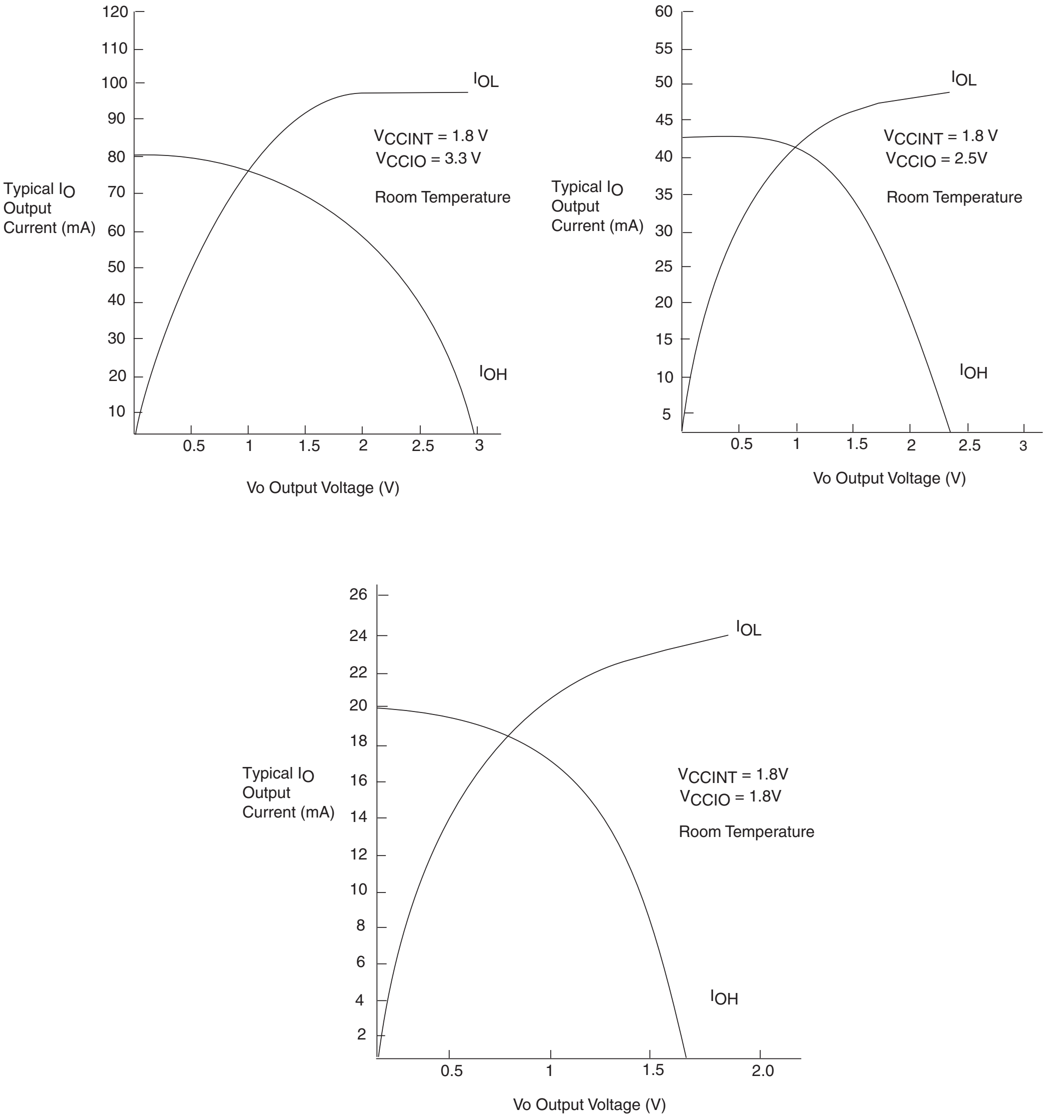
(1) The I_{OH} parameter refers to high-level output current.

(2) The I_{OL} parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.

(3) V_{REF} specifies center point of switching range.

Figure 31 shows the output drive characteristics of APEX 20KC devices.

Figure 31. Output Drive Characteristics of APEX 20KC Devices *Note (1)*

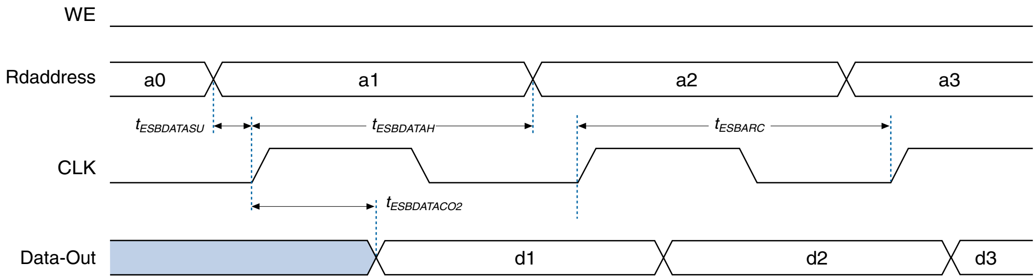


Note to Figure 31:

(1) These are transient (AC) currents.

Figure 34. ESB Synchronous Timing Waveforms

ESB Synchronous Read



ESB Synchronous Write (ESB Output Registers Used)

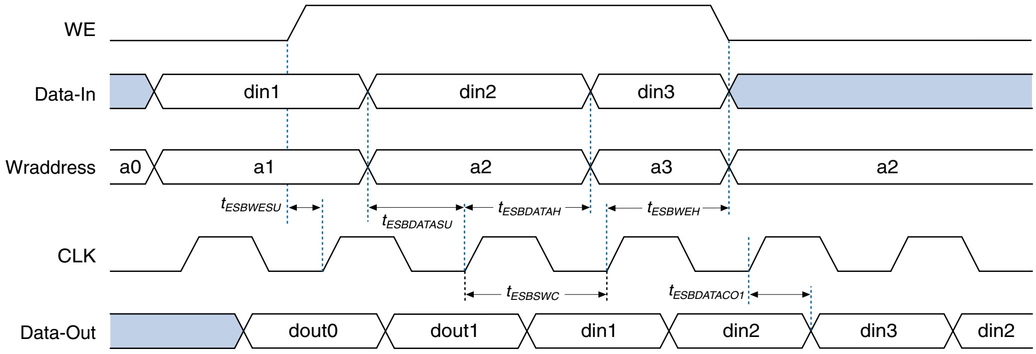


Figure 35 shows the timing model for bidirectional I/O pin timing.

Table 39. APEX 20KC Minimum Pulse Width Timing Parameters

Symbol	Parameter
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 40 and 41 describe APEX 20KC external timing parameters. The timing values for these pin-to-pin delays are reported for all pins using the 3.3-V LVTTL I/O standard.

Table 40. APEX 20KC External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	*(2)*
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	*(2)*

Table 67. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.86		2.54		3.15		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.63	2.00	5.26	2.00	5.69	ns
$t_{XZBIDIR}$		8.98		9.89		10.67	ns
$t_{ZXBIDIR}$		8.98		9.89		10.67	ns
$t_{INSUBIDIRPLL}$	4.17		5.27		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.32	0.50	2.55	-	-	ns
$t_{XZBIDIRPLL}$		6.67		7.18		-	ns
$t_{ZXBIDIRPLL}$		6.67		7.18		-	ns

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 68. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		0.04		0.11		0.14	ns
PCI		0.00		0.04		0.03	ns
GTL+		–0.30		0.25		0.23	ns
SSTL-3 Class I		–0.19		–0.13		–0.13	ns
SSTL-3 Class II		–0.19		–0.13		–0.13	ns
SSTL-2 Class I		–0.19		–0.13		–0.13	ns
SSTL-2 Class II		–0.19		–0.13		–0.13	ns
LVDS		–0.19		–0.17		–0.16	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns