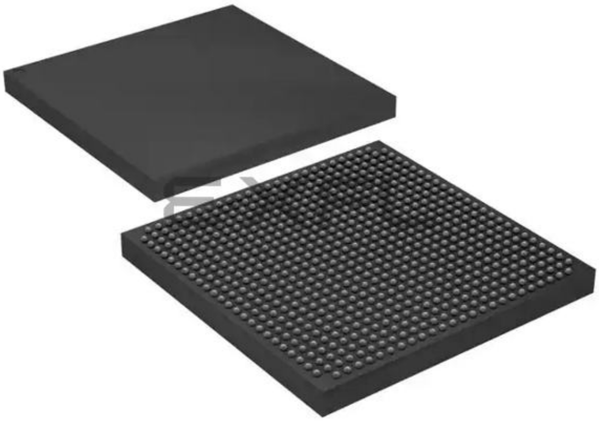
Intel - EP20K1000CF672C7ES Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	508
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1000cf672c7es

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

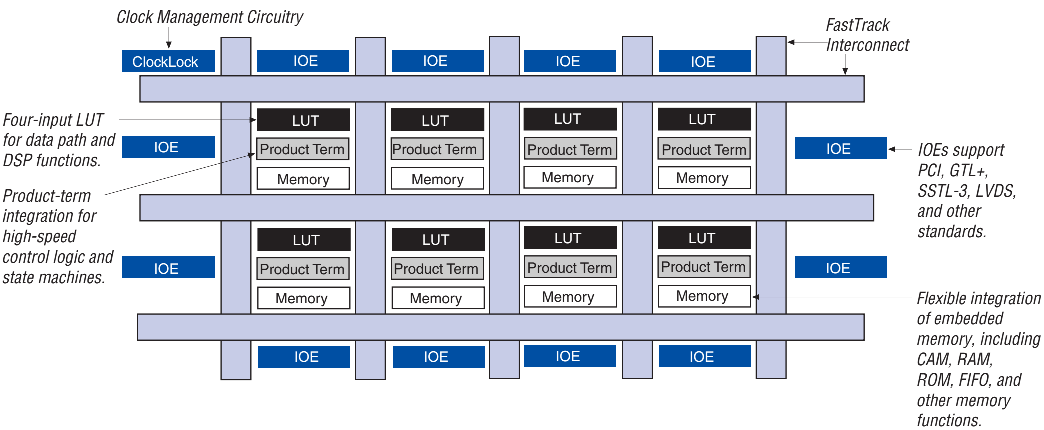
Functional Description

APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

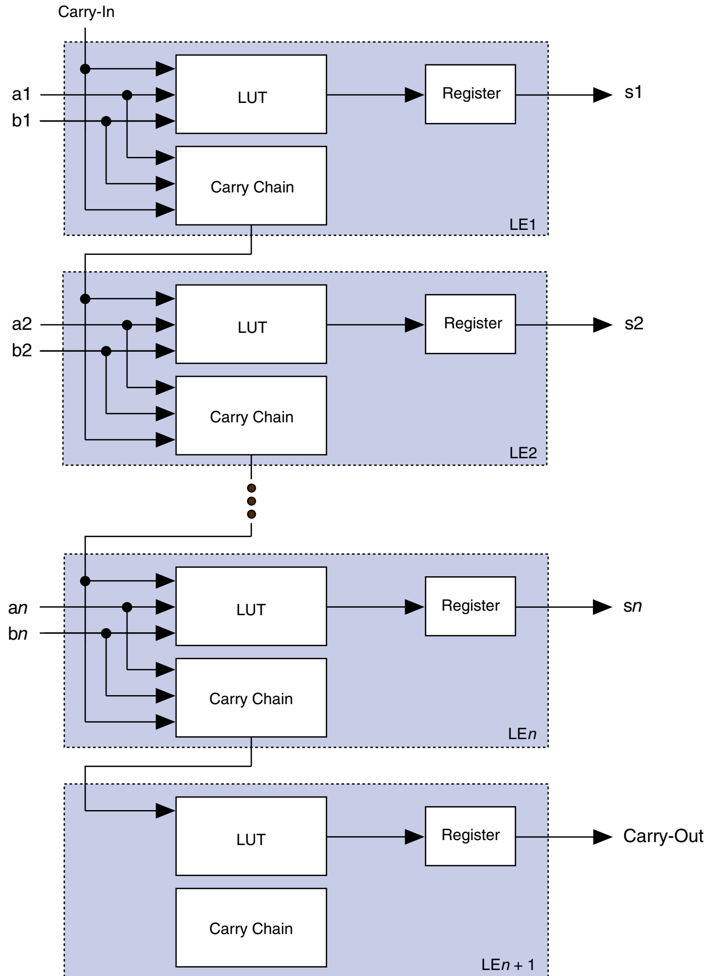
The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

Figure 1. APEX 20KC Device Block Diagram



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

Figure 6. APEX 20KC Carry Chain



LE Operating Modes

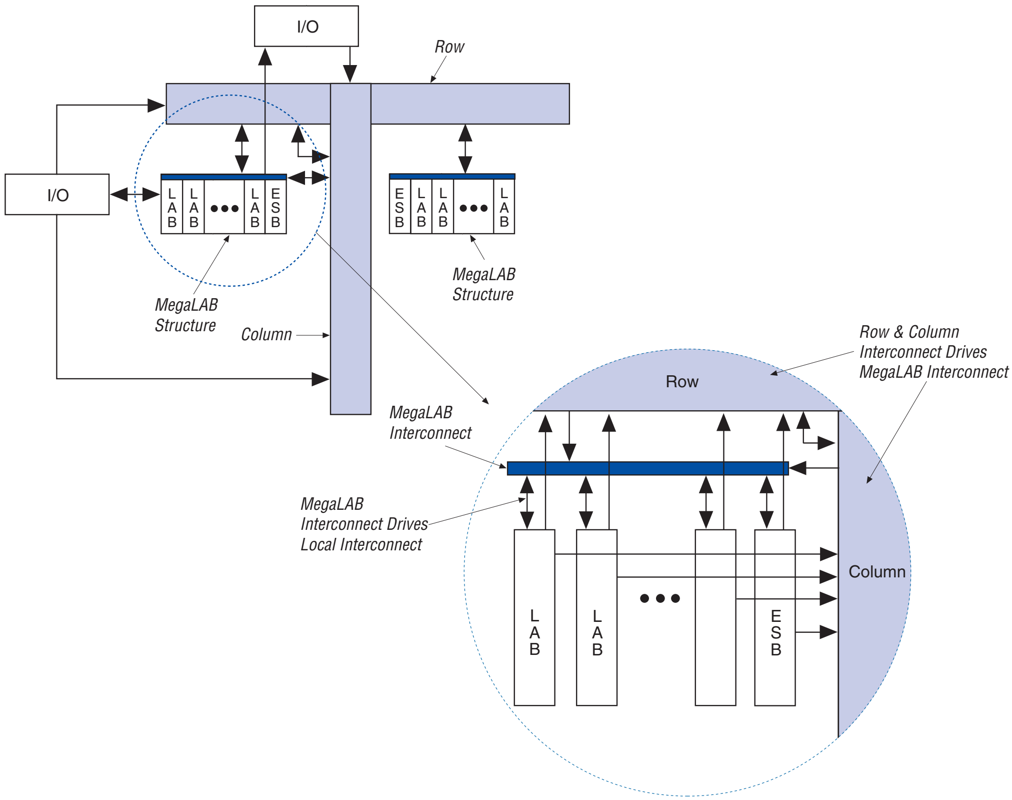
The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

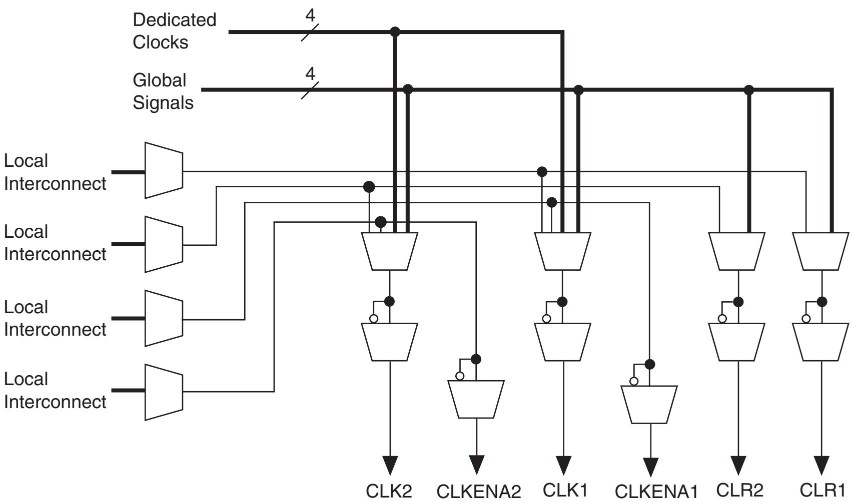
The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 10. FastTrack Connection to Local Interconnect



The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

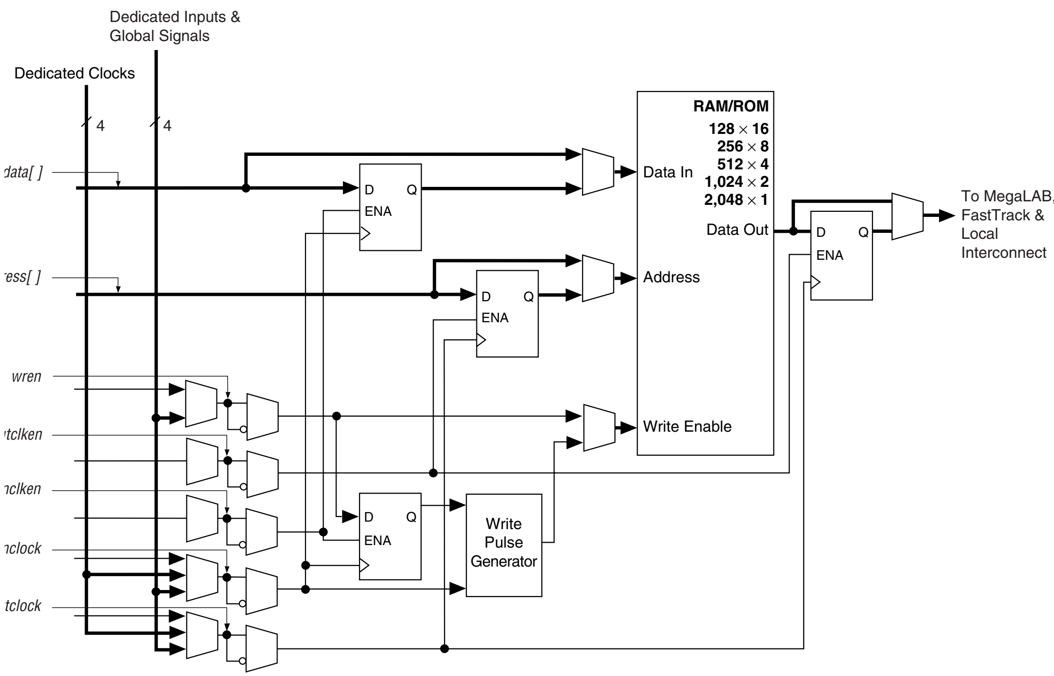
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Note to Figure 20:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)*

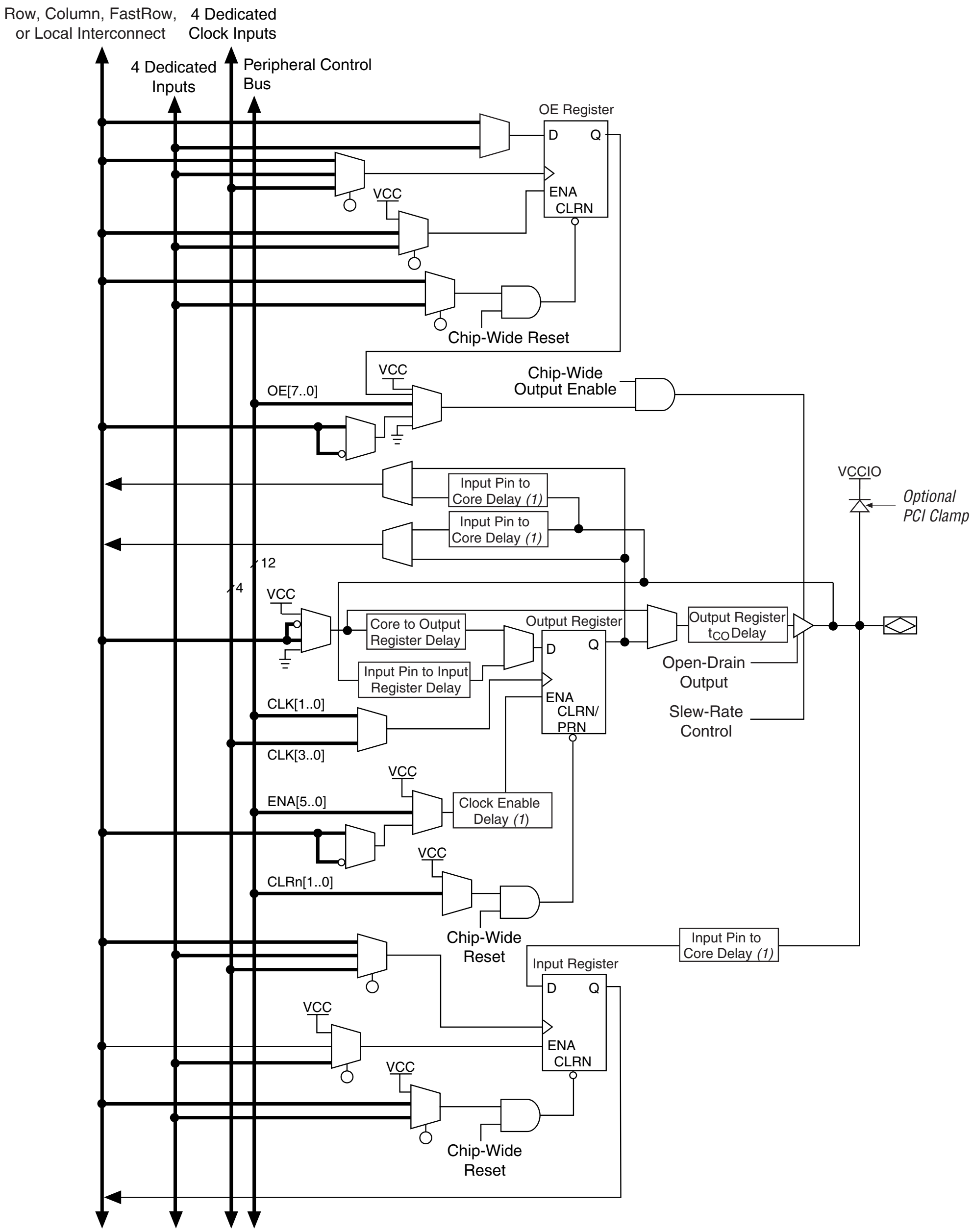
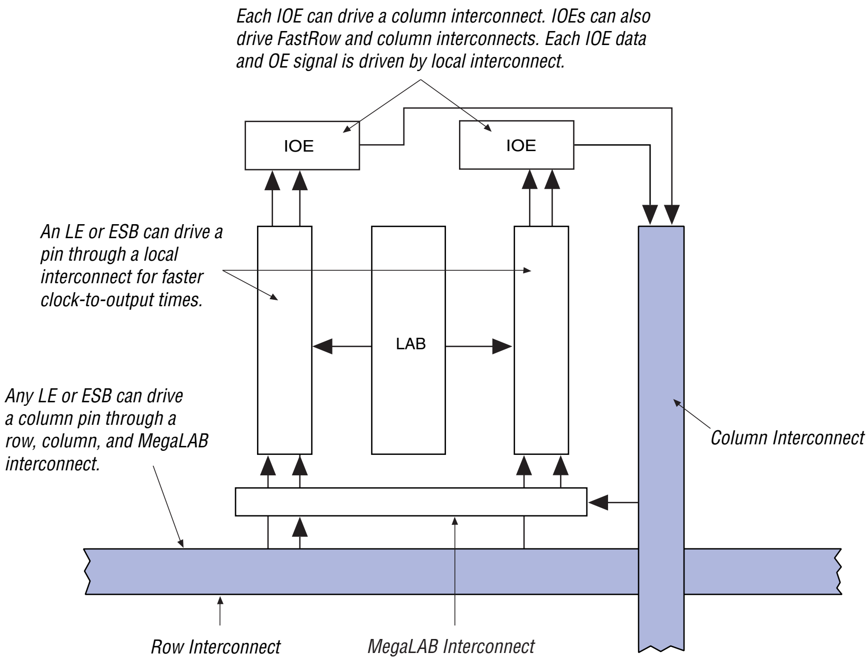


Figure 27 shows how a column IOE connects to the interconnect.

Figure 27. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC `VCCINT` pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the `VCCIO` pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ *(1)*	✓ *(1)*		✓			
2.5		✓	✓ *(1)*			✓		
3.3		✓	✓	✓ *(2)*		✓ *(3)*	✓	✓

Notes to Table 10:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

Table 13. APEX 20KC JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`.
IDCODE	Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Table 26. 3.3-V PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
I_{IL}	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10.0		10.0	µA
V_{OH}	High-level output voltage	$I_{OUT} = –500$ µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1,500$ µA			$0.1 \times V_{CCIO}$	V
L_{pin}	Pin Inductance				15.0	nH

Table 27. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	$R_L = 100\ \Omega$	250		650	mV
ΔV_{OD}	Change in V_{OD} between high and low	$R_L = 100\ \Omega$			50	mV
V_{OS}	Output offset voltage	$R_L = 100\ \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	$R_L = 100\ \Omega$			50	mV
V_{TH}	Differential input threshold	$V_{CM} = 1.2$ V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX devices)		90	100	110	Ω

Figure 34. ESB Synchronous Timing Waveforms

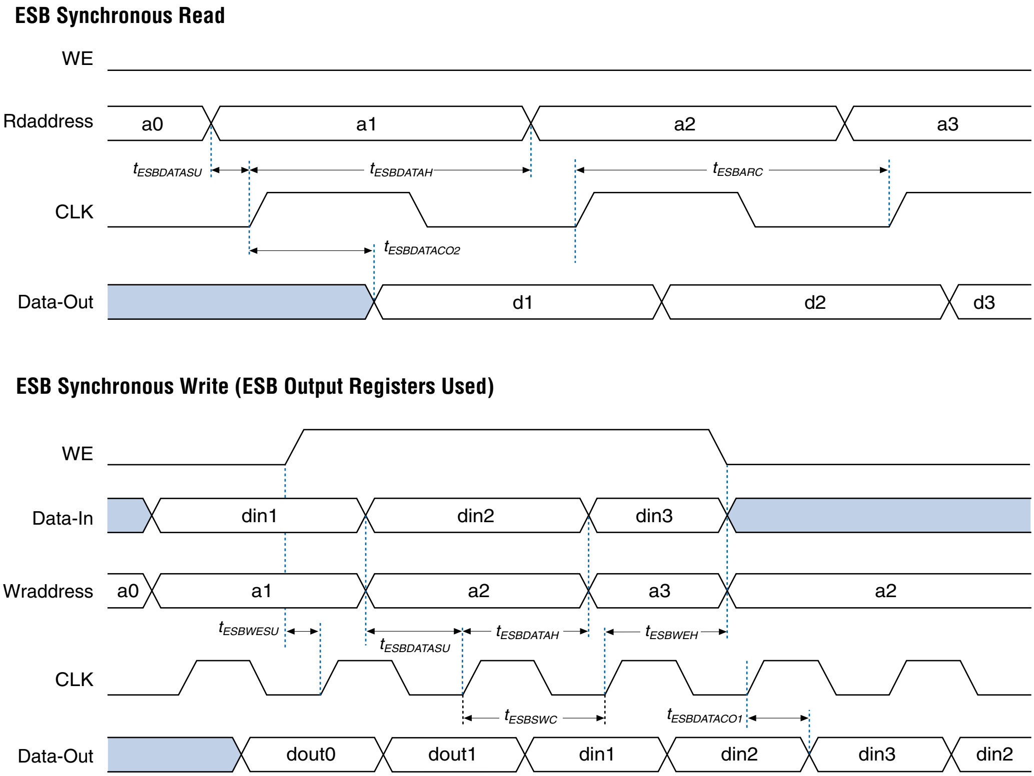
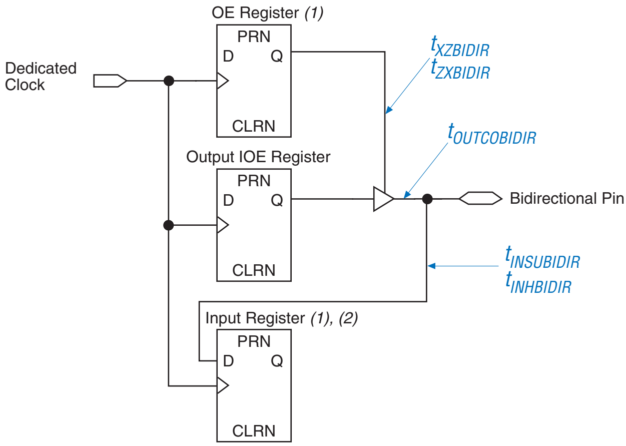


Figure 35 shows the timing model for bidirectional I/O pin timing.

Figure 35. Synchronous Bidirectional Pin External Timing



Notes to Figure 35:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the "Output Enable Routing = Single-Pin" option in the Quartus II software to set the output enable register.

(2) Use the "Decrease Input Delay to Internal Cells = OFF" option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set "Decrease Input Delay to Internal Cells = ON" and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 36 to 38 describes the f_{MAX} timing parameters shown in Figure 32. Table 39 describes the functional timing parameters.

Table 36. APEX 20KC f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 39. APEX 20KC Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 40 and 41 describe APEX 20KC external timing parameters. The timing values for these pin-to-pin delays are reported for all pins using the 3.3-V LVTTL I/O standard.

Table 40. APEX 20KC External Timing Parameters *Note (1)*		
Symbol	**Clock Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	*(2)*
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	*(2)*

Table 41. APEX 20KC External Bidirectional Timing Parameters *Note (1)*		
Symbol	**Parameter**	**Condition**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	*(2)*
$t_{XZBIDIR}$	Synchronous output enable register to output buffer disable delay	*(2)*
$t_{ZXBIDIR}$	Synchronous output enable register to output buffer enable delay	*(2)*
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	*(2)*
$t_{XZBIDIRPLL}$	Synchronous output enable register to output buffer disable delay with PLL	*(2)*
$t_{ZXBIDIRPLL}$	Synchronous output enable register to output buffer enable delay with PLL	*(2)*

Notes to Tables 40 and 41:
(1) These timing parameters are sample-tested only.
(2) For more information, refer to Table 43.

Tables 42 and 43 define the timing delays for each I/O standard. Some output standards require test load circuits for AC timing measurements as shown in Figures 36 through 38.

Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 1 of 2) *Note (1)*		
Symbol	**Parameter**	**Condition**
LVCMOS	Input adder delay for the LVCMOS I/O standard	
LVTTL	Input adder delay for the LVTTL I/O standard	
2.5 V	Input adder delay for the 2.5-V I/O standard	
1.8 V	Input adder delay for the 1.8-V I/O standard	
PCI	Input adder delay for the PCI I/O standard	
GTl+	Input adder delay for the GTL+ I/O standard	
SSTL-3 Class I	Input adder delay for the SSTL-3 Class I I/O standard	
SSTL-3 Class II	Input adder delay for the SSTL-3 Class II I/O standard	
SSTL-2 Class I	Input adder delay for the SSTL -2 Class I I/O standard	
SSTL-2 Class II	Input adder delay for the SSTL -2 Class II I/O standard	

Table 67. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.86		2.54		3.15		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.63	2.00	5.26	2.00	5.69	ns
$t_{XZBIDIR}$		8.98		9.89		10.67	ns
$t_{ZXBIDIR}$		8.98		9.89		10.67	ns
$t_{INSUBIDIRPLL}$	4.17		5.27		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.32	0.50	2.55	-	-	ns
$t_{XZBIDIRPLL}$		6.67		7.18		-	ns
$t_{ZXBIDIRPLL}$		6.67		7.18		-	ns

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 68. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		0.04		0.11		0.14	ns
PCI		0.00		0.04		0.03	ns
GTL+		–0.30		0.25		0.23	ns
SSTL-3 Class I		–0.19		–0.13		–0.13	ns
SSTL-3 Class II		–0.19		–0.13		–0.13	ns
SSTL-2 Class I		–0.19		–0.13		–0.13	ns
SSTL-2 Class II		–0.19		–0.13		–0.13	ns
LVDS		–0.19		–0.17		–0.16	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		–0.52		–0.53		–0.56	ns
GTL+		–0.18		–0.29		–0.39	ns
SSTL-3 Class I		–0.67		–0.71		–0.75	ns
SSTL-3 Class II		–0.67		–0.71		–0.75	ns
SSTL-2 Class I		–0.67		–0.71		–0.75	ns
SSTL-2 Class II		–0.67		–0.71		–0.75	ns
LVDS		–0.69		–0.70		–0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.