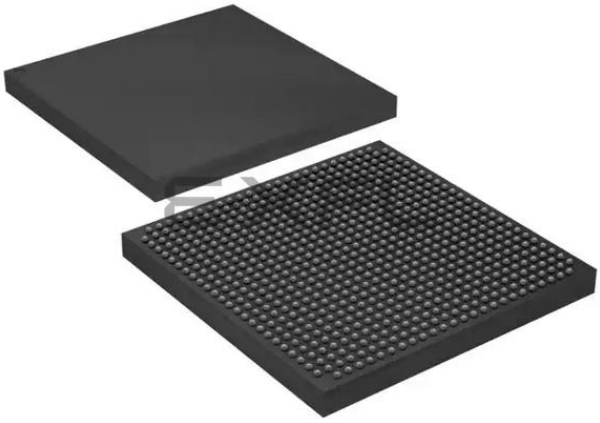


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	508
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1000cf672c7gz

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count Notes (1), (2)			
Device	**484 Pin**	**672 Pin**	**1,020 Pin**
EP20K200C	376		
EP20K400C		488 (3)	
EP20K600C		508 (3)	588
EP20K1000C		508 (3)	708

Notes to Tables 3 and 4:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20KC device package types include plastic quad flat pack (PQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA™ packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20KC QFP & BGA Package Sizes				
Feature	**208-Pin PQFP**	**240-Pin PQFP**	**356-Pin BGA**	**652-Pin BGA**
Pitch (mm)	0.50	0.50	1.27	1.27
Area (mm^2)	924	1,218	1,225	2,025
Length × Width (mm × mm)	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

Table 6. APEX 20KC FineLine BGA Package Sizes			
Feature	**484 Pin**	**672 Pin**	**1,020 Pin**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	529	729	1,089
Length × Width (mm × mm)	23 × 23	27 × 27	33 × 33

General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

Table 7. APEX 20KC Device Features (Part 2 of 2)

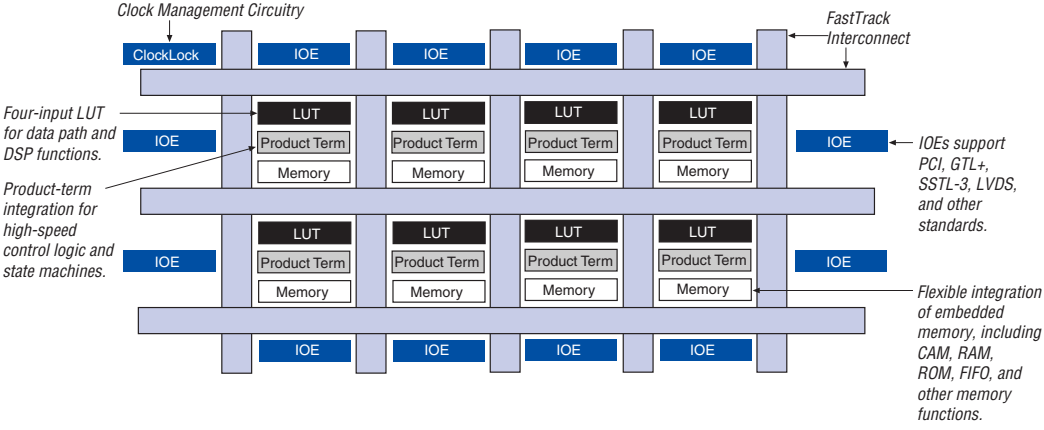
Feature	APEX 20KC Devices
I/O standard support	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI and PCI-X 3.3-V AGP CTT GTL+ LVCMOS LVTTL True-LVDS™ and LVPECL data pins (in EP20K400C and larger devices) LVDS and LVPECL clock pins (in all devices) LVDS and LVPECL data pins up to 156 Mbps (in EP20K200C devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	CAM Dual-port RAM FIFO RAM ROM

All APEX 20KC devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault-coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20KC devices can be configured on the board for the specific functionality required.

APEX 20KC devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC16, EPC8, EPC4, EPC2, and EPC1 configuration devices and one-time programmable (OTP) EPC1 configuration devices, which configure APEX 20KC devices via a serial data stream. Moreover, APEX 20KC devices contain an optimized interface that permits microprocessors to configure APEX 20KC devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20KC devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

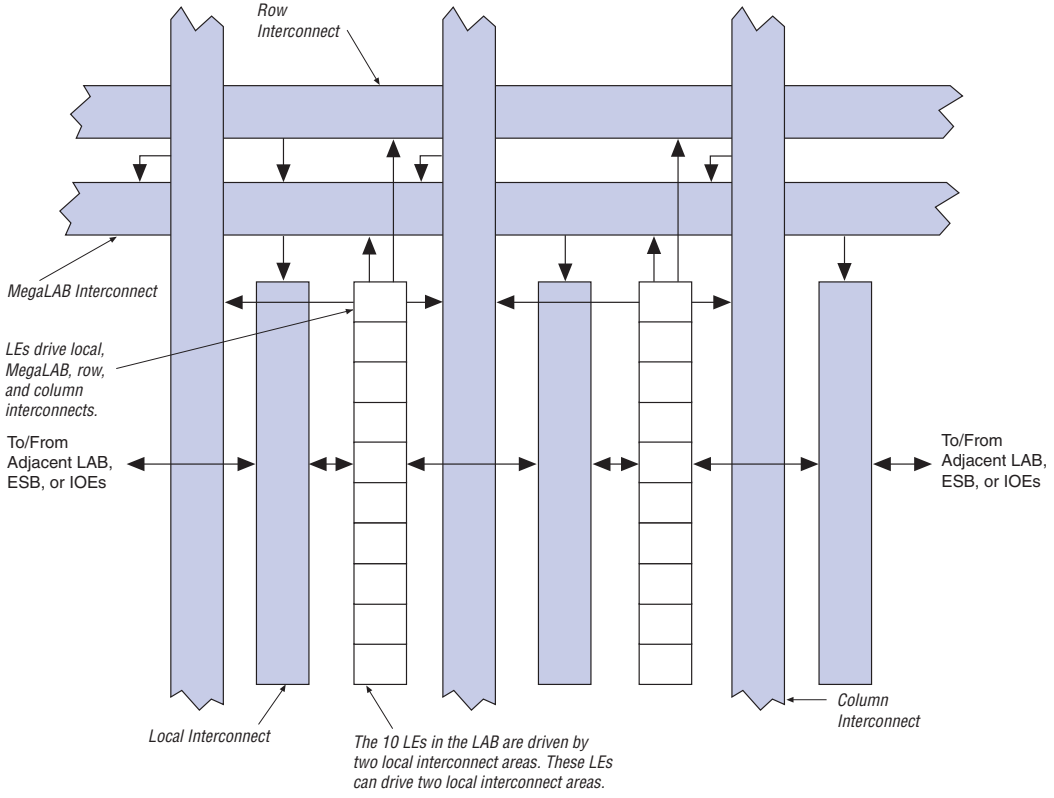
The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

Figure 1. APEX 20KC Device Block Diagram



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

Figure 3. LAB Structure

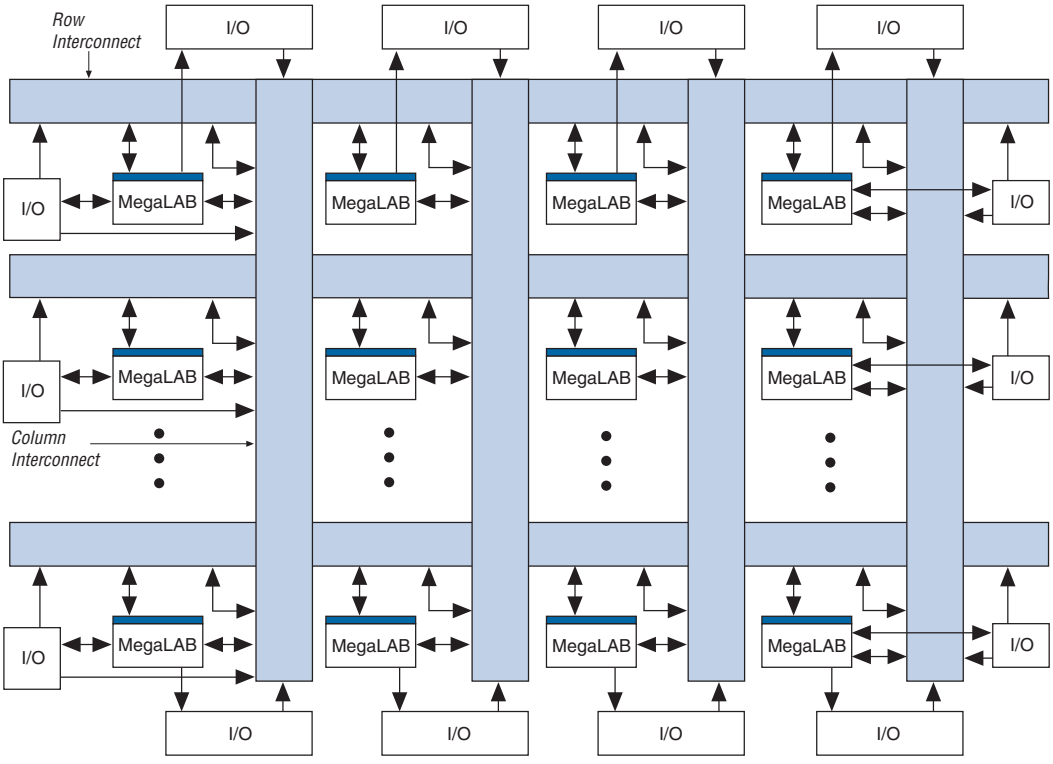


Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

Figure 9. APEX 20KC Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

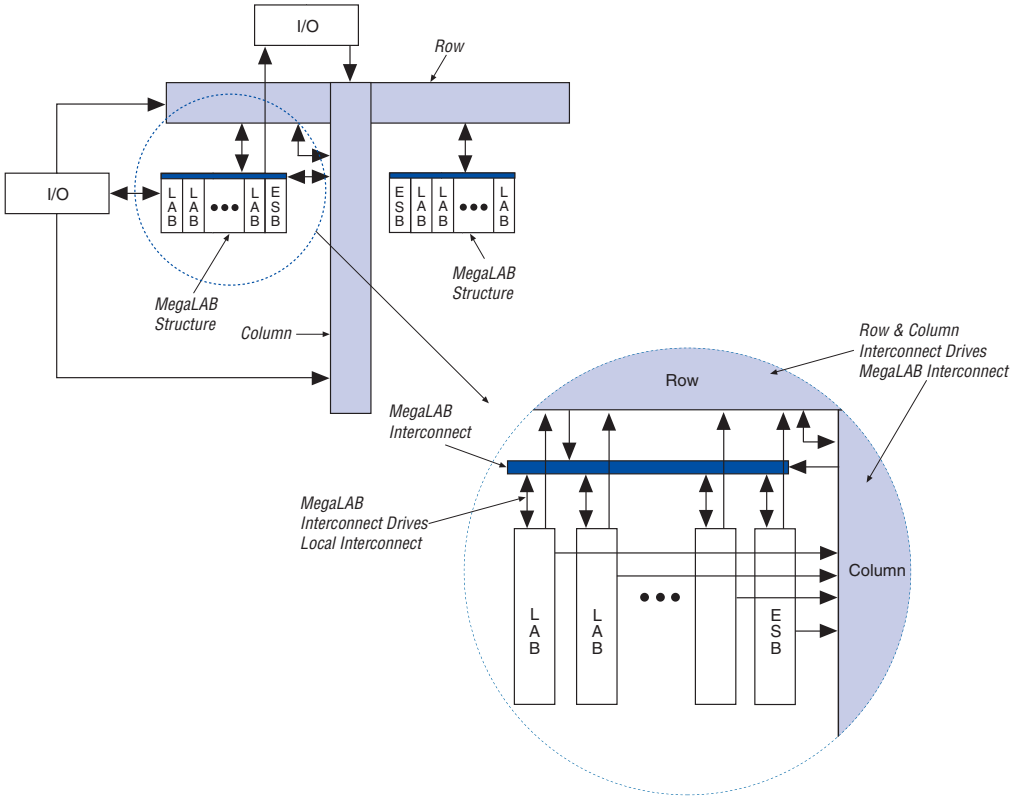


Figure 12. APEX 20KC FastRow Interconnect

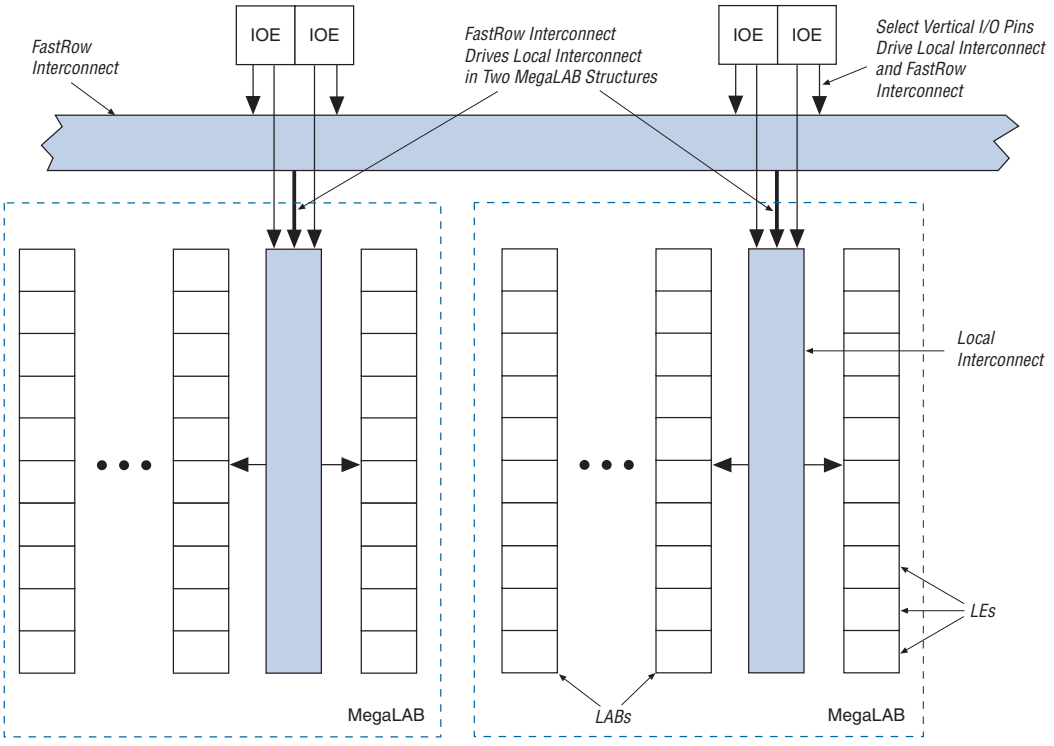
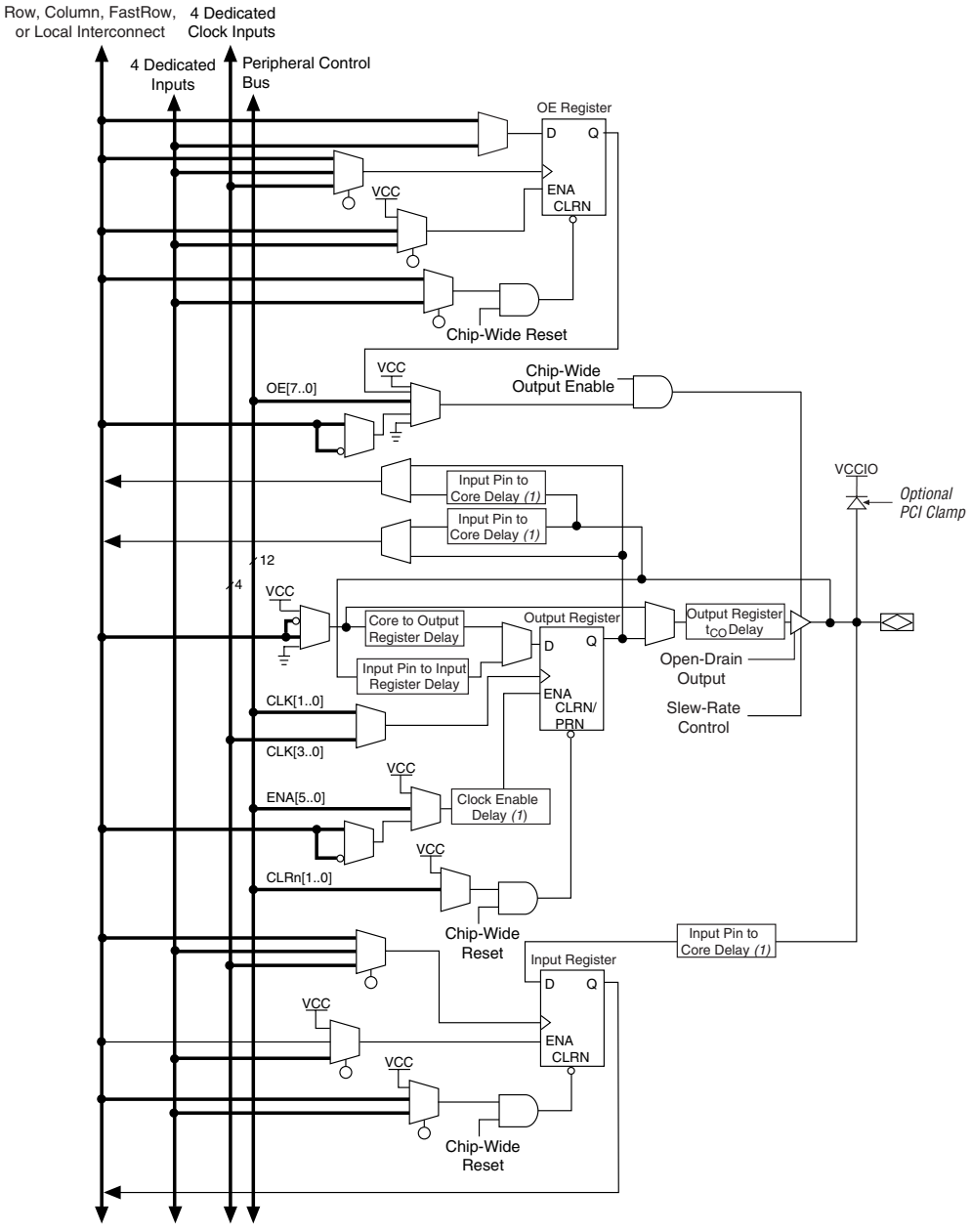


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)*



Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes to Table 10:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades have PLLs and support the ClockLock and ClockBoost features.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

Table 11. APEX 20KC ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	%
$t_{OUTJITTER}$	RMS jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	%
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} *(2), (3)*	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} *(4)*	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz
f_{IN}	Input clock frequency	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Notes to Tables 11 and 12:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ f_{VCO} ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

Table 13. APEX 20KC JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(2)*			0.65	V

Table 29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(2)*			V_{TT} – 0.57	V

Figure 33. ESB Asynchronous Timing Waveforms

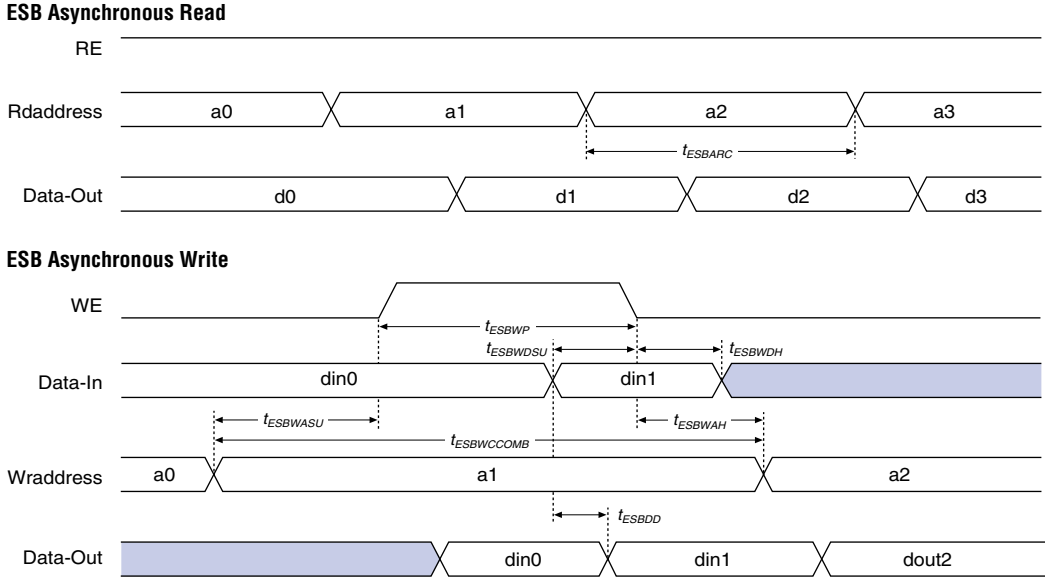


Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 2 of 2) *Note (1)*		
Symbol	**Parameter**	**Condition**
LVDS	Input adder delay for the LVDS I/O standard	
CTT	Input adder delay for the CTT I/O standard	
AGP	Input adder delay for the AGP I/O standard	

Table 43. APEX 20KC Selectable I/O Standard Output Adder Delays *Note (1)*		
Symbol	**Parameter**	**Condition**
LVCMOS	Output adder delay for the LVCMOS I/O standard	
LVTTL	Output adder delay for the LVTTL I/O standard	Cload = 35 pF Rup = 564.5 Ω Rdn = 430 Ω *(2)*
2.5 V	Output adder delay for the 2.5-V I/O standard	Cload = 35 pF Rup = 450 Ω Rdn = 450 Ω *(2)*
1.8 V	Output adder delay for the 1.8-V I/O standard	Cload = 35 pF Rup = 520 Ω Rdn = 480 Ω *(2)*
PCI	Output adder delay for the PCI I/O standard	Cload = 10 pF Rup = 1M Ω Rdn = 25 Ω *(2)*
GTl+	Output adder delay for the GTL+ I/O standard	Cload = 30 pF Rup = 25 Ω *(2)*
SSTL-3 Class I	Output adder delay for the SSTL-3 Class I I/O standard	Cload1 = 0 pF Cload2 = 30 pF R = 25 Ω *(2)*
SSTL-3 Class II	Output adder delay for the SSTL-3 Class II I/O standard	Cload1 = 0 pF Cload2 = 30 pF R = 25 Ω *(2)*
SSTL-2 Class I	Output adder delay for the SSTL-2 Class I I/O standard	
SSTL-2 Class II	Output adder delay for the SSTL-2 Class II I/O standard	
LVDS	Output adder delay for the LVDS I/O standard	Cload = 4 pF R=100 Ω *(2)*
CTT	Output adder delay for the CTT I/O standard	
AGP	Output adder delay for the AGP I/O standard	

Note to Tables 42 and 43:

(1) These delays report the differences in delays for different I/O standards. Add the delay for the I/O standard that is used to the external timing parameters.

(2) See Figure 36 for more information.

Table 57. EP20K600C f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.30		1.51		1.69	ns
t_{ESBSRC}		2.35		2.49		2.72	ns
t_{ESBAWC}		2.92		3.46		3.86	ns
t_{ESBSWC}		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
t_{ESBWAH}	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
t_{ESBWDH}	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
t_{ESBRAH}	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	–0.20		–0.24		–0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		–0.02		ns
$t_{ESBDATACO1}$		1.09		1.28		1.43	ns
$t_{ESBDATACO2}$		2.10		2.52		2.82	ns
t_{ESBDD}		2.50		2.97		3.32	ns
t_{PD}		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

Table 58. EP20K600C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.16		0.18	ns
t_{F5-20}		0.94		1.05		1.20	ns
t_{F20+}		1.76		1.98		2.23	ns

Table 63. EP20K1000C f_{MAX} ESB Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.48		1.57		1.65	ns
t_{ESBSRC}		2.36		2.50		2.73	ns
t_{ESBAWC}		2.93		3.46		3.86	ns
t_{ESBSWC}		3.08		3.43		3.83	ns
$t_{ESBWASU}$	0.51		0.50		0.52		ns
t_{ESBWAH}	0.38		0.51		0.57		ns
$t_{ESBWDSU}$	0.62		0.62		0.66		ns
t_{ESBWDH}	0.38		0.51		0.57		ns
$t_{ESBRASU}$	1.40		1.47		1.53		ns
t_{ESBRAH}	0.00		0.07		0.18		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	1.92		2.19		2.35		ns
$t_{ESBWADDRSU}$	–0.20		–0.28		–0.32		ns
$t_{ESBRADDRSU}$	0.00		–0.03		–0.05		ns
$t_{ESBDATACO1}$		1.12		1.30		1.46	ns
$t_{ESBDATACO2}$		2.11		2.53		2.84	ns
t_{ESBDD}		2.56		2.96		3.30	ns
t_{PD}		1.49		1.79		2.02	ns
$t_{PTERMSU}$	0.61		0.69		0.77		ns
$t_{PTERMCO}$		1.13		1.32		1.48	ns

Table 64. EP20K1000C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		1.13		1.31		1.50	ns
t_{F20+}		2.30		2.71		3.19	ns

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com