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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	271
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200cb356c7es

The APEX 20KC architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20KC architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by automatically linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 12. APEX 20KC FastRow Interconnect

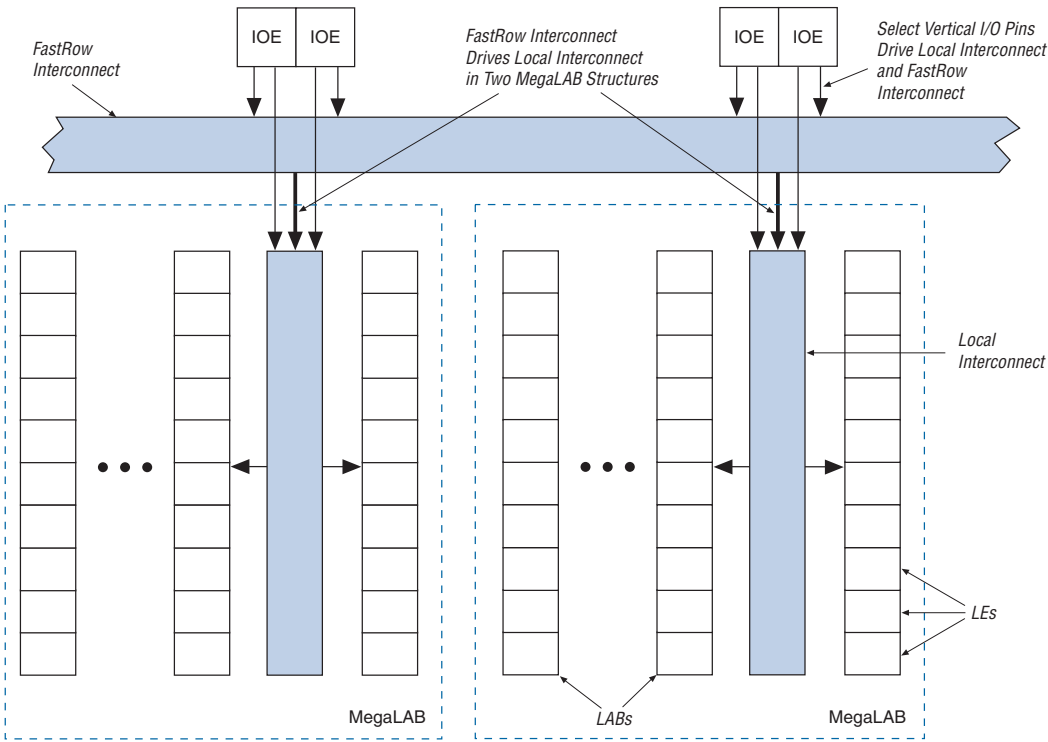


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

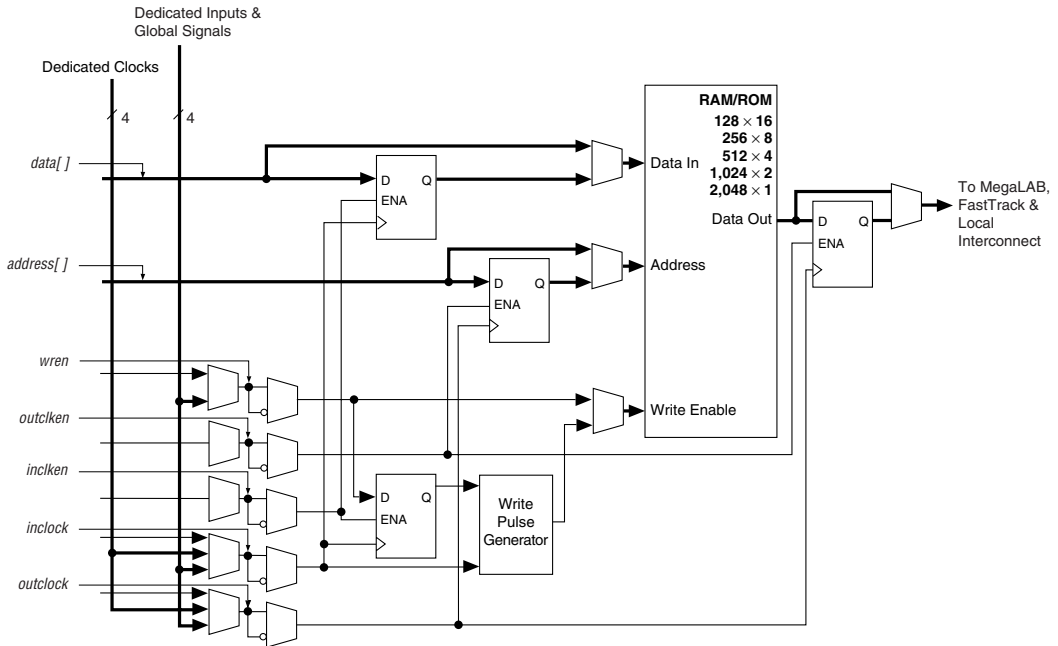
When implementing memory, each ESB can be configured in any of the following sizes: 128×16 , 256×8 , 512×4 , $1,024 \times 2$, or $2,048 \times 1$. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128×16 RAM blocks can be combined to form a 128×32 RAM block, and two 512×4 RAM blocks can be combined to form a 512×8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See [Figure 22](#).

Figure 22. ESB in Single-Port Mode *Note (1)*



Note to Figure 22:

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

[Table 9](#) describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

Table 9. APEX 20KC Programmable Delay Chains	
Programmable Delay	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin
Clock enable delay	Increase clock enable delay

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

Table 11. APEX 20KC ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	%
$t_{OUTJITTER}$	RMS jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	%
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
$t_{LOCK}^{(2), (3)}$	Time required for ClockLock or ClockBoost to acquire lock				40	μs

Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}^{(4)}$	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. [Tables 14 and 15](#) show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

Table 14. APEX 20KC Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K200C	1,164
EP20K400C	1,506
EP20K600C	1,806
EP20K1000C	2,190

Table 15. 32-Bit APEX 20KC Device IDCODE

Device	IDCODE (32 Bits) ⁽¹⁾			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) ⁽²⁾
EP20K200C	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K400C	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600C	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000C	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 15:

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.

[Figure 30](#) shows the timing requirements for the JTAG signals.

Jam Programming & Test Language Specification

Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those defined in the “Timing Model” section on page 65. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

Table 17. APEX 20KC Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage	With respect to ground (2)	–0.5	2.5	V
V _{CCIO}			–0.5	4.6	V
V _I	DC input voltage		–0.5	4.6	V
I _{OUT}	DC output current, per pin		–25	25	mA
T _{STG}	Storage temperature	No bias	–65	150	° C
T _{AMB}	Ambient temperature	Under bias	–65	135	° C
T _J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	(2), (5)	-0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	-40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current (8)	$V_I = 3.6$ to 0.0 V	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current (8)	$V_O = 4.1$ to -0.5 V	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	$V_I =$ ground, no load, no toggling inputs, -7 speed grade		10		mA
		$V_I =$ ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (9)	20		50	k Ω
		$V_{CCIO} = 2.375$ V (9)	30		80	k Ω
		$V_{CCIO} = 1.71$ V (9)	60		150	k Ω



DC operating specifications on APEX 20KC I/O standards are listed in Tables 21 to 35.

Table 22. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or }3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OH} = -0.1\text{ mA}$ (1)	$V_{CCIO} - 0.2$		V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OL} = 0.1\text{ mA}$ (2)		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or }3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = -0.1\text{ mA}$ (1)	2.1		V
		$I_{OH} = -1\text{ mA}$ (1)	2.0		V
		$I_{OH} = -2\text{ mA}$ (1)	1.7		V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1\text{ mA}$ (2)		0.2	V
		$I_{OL} = 1\text{ mA}$ (2)		0.4	V
		$I_{OL} = 2\text{ mA}$ (2)		0.7	V

Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 36 \text{ mA}$ (2)			0.65	V

Table 29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -7.6 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 7.6 \text{ mA}$ (2)			$V_{TT} - 0.57$	V

Table 30. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -15.2 \text{ mA}$ (1)	$V_{TT} + 0.76$			V
V_{OL}	Low-level output voltage	$I_{OL} = 15.2 \text{ mA}$ (2)			$V_{TT} - 0.76$	V

Table 31. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (1)	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (2)			$V_{TT} - 0.6$	V

Table 32. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -16 \text{ mA}$ (1)	$V_{TT} + 0.8$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$ (2)			$V_{TT} - 0.8$	V

Table 33. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.1$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (1)	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (2)			0.4	V

Figure 36. AC Test Conditions for LVTTL, 2.5 V, 1.8 V, PCI & GTL+ I/O Standards

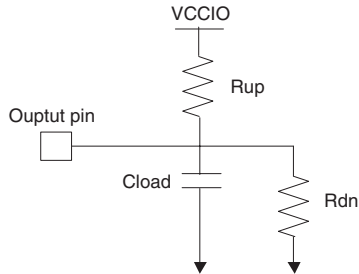


Figure 37. AC Test Conditions for SSTL-3 Class I & II I/O Standards

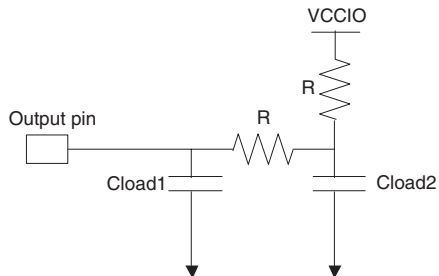


Figure 38. AC Test Conditions for the LVDS I/O Standard

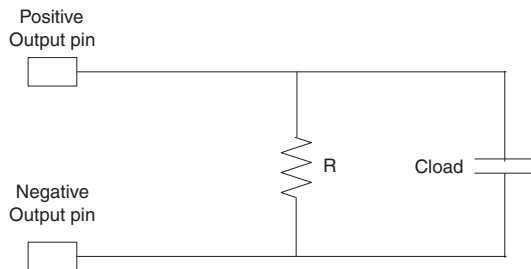


Table 46. EP20K200C t_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.20	ns
t_{F5-20}		0.81		0.94		1.12	ns
t_{F20+}		0.98		1.13		1.35	ns

Table 47. EP20K200C Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.33		1.66		2.00		ns
t_{CL}	1.33		1.66		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.33		1.66		2.00		ns
t_{ESBCL}	1.33		1.66		2.00		ns
t_{ESBWP}	1.05		1.28		1.44		ns
t_{ESBRP}	0.87		1.06		1.19		ns

Table 48. EP20K200C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.23		1.26		1.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	3.79	2.00	4.31	2.00	4.70	ns
$t_{INSUPLL}$	0.81		0.92		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.36	0.50	2.62	-	-	ns

Table 55. EP20K400C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	1.29		1.67		1.92		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.25	2.00	4.61	2.00	5.03	ns
t_{XZBIDIR}		6.55		6.97		7.35	ns
t_{ZXBIDIR}		6.55		6.97		7.36	ns
$t_{\text{INSUBIDIRPLL}}$	3.22		3.80		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.27	0.50	2.55	-	-	ns
$t_{\text{XZBIDIRPLL}}$		4.62		4.84		-	ns
$t_{\text{ZXBIDIRPLL}}$		4.62		4.84		-	ns

Table 56. EP20K600C t_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.65		0.78		0.92	ns

Table 59. EP20K600C Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.33		1.66		2.00		ns
t_{CL}	1.33		1.66		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.33		1.66		2.00		ns
t_{ESBCL}	1.33		1.66		2.00		ns
t_{ESBWP}	1.05		1.28		1.44		ns
t_{ESBRP}	0.87		1.06		1.19		ns

Table 60. EP20K600C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.28		1.40		1.45		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.37	0.50	2.63	-	-	ns

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		-0.52		-0.53		-0.56	ns
GTL+		-0.18		-0.29		-0.39	ns
SSTL-3 Class I		-0.67		-0.71		-0.75	ns
SSTL-3 Class II		-0.67		-0.71		-0.75	ns
SSTL-2 Class I		-0.67		-0.71		-0.75	ns
SSTL-2 Class II		-0.67		-0.71		-0.75	ns
LVDS		-0.69		-0.70		-0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at <http://www.altera.com>.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.