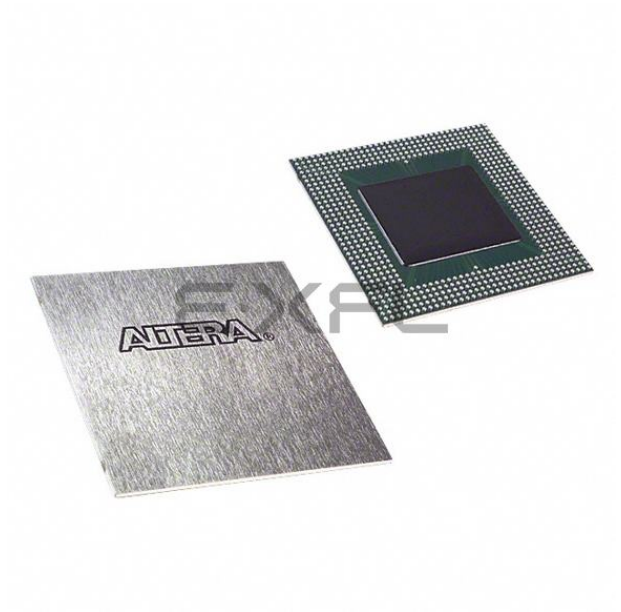

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	-
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200cb652c7

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count Notes (1), (2)			
Device	**484 Pin**	**672 Pin**	**1,020 Pin**
EP20K200C	376		
EP20K400C		488 (3)	
EP20K600C		508 (3)	588
EP20K1000C		508 (3)	708

Notes to Tables 3 and 4:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20KC device package types include plastic quad flat pack (PQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA™ packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20KC QFP & BGA Package Sizes				
Feature	**208-Pin PQFP**	**240-Pin PQFP**	**356-Pin BGA**	**652-Pin BGA**
Pitch (mm)	0.50	0.50	1.27	1.27
Area (mm^2)	924	1,218	1,225	2,025
Length × Width (mm × mm)	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

Table 6. APEX 20KC FineLine BGA Package Sizes			
Feature	**484 Pin**	**672 Pin**	**1,020 Pin**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	529	729	1,089
Length × Width (mm × mm)	23 × 23	27 × 27	33 × 33

General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

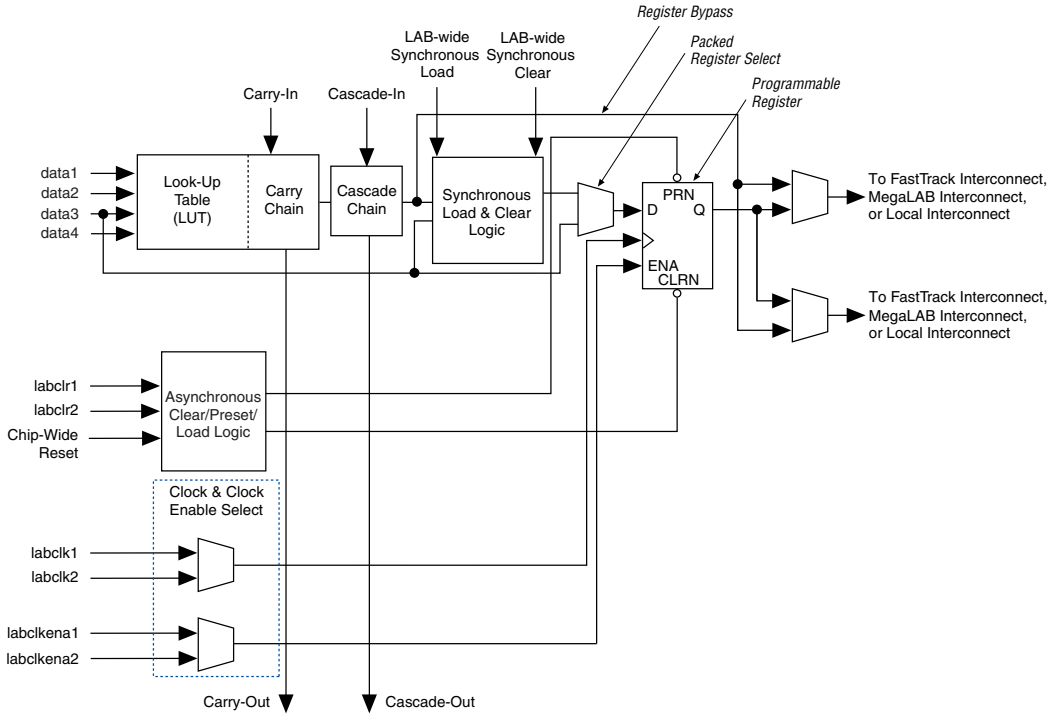
Table 7. APEX 20KC Device Features (Part 2 of 2)

Feature	APEX 20KC Devices
I/O standard support	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI and PCI-X 3.3-V AGP CTT GTL+ LVCMOS LVTTL True-LVDS™ and LVPECL data pins (in EP20K400C and larger devices) LVDS and LVPECL clock pins (in all devices) LVDS and LVPECL data pins up to 156 Mbps (in EP20K200C devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	CAM Dual-port RAM FIFO RAM ROM

All APEX 20KC devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault-coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20KC devices can be configured on the board for the specific functionality required.

APEX 20KC devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC16, EPC8, EPC4, EPC2, and EPC1 configuration devices and one-time programmable (OTP) EPC1 configuration devices, which configure APEX 20KC devices via a serial data stream. Moreover, APEX 20KC devices contain an optimized interface that permits microprocessors to configure APEX 20KC devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20KC devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

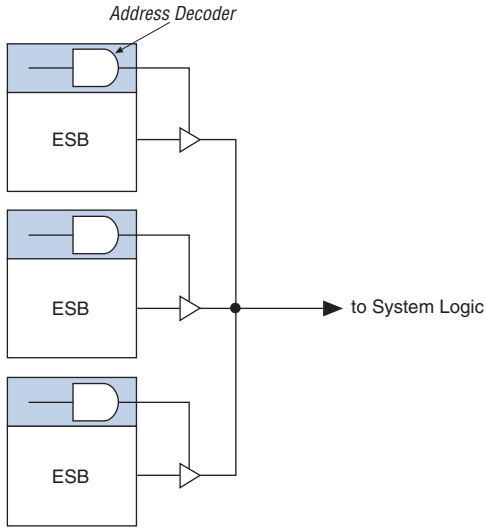
Figure 5. APEX 20KC Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

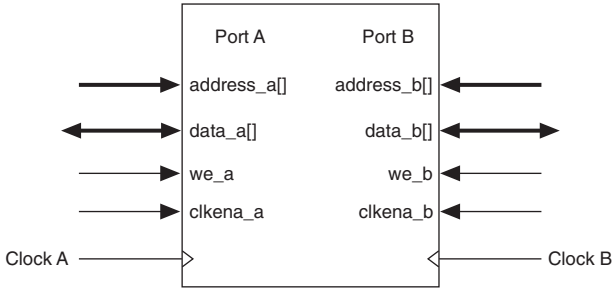
Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 19.

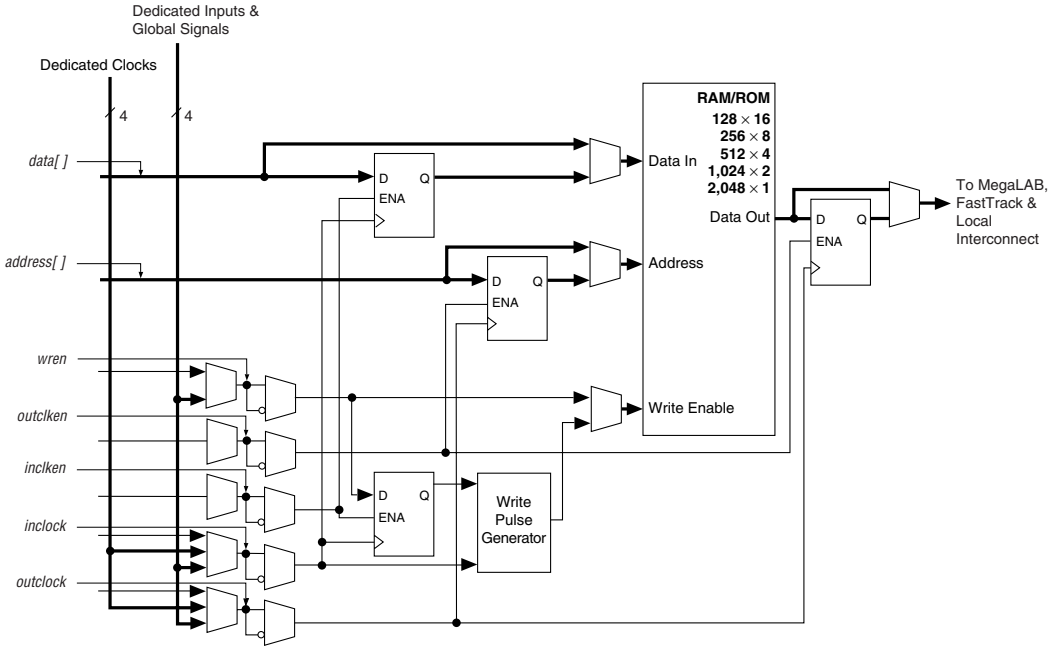
Figure 19. APEX 20KC ESB Implementing Dual-Port RAM



Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



Note to Figure 22:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20KC ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20KC device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20KC IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins.

The register in the APEX 20KC IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25 shows how fast bidirectional I/O pins are implemented in APEX 20KC devices. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)*

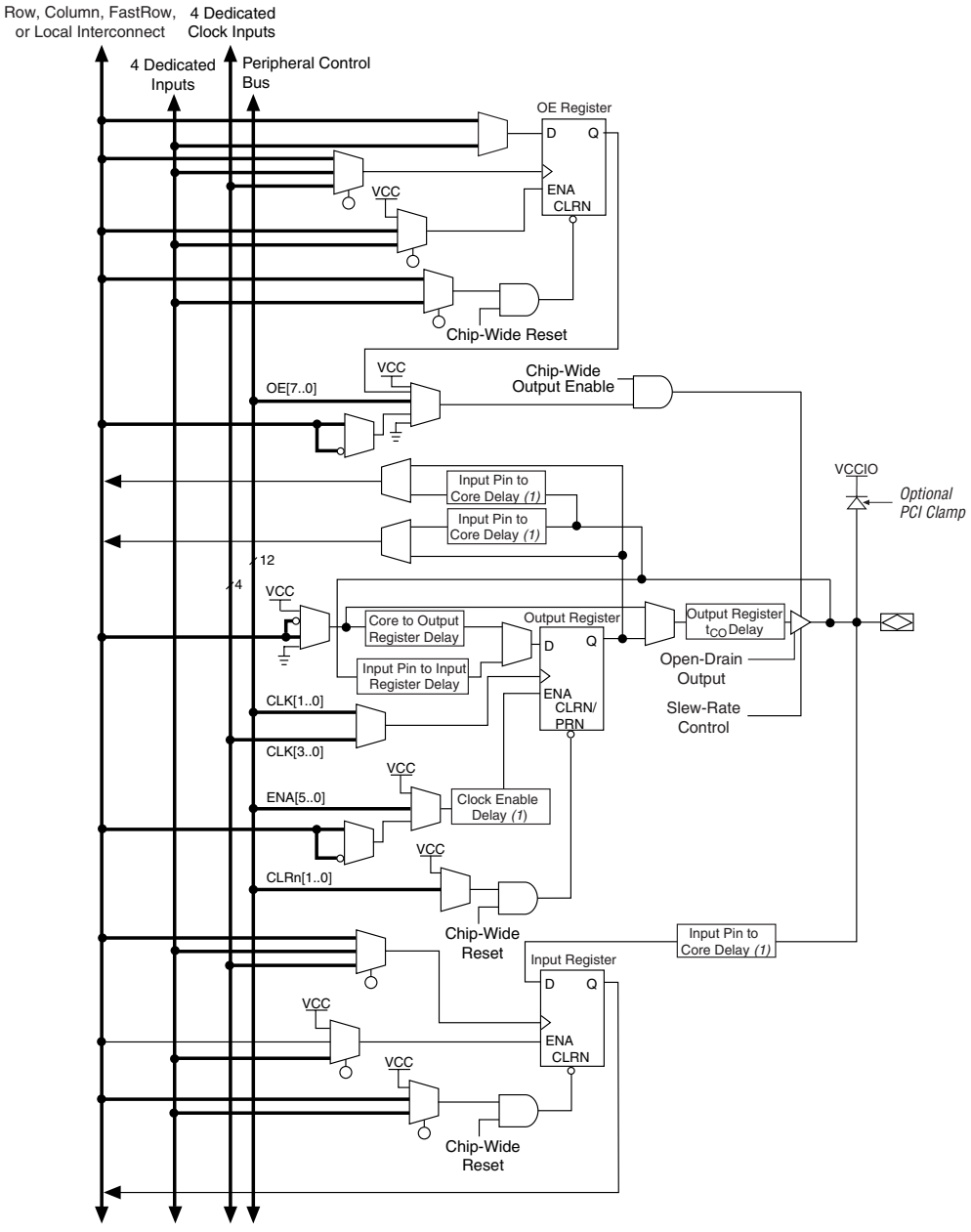
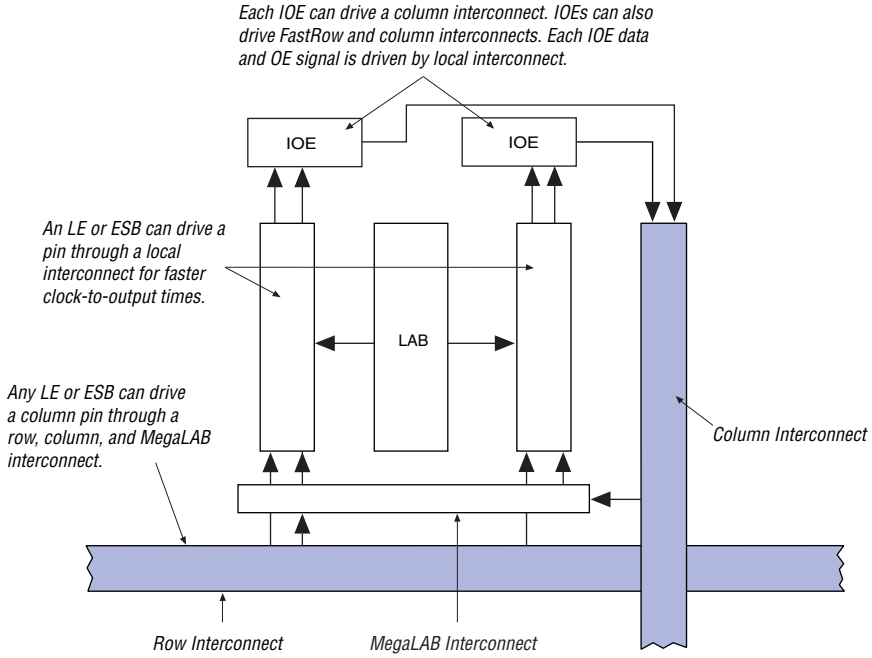


Figure 27 shows how a column IOE connects to the interconnect.

Figure 27. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

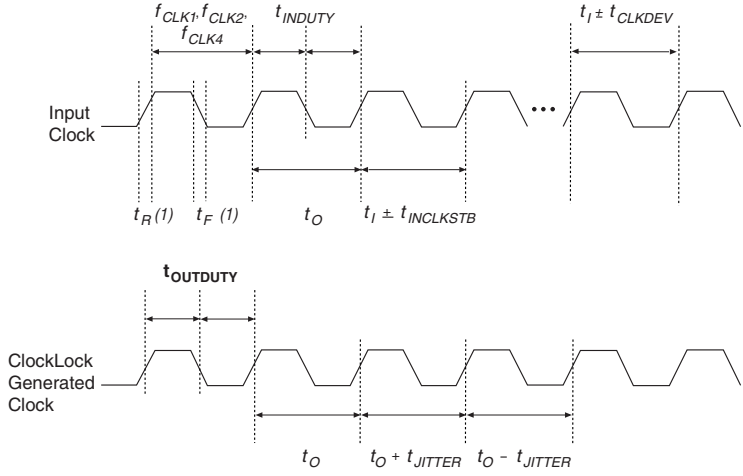
ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20KC ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KC devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 29 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Figure 29. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.



Note to Figure 29:

(1) Rise and fall times are measured from 10% to 90%.

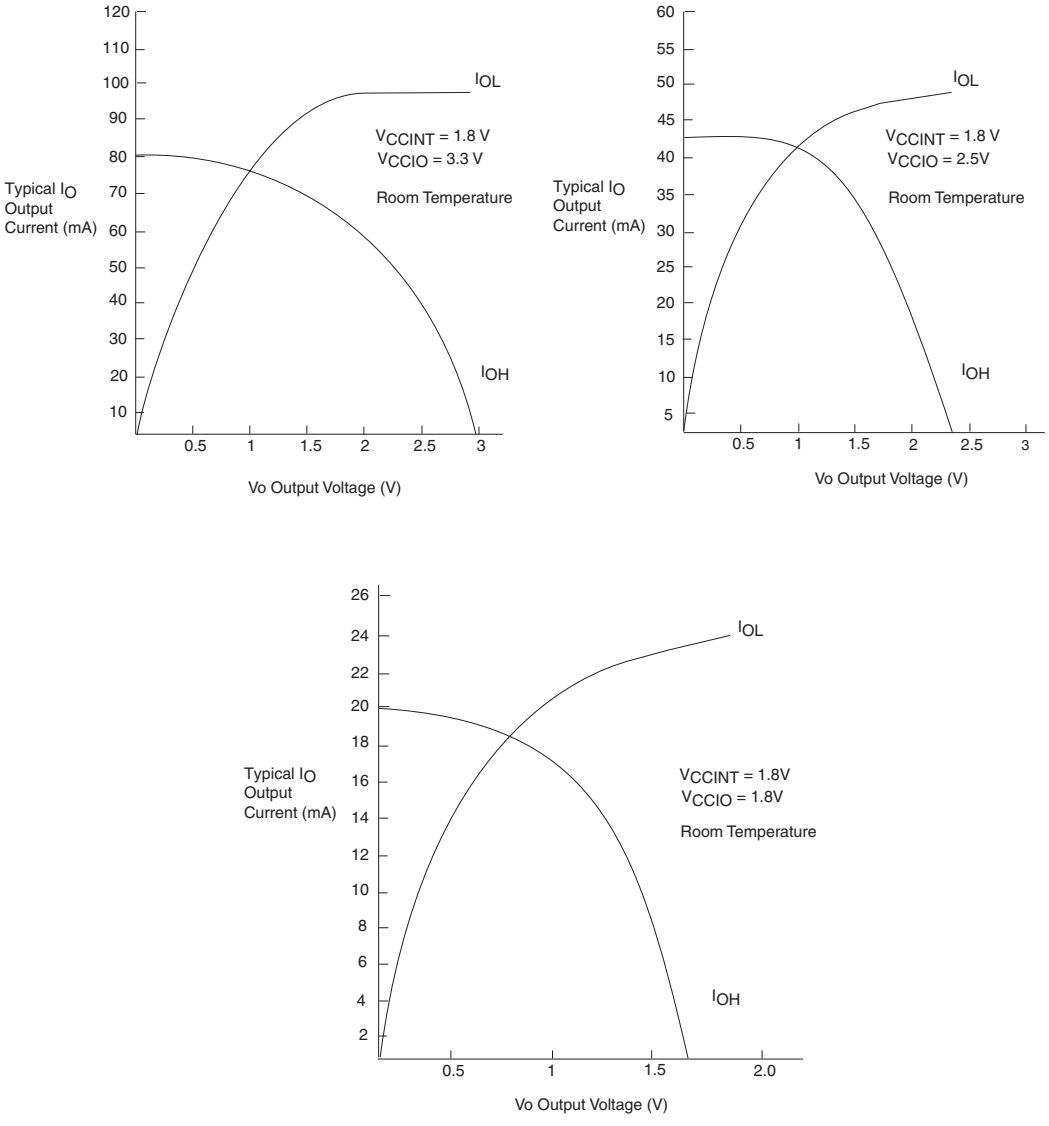
Table 32. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(2)*			V_{TT} – 0.8	V

Table 33. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			0.4	V

Figure 31. Output Drive Characteristics of APEX 20KC Devices *Note (1)*



Note to Figure 31:

(1) These are transient (AC) currents.

Table 41. APEX 20KC External Bidirectional Timing Parameters Note (1)		
Symbol	**Parameter**	**Condition**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	(2)
$t_{XZBIDIR}$	Synchronous output enable register to output buffer disable delay	(2)
$t_{ZXBIDIR}$	Synchronous output enable register to output buffer enable delay	(2)
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	(2)
$t_{XZBIDIRPLL}$	Synchronous output enable register to output buffer disable delay with PLL	(2)
$t_{ZXBIDIRPLL}$	Synchronous output enable register to output buffer enable delay with PLL	(2)

Notes to Tables 40 and 41:
(1) These timing parameters are sample-tested only.
(2) For more information, refer to Table 43.

Tables 42 and 43 define the timing delays for each I/O standard. Some output standards require test load circuits for AC timing measurements as shown in Figures 36 through 38.

Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 1 of 2) Note (1)		
Symbol	**Parameter**	**Condition**
LVCMOS	Input adder delay for the LVCMOS I/O standard	
LVTTL	Input adder delay for the LVTTL I/O standard	
2.5 V	Input adder delay for the 2.5-V I/O standard	
1.8 V	Input adder delay for the 1.8-V I/O standard	
PCI	Input adder delay for the PCI I/O standard	
GTl+	Input adder delay for the GTL+ I/O standard	
SSTL-3 Class I	Input adder delay for the SSTL-3 Class I I/O standard	
SSTL-3 Class II	Input adder delay for the SSTL-3 Class II I/O standard	
SSTL-2 Class I	Input adder delay for the SSTL -2 Class I I/O standard	
SSTL-2 Class II	Input adder delay for the SSTL -2 Class II I/O standard	

Table 49. EP20K200C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.38		1.78		1.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	3.79	2.00	4.31	2.00	4.70	ns
$t_{XZBIDIR}$		6.12		6.51		7.89	ns
$t_{ZXBIDIR}$		6.12		6.51		7.89	ns
$t_{INSUBIDIRPLL}$	2.82		3.47		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.36	0.50	2.62	-	-	ns
$t_{XZBIDIRPLL}$		4.69		4.82		-	ns
$t_{ZXBIDIRPLL}$		4.69		4.82		-	ns

Table 50. EP20K400C f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.65		0.78		0.92	ns

Table 51. EP20K400C f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.30		1.51		1.69	ns
t_{ESBSRC}		2.35		2.49		2.72	ns
t_{ESBAWC}		2.92		3.46		3.86	ns
t_{ESBSWC}		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
t_{ESBWAH}	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
t_{ESBWDH}	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
t_{ESBRAH}	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	–0.20		–0.24		–0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		–0.02		ns
$t_{ESBDATACO1}$		1.09		1.28		1.43	ns
$t_{ESBDATACO2}$		2.10		2.52		2.82	ns
t_{ESBDD}		2.50		2.97		3.32	ns
t_{PD}		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

Table 52. EP20K400C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		0.94		1.06		1.25	ns
t_{F20+}		1.73		1.96		2.30	ns

Table 59. EP20K600C Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.33		1.66		2.00		ns
t_{CL}	1.33		1.66		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.33		1.66		2.00		ns
t_{ESBCL}	1.33		1.66		2.00		ns
t_{ESBWP}	1.05		1.28		1.44		ns
t_{ESBRP}	0.87		1.06		1.19		ns

Table 60. EP20K600C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.28		1.40		1.45		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.37	0.50	2.63	-	-	ns

Table 67. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.86		2.54		3.15		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.63	2.00	5.26	2.00	5.69	ns
$t_{XZBIDIR}$		8.98		9.89		10.67	ns
$t_{ZXBIDIR}$		8.98		9.89		10.67	ns
$t_{INSUBIDIRPLL}$	4.17		5.27		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.32	0.50	2.55	-	-	ns
$t_{XZBIDIRPLL}$		6.67		7.18		-	ns
$t_{ZXBIDIRPLL}$		6.67		7.18		-	ns

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 68. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		0.04		0.11		0.14	ns
PCI		0.00		0.04		0.03	ns
GTL+		–0.30		0.25		0.23	ns
SSTL-3 Class I		–0.19		–0.13		–0.13	ns
SSTL-3 Class II		–0.19		–0.13		–0.13	ns
SSTL-2 Class I		–0.19		–0.13		–0.13	ns
SSTL-2 Class II		–0.19		–0.13		–0.13	ns
LVDS		–0.19		–0.17		–0.16	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 70), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20KC devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 70. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC16, EPC8, EPC4, EPC2, or EPC1 configuration device
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam Standard Test and Programming Language (STAPL) or JBC File

For more information on configuration, see *Application Note 116 (Configuring SRAM-Based LUT Devices)*.

Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information.

Ordering Information

Figure 39 describes the ordering codes for Stratix devices. For more information on a specific package, refer to the *Altera Device Package Information Data Sheet*.