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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	-
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200cb652c8

- Advanced interconnect structure
 - Copper interconnect for high performance
 - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
 - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions optimized for APEX 20KC architecture available
 - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
 - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
 - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP & BGA Package Options & I/O Count *Notes (1), (2)*

Device	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K200C	136	168	271	
EP20K400C				488
EP20K600C				488
EP20K1000C				488

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	484 Pin	672 Pin	1,020 Pin
EP20K200C	376		
EP20K400C		488 (3)	
EP20K600C		508 (3)	588
EP20K1000C		508 (3)	708

Notes to Tables 3 and 4:

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20KC device package types include plastic quad flat pack (PQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA™ packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20KC QFP & BGA Package Sizes

Feature	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
Pitch (mm)	0.50	0.50	1.27	1.27
Area (mm ²)	924	1,218	1,225	2,025
Length × Width (mm × mm)	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

Table 6. APEX 20KC FineLine BGA Package Sizes

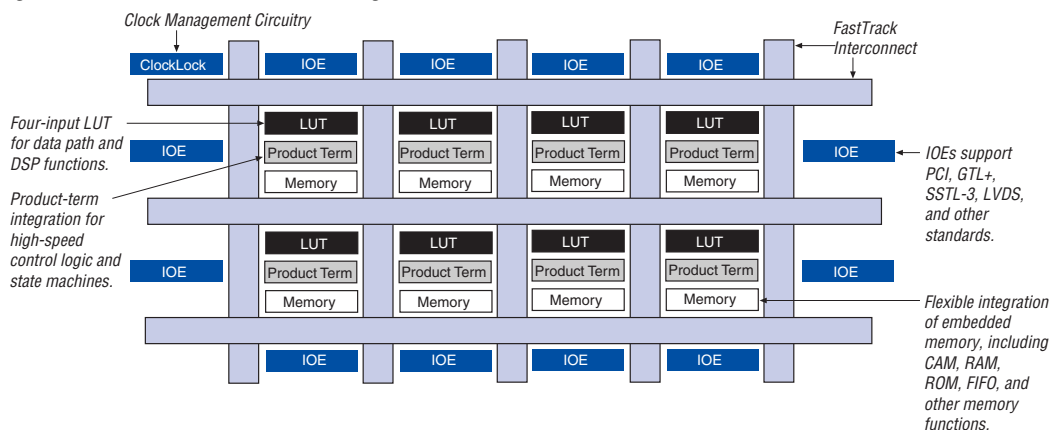
Feature	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00
Area (mm ²)	529	729	1,089
Length × Width (mm × mm)	23 × 23	27 × 27	33 × 33

General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

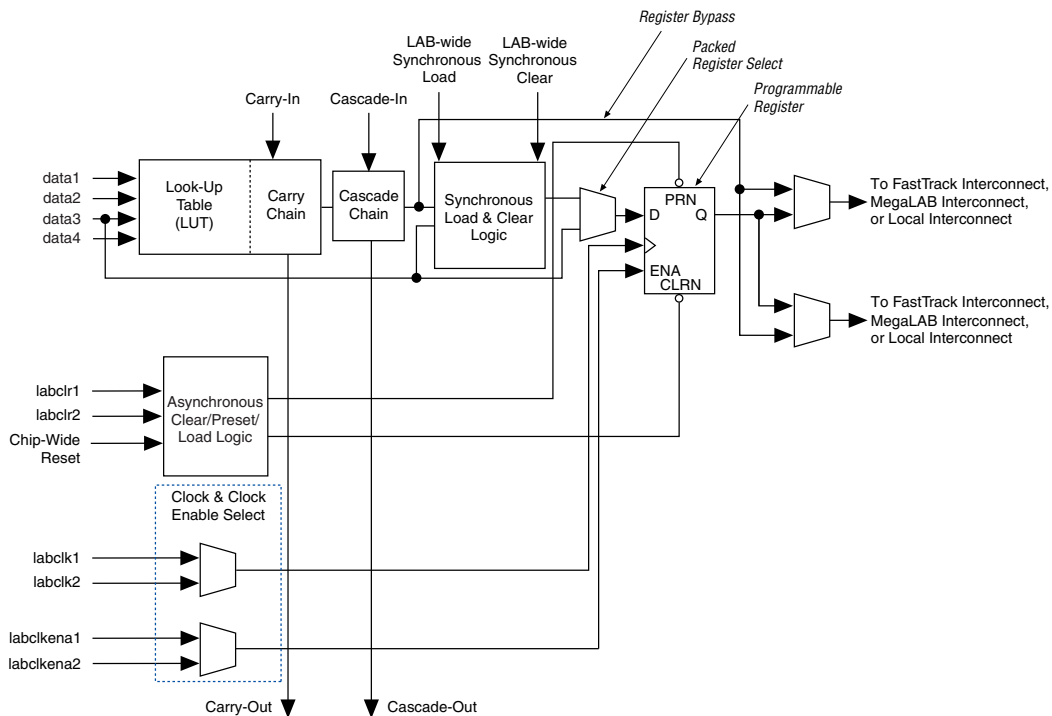
The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

Figure 1. APEX 20KC Device Block Diagram



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

Figure 5. APEX 20KC Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20KC architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

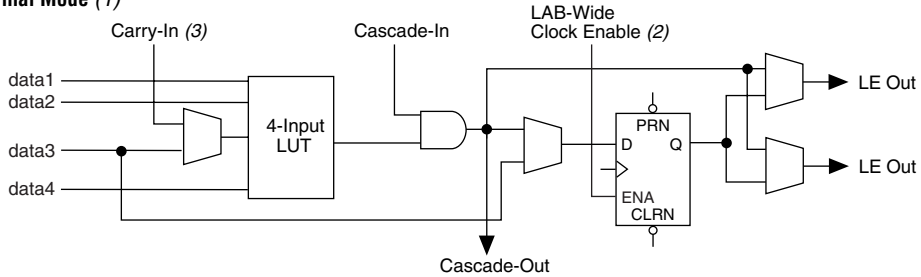
The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20KC architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by automatically linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

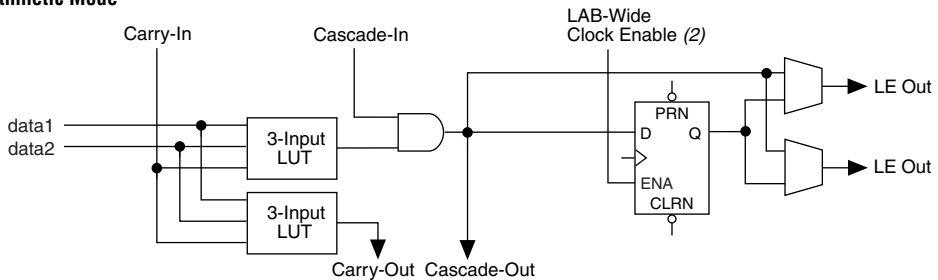
Figure 6 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 8. APEX 20KC LE Operating Modes

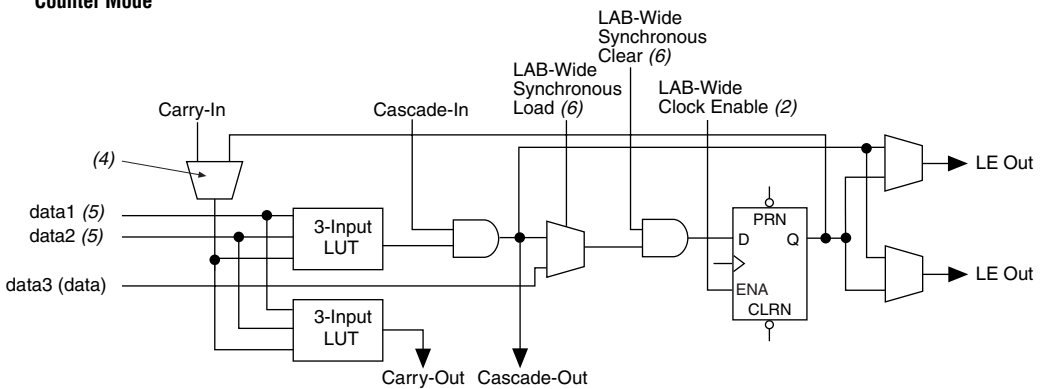
Normal Mode (1)



Arithmetic Mode



Counter Mode



Notes to Figure 8:

- (1) LEs in normal mode support register packing.
- (2) There are two LAB-wide clock enables per LAB.
- (3) When using the carry-in in normal mode, the packed register feature is unavailable.
- (4) A register feedback multiplexer is available on LE1 of each LAB.
- (5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
- (6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Figure 10. FastTrack Connection to Local Interconnect

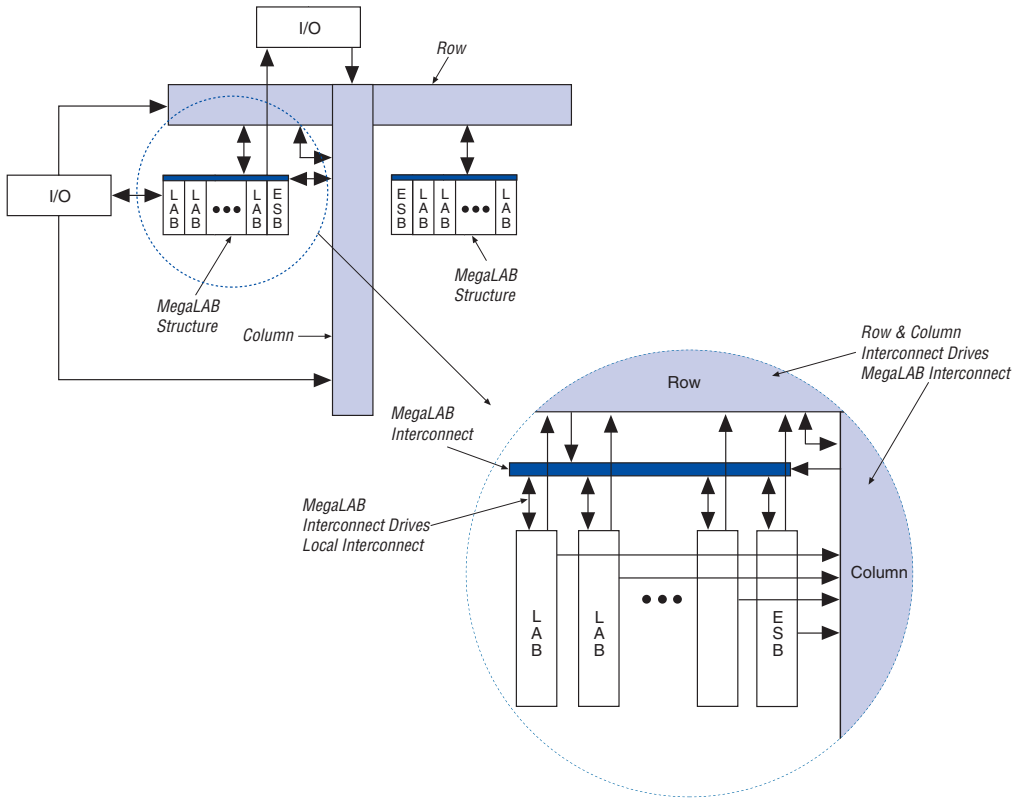
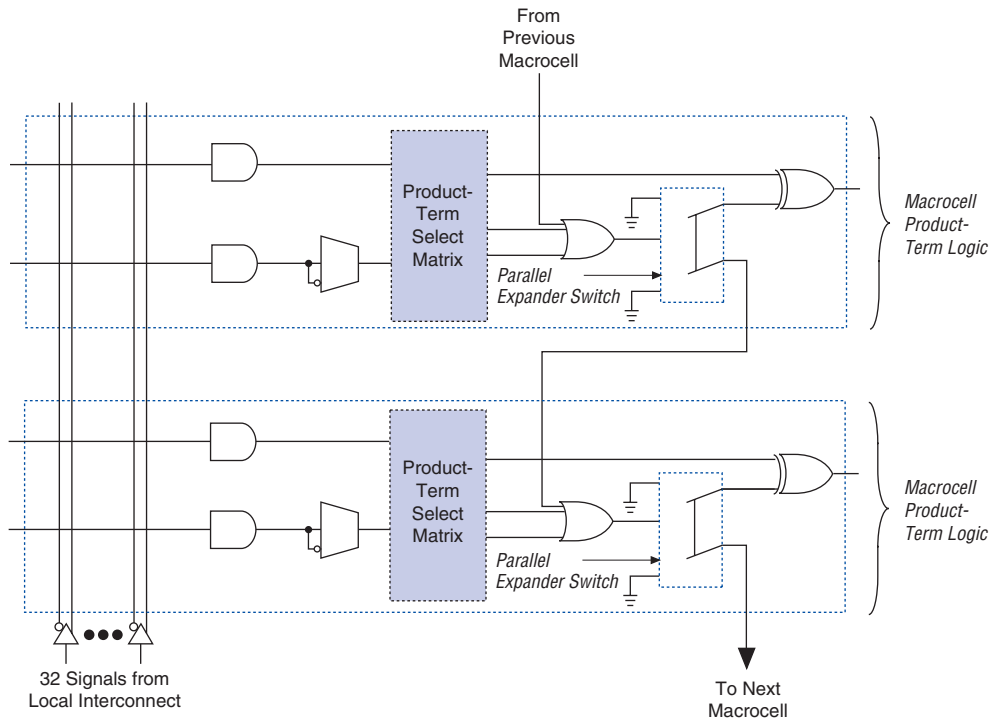


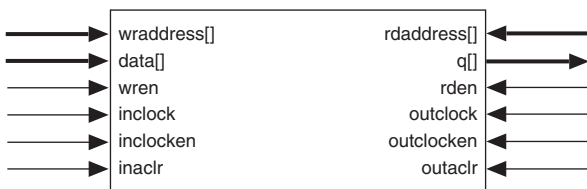
Figure 16. APEX 20KC Parallel Expanders



Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

Figure 17. ESB Block Diagram



CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Advanced I/O Standard Support

APEX 20KC IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

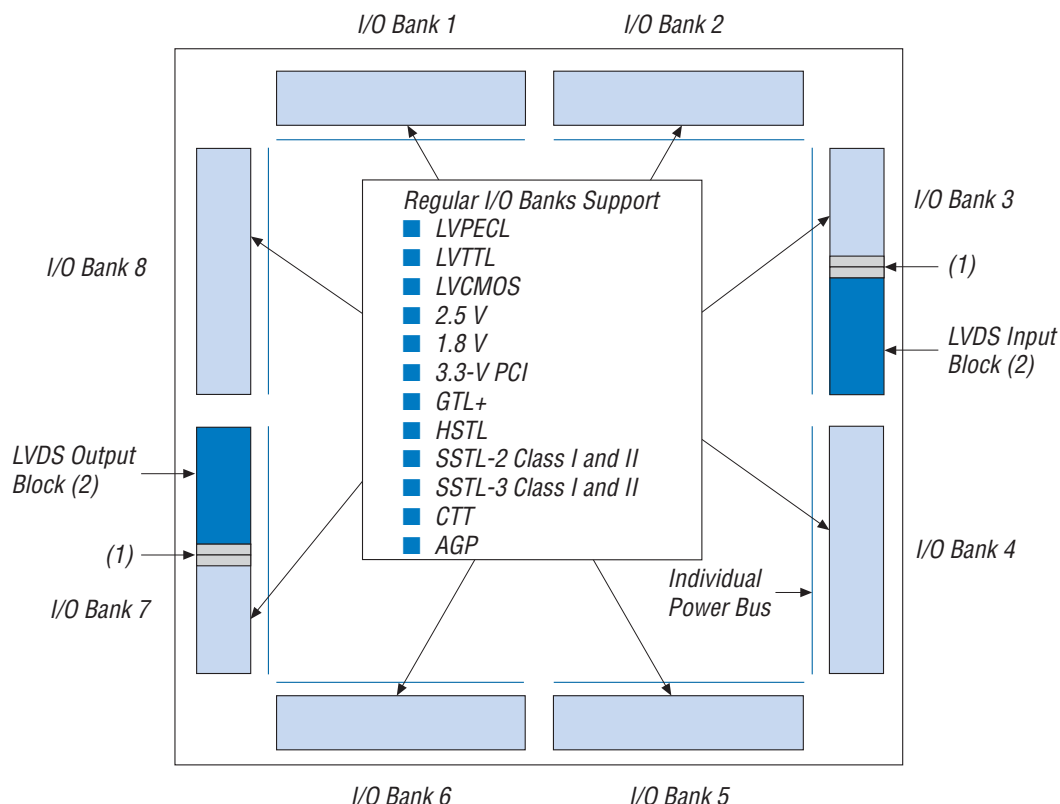


For more information on I/O standards supported by APEX 20KC devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KC device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL at up to 156 Mbps per channel with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own V_{CCIO} pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K400C and larger APEX 20KC devices support the LVDS interface for data pins (EP20K200C devices support LVDS clock pins, but not data pins). EP20K400C and EP20K600C devices support LVDS for data pins at up to 840 Mbps per channel. EP20K1000C devices support LVDS on 16 channels at up to 750 Mbps.

Each bank can support multiple standards with the same V_{CCIO} for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for the LVDS I/O standard, they support all of the other I/O standards. [Figure 28](#) shows the arrangement of the APEX 20KC I/O banks.

Figure 28. APEX 20KC I/O Banks

Notes to Figure 28:

- (1) For more information on placing I/O pins in LVDS blocks, refer to the “Guidelines for Using LVDS Blocks” section in [Application Note 120 \(Using LVDS in APEX 20KE Devices\)](#).
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20KC devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Figure 30. APEX 20KC JTAG Waveforms

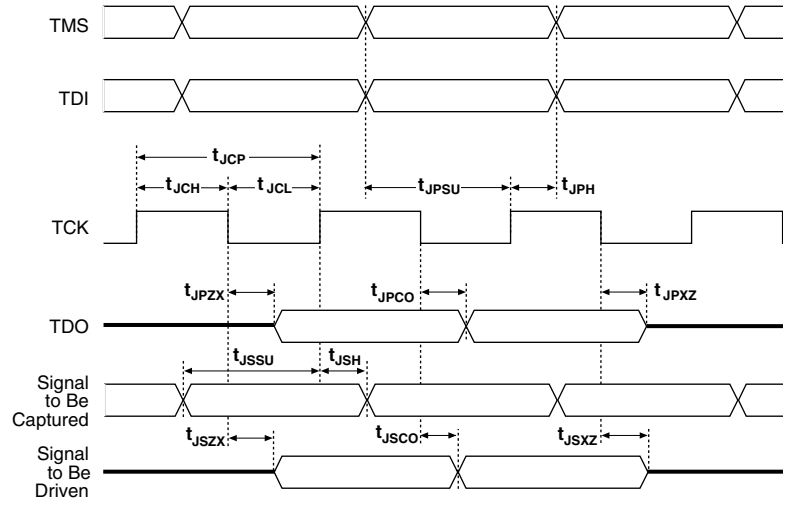


Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

Table 16. APEX 20KC JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- [Application Note 39 \(IEEE Std. 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#)

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	(2), (5)	-0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	-40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current (8)	$V_I = 3.6$ to 0.0 V	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current (8)	$V_O = 4.1$ to -0.5 V	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	$V_I =$ ground, no load, no toggling inputs, -7 speed grade		10		mA
		$V_I =$ ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (9)	20		50	k Ω
		$V_{CCIO} = 2.375$ V (9)	30		80	k Ω
		$V_{CCIO} = 1.71$ V (9)	60		150	k Ω



DC operating specifications on APEX 20KC I/O standards are listed in [Tables 21 to 35](#).

Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 36 \text{ mA}$ (2)			0.65	V

Table 29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -7.6 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 7.6 \text{ mA}$ (2)			$V_{TT} - 0.57$	V

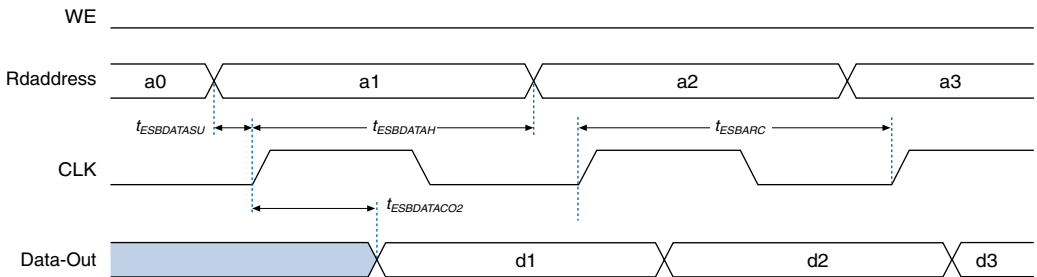
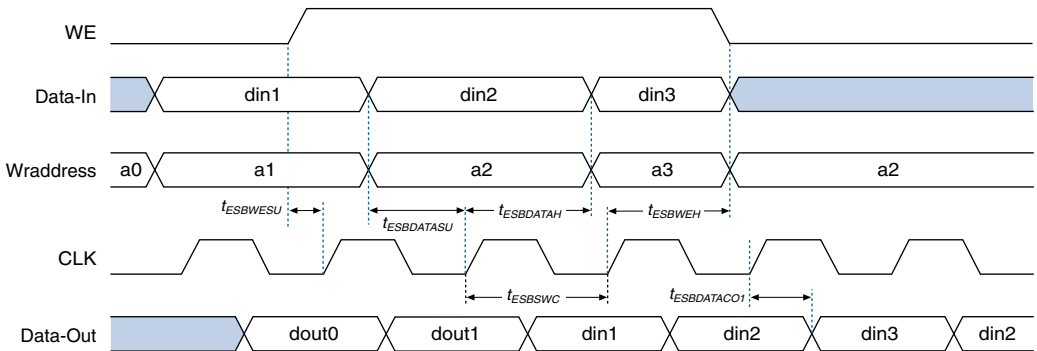
Figure 34. ESB Synchronous Timing Waveforms
ESB Synchronous Read

ESB Synchronous Write (ESB Output Registers Used)


Figure 35 shows the timing model for bidirectional I/O pin timing.

Table 51. EP20K400C t_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.30		1.51		1.69	ns
t_{ESBSRC}		2.35		2.49		2.72	ns
t_{ESBAWC}		2.92		3.46		3.86	ns
t_{ESBSWC}		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
t_{ESBWAH}	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
t_{ESBWDH}	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
t_{ESBRAH}	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	-0.20		-0.24		-0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		-0.02		ns
$t_{ESBDATAO1}$		1.09		1.28		1.43	ns
$t_{ESBDATAO2}$		2.10		2.52		2.82	ns
t_{ESBDD}		2.50		2.97		3.32	ns
t_{PD}		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

Table 52. EP20K400C t_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		0.94		1.06		1.25	ns
t_{F20+}		1.73		1.96		2.30	ns

Table 61. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.03		2.57		2.97		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
t_{XZBIDIR}		8.31		9.14		9.76	ns
t_{ZXBIDIR}		8.31		9.14		9.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.99		4.77		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.37	0.50	2.63	-	-	ns
$t_{\text{XZBIDIRPLL}}$		6.35		6.94		-	ns
$t_{\text{ZXBIDIRPLL}}$		6.35		6.94		-	ns

Table 62. EP20K1000C t_{MAX} LE Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.66		0.79		0.92	ns

Table 63. EP20K1000C t_{MAX} ESB Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.48		1.57		1.65	ns
t_{ESBSRC}		2.36		2.50		2.73	ns
t_{ESBAWC}		2.93		3.46		3.86	ns
t_{ESBSWC}		3.08		3.43		3.83	ns
$t_{ESBWASU}$	0.51		0.50		0.52		ns
t_{ESBWAH}	0.38		0.51		0.57		ns
$t_{ESBWDSU}$	0.62		0.62		0.66		ns
t_{ESBWDH}	0.38		0.51		0.57		ns
$t_{ESBRASU}$	1.40		1.47		1.53		ns
t_{ESBRAH}	0.00		0.07		0.18		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	1.92		2.19		2.35		ns
$t_{ESBWADDRSU}$	-0.20		-0.28		-0.32		ns
$t_{ESBRADDRSU}$	0.00		-0.03		-0.05		ns
$t_{ESBDATAO1}$		1.12		1.30		1.46	ns
$t_{ESBDATAO2}$		2.11		2.53		2.84	ns
t_{ESBDD}		2.56		2.96		3.30	ns
t_{PD}		1.49		1.79		2.02	ns
$t_{PTERMSU}$	0.61		0.69		0.77		ns
$t_{PTERMCO}$		1.13		1.32		1.48	ns

Table 64. EP20K1000C t_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		1.13		1.31		1.50	ns
t_{F20+}		2.30		2.71		3.19	ns

Table 67. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	1.86		2.54		3.15		ns
t_{INHBDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.63	2.00	5.26	2.00	5.69	ns
t_{XZBIDIR}		8.98		9.89		10.67	ns
t_{ZXBIDIR}		8.98		9.89		10.67	ns
$t_{\text{INSUBDIRPLL}}$	4.17		5.27		-		ns
$t_{\text{INHBDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.32	0.50	2.55	-	-	ns
$t_{\text{XZBIDIRPLL}}$		6.67		7.18		-	ns
$t_{\text{ZXBIDIRPLL}}$		6.67		7.18		-	ns

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 68. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		0.04		0.11		0.14	ns
PCI		0.00		0.04		0.03	ns
GTL+		-0.30		0.25		0.23	ns
SSTL-3 Class I		-0.19		-0.13		-0.13	ns
SSTL-3 Class II		-0.19		-0.13		-0.13	ns
SSTL-2 Class I		-0.19		-0.13		-0.13	ns
SSTL-2 Class II		-0.19		-0.13		-0.13	ns
LVDS		-0.19		-0.17		-0.16	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		-0.52		-0.53		-0.56	ns
GTL+		-0.18		-0.29		-0.39	ns
SSTL-3 Class I		-0.67		-0.71		-0.75	ns
SSTL-3 Class II		-0.67		-0.71		-0.75	ns
SSTL-2 Class I		-0.67		-0.71		-0.75	ns
SSTL-2 Class II		-0.67		-0.71		-0.75	ns
LVDS		-0.69		-0.70		-0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at <http://www.altera.com>.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.