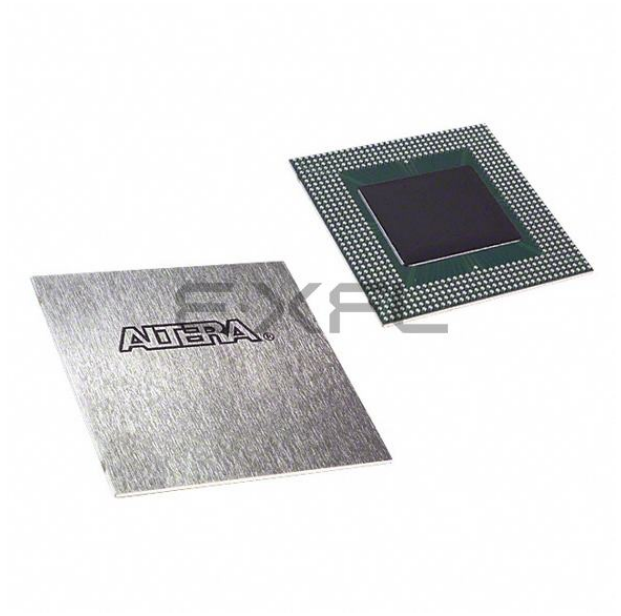

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	-
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200cb652c9

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count Notes (1), (2)			
Device	**484 Pin**	**672 Pin**	**1,020 Pin**
EP20K200C	376		
EP20K400C		488 (3)	
EP20K600C		508 (3)	588
EP20K1000C		508 (3)	708

Notes to Tables 3 and 4:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20KC device package types include plastic quad flat pack (PQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA™ packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20KC QFP & BGA Package Sizes				
Feature	**208-Pin PQFP**	**240-Pin PQFP**	**356-Pin BGA**	**652-Pin BGA**
Pitch (mm)	0.50	0.50	1.27	1.27
Area (mm^2)	924	1,218	1,225	2,025
Length × Width (mm × mm)	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

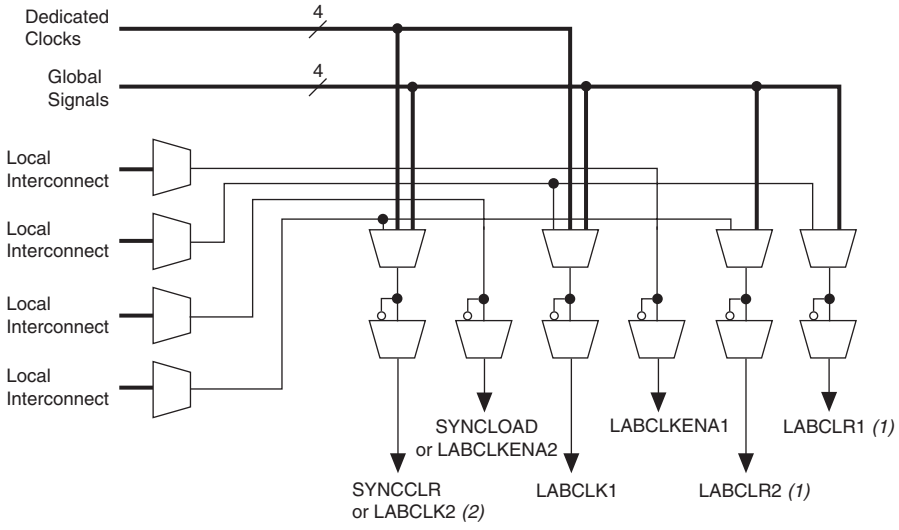
Table 6. APEX 20KC FineLine BGA Package Sizes			
Feature	**484 Pin**	**672 Pin**	**1,020 Pin**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	529	729	1,089
Length × Width (mm × mm)	23 × 23	27 × 27	33 × 33

General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE, the smallest unit of logic in the APEX 20KC architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Figure 12. APEX 20KC FastRow Interconnect

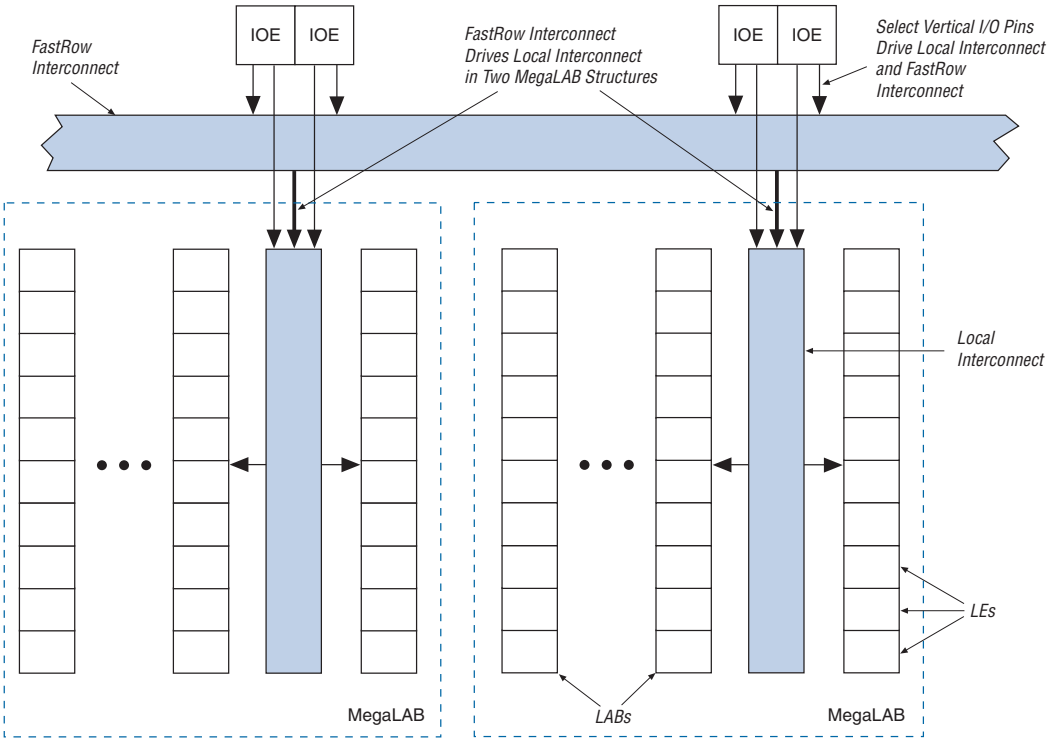
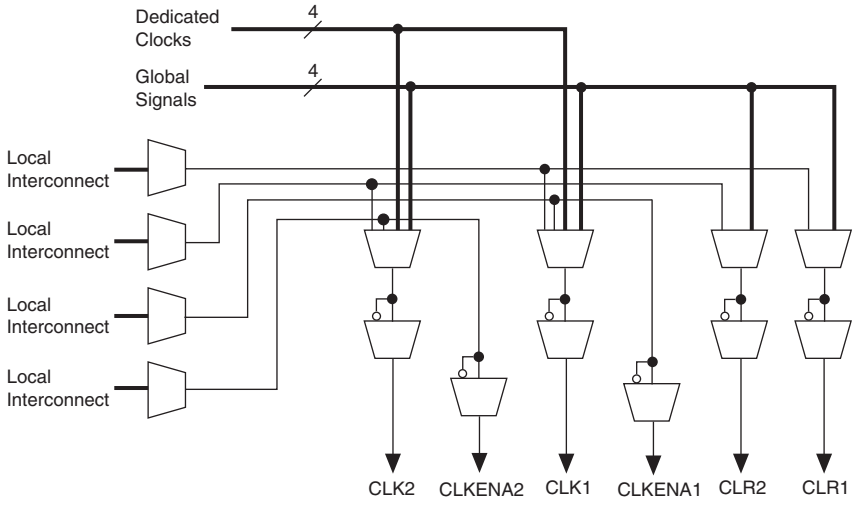


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Notes to Figure 25:
(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

Figure 26. Row IOE Connection to the Interconnect

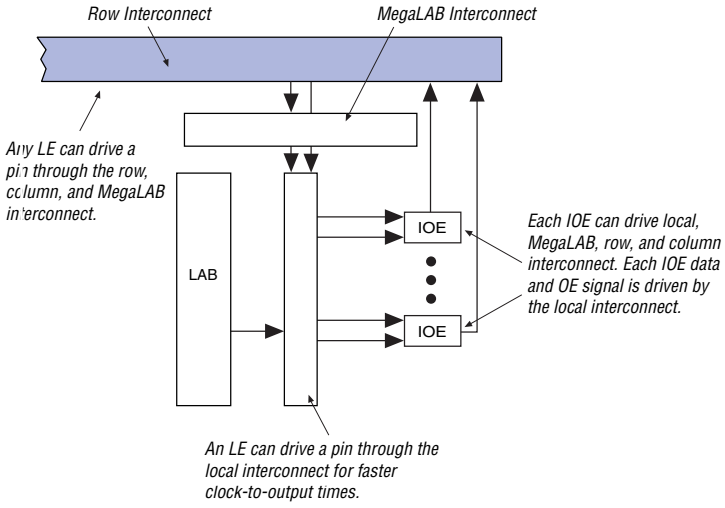
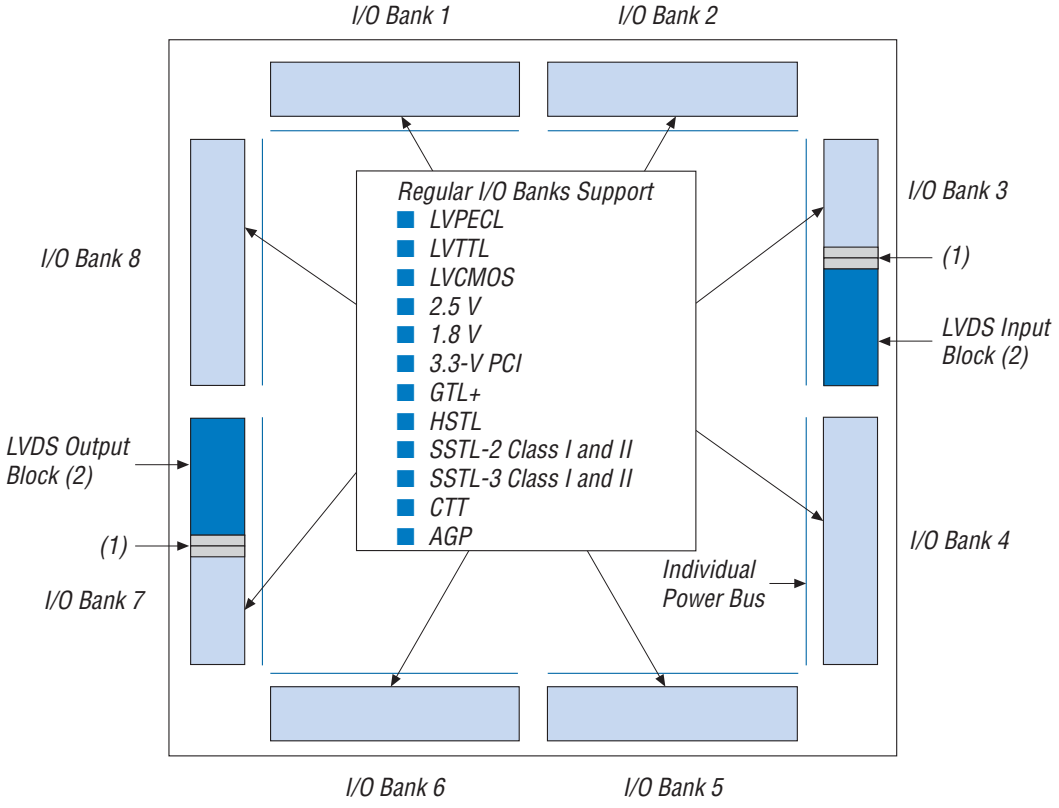


Figure 28. APEX 20KC I/O Banks



Notes to Figure 28:

(1) For more information on placing I/O pins in LVDS blocks, refer to the "Guidelines for Using LVDS Blocks" section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20KC devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes to Table 10:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades have PLLs and support the ClockLock and ClockBoost features.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 17 through 20:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and time periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KC device recommended operating conditions, shown in Table 18 on page 55.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(10) Capacitance is sample-tested only.

Tables 21 through 35 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –12 mA, V_{CCIO} = 3.0 V *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{CCIO} = 3.0 V *(2)*		0.4	V

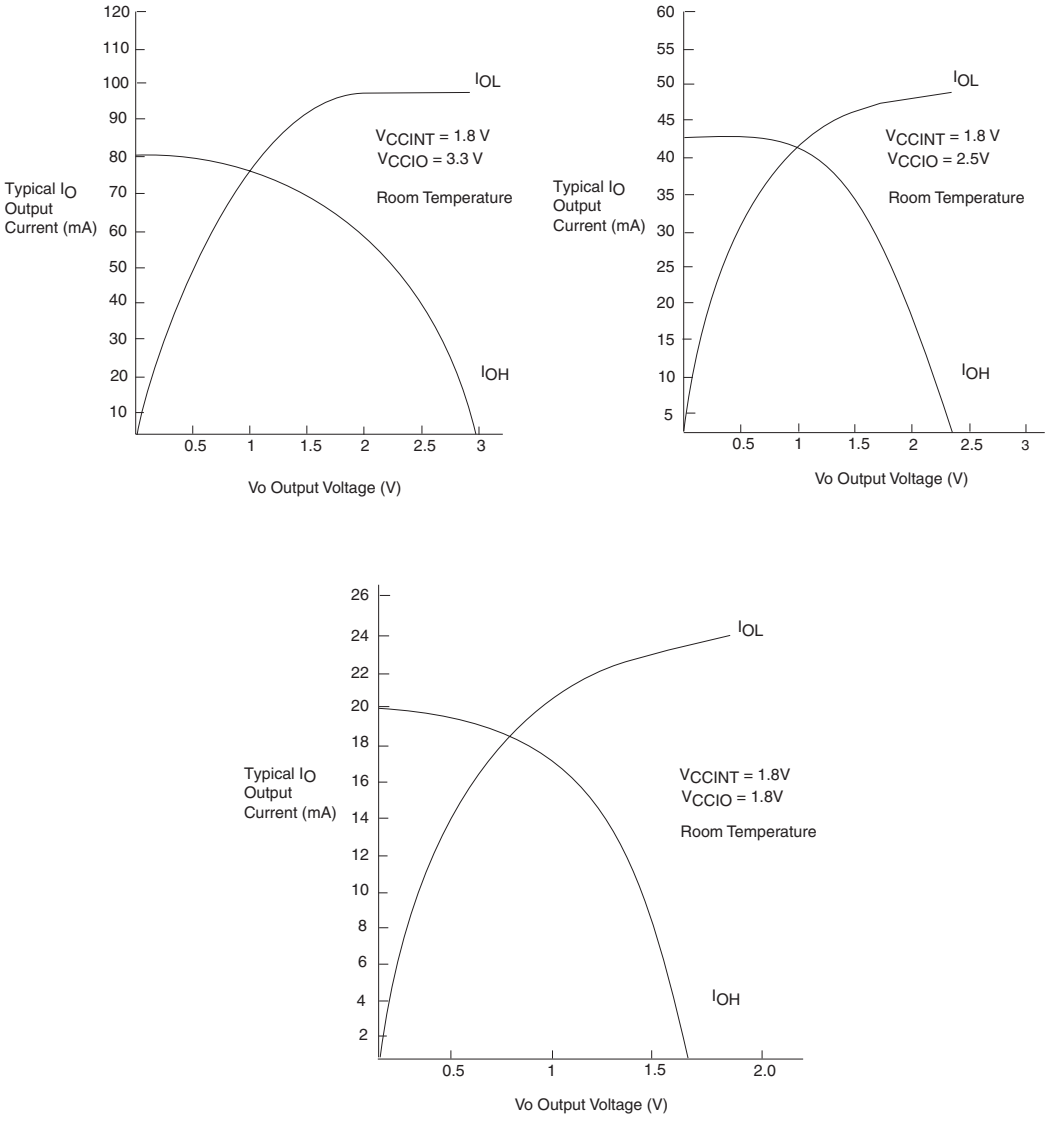
Table 26. 3.3-V PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
I_{IL}	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10.0		10.0	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
L_{pin}	Pin Inductance				15.0	nH

Table 27. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		650	mV
Δ V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX devices)		90	100	110	Ω

Figure 31. Output Drive Characteristics of APEX 20KC Devices *Note (1)*



Note to Figure 31:

(1) These are transient (AC) currents.

Figure 33. ESB Asynchronous Timing Waveforms

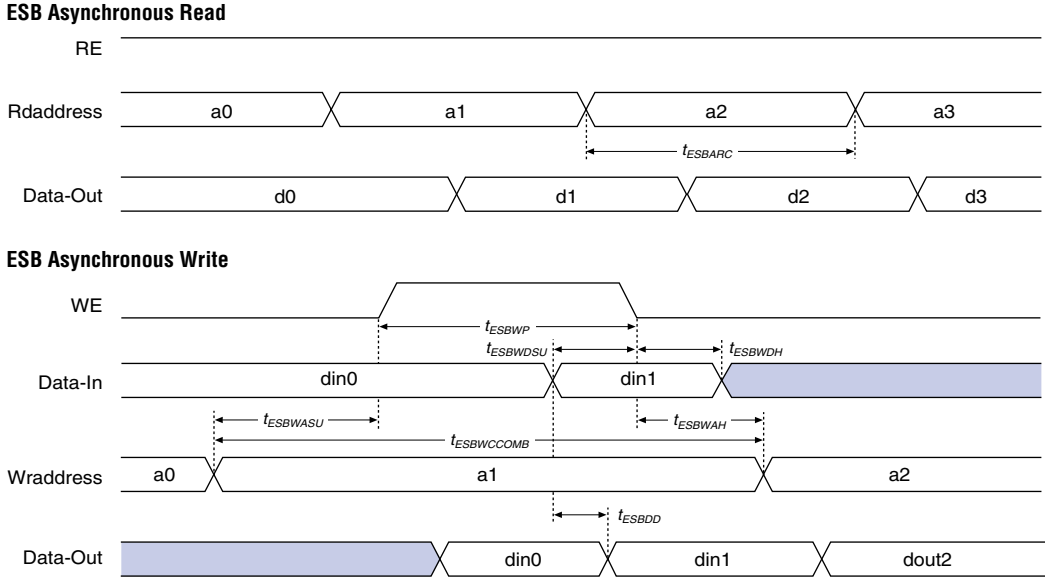


Figure 34. ESB Synchronous Timing Waveforms

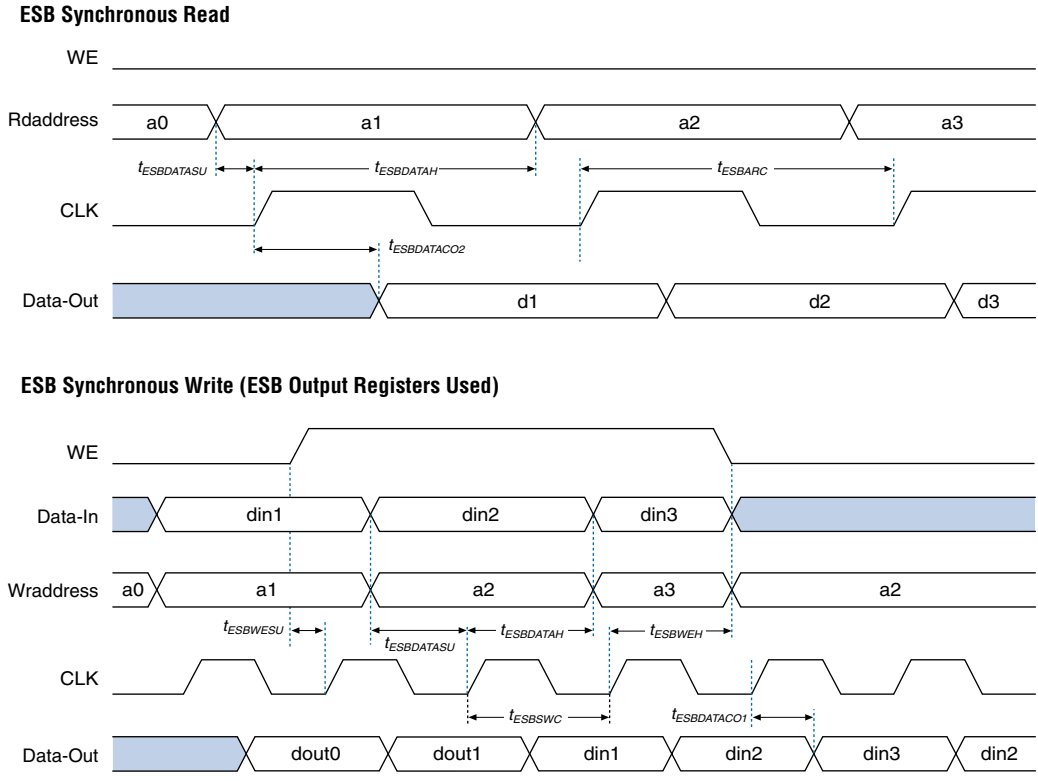


Figure 35 shows the timing model for bidirectional I/O pin timing.

Table 46. EP20K200C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.20	ns
t_{F5-20}		0.81		0.94		1.12	ns
t_{F20+}		0.98		1.13		1.35	ns

Table 47. EP20K200C Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.33		1.66		2.00		ns
t_{CL}	1.33		1.66		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.33		1.66		2.00		ns
t_{ESBCL}	1.33		1.66		2.00		ns
t_{ESBWP}	1.05		1.28		1.44		ns
t_{ESBRP}	0.87		1.06		1.19		ns

Table 48. EP20K200C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.23		1.26		1.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	3.79	2.00	4.31	2.00	4.70	ns
$t_{INSUPLL}$	0.81		0.92		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.36	0.50	2.62	-	-	ns

Table 61. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.03		2.57		2.97		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{XZBIDIR}$		8.31		9.14		9.76	ns
$t_{ZXBIDIR}$		8.31		9.14		9.76	ns
$t_{INSUBIDIRPLL}$	3.99		4.77		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.37	0.50	2.63	-	-	ns
$t_{XZBIDIRPLL}$		6.35		6.94		-	ns
$t_{ZXBIDIRPLL}$		6.35		6.94		-	ns

Table 62. EP20K1000C f_{MAX} LE Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.66		0.79		0.92	ns

Table 63. EP20K1000C f_{MAX} ESB Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.48		1.57		1.65	ns
t_{ESBSRC}		2.36		2.50		2.73	ns
t_{ESBAWC}		2.93		3.46		3.86	ns
t_{ESBSWC}		3.08		3.43		3.83	ns
$t_{ESBWASU}$	0.51		0.50		0.52		ns
t_{ESBWAH}	0.38		0.51		0.57		ns
$t_{ESBWDSU}$	0.62		0.62		0.66		ns
t_{ESBWDH}	0.38		0.51		0.57		ns
$t_{ESBRASU}$	1.40		1.47		1.53		ns
t_{ESBRAH}	0.00		0.07		0.18		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	1.92		2.19		2.35		ns
$t_{ESBWADDRSU}$	–0.20		–0.28		–0.32		ns
$t_{ESBRADDRSU}$	0.00		–0.03		–0.05		ns
$t_{ESBDATACO1}$		1.12		1.30		1.46	ns
$t_{ESBDATACO2}$		2.11		2.53		2.84	ns
t_{ESBDD}		2.56		2.96		3.30	ns
t_{PD}		1.49		1.79		2.02	ns
$t_{PTERMSU}$	0.61		0.69		0.77		ns
$t_{PTERMCO}$		1.13		1.32		1.48	ns

Table 64. EP20K1000C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		1.13		1.31		1.50	ns
t_{F20+}		2.30		2.71		3.19	ns

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		–0.52		–0.53		–0.56	ns
GTL+		–0.18		–0.29		–0.39	ns
SSTL-3 Class I		–0.67		–0.71		–0.75	ns
SSTL-3 Class II		–0.67		–0.71		–0.75	ns
SSTL-2 Class I		–0.67		–0.71		–0.75	ns
SSTL-2 Class II		–0.67		–0.71		–0.75	ns
LVDS		–0.69		–0.70		–0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

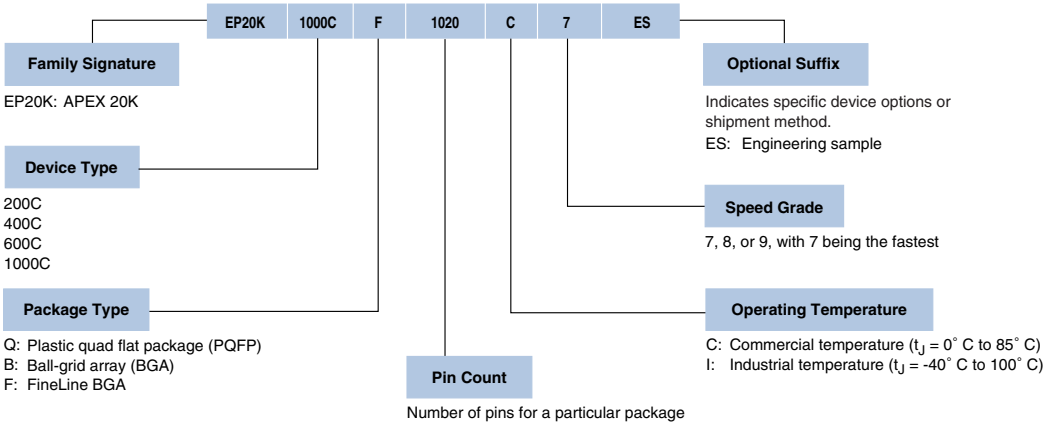
The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

Figure 39. APEX 20KC Device Packaging Ordering Information



Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2 supersedes information published in previous versions.

Version 2.2

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2:

- Updated Tables 1.
- Updated notes in Tables 20.

Version 2.1

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.1:

- Removed figure on AC Test Conditions.
- Updated conditions in Tables 40 and 41.
- Added Tables 42 and 43.
- Updated V_{OD} in Table 27.
- Added Figures 36 through 38.
- Updated Tables 44 through 49.
- Updated Tables 62 through 67.
- Removed notes in Tables 44 through 67.
- Various textual changes throughout the document.