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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	376
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k200cf484c7">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k200cf484c7</a>

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

<b>Table 7. APEX 20KC Device Features (Part 1 of 2)</b>	
<b>Feature</b>	<b>APEX 20KC Devices</b>
MultiCore system integration	Full support
Hot-socketing support	Full support
SignalTap logic analysis	Full support
32-/64-bit, 33-MHz PCI	Full compliance
32-/64-bit, 66-MHz PCI	Full compliance in -7 and -8 speed grades in selected devices
MultiVolt I/O	1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$ $V_{CCIO}$ selected bank by bank 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift circuitry LVDS support Up to four PLLs ClockShift clock phase adjustment
Dedicated clock and input pins	Eight

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

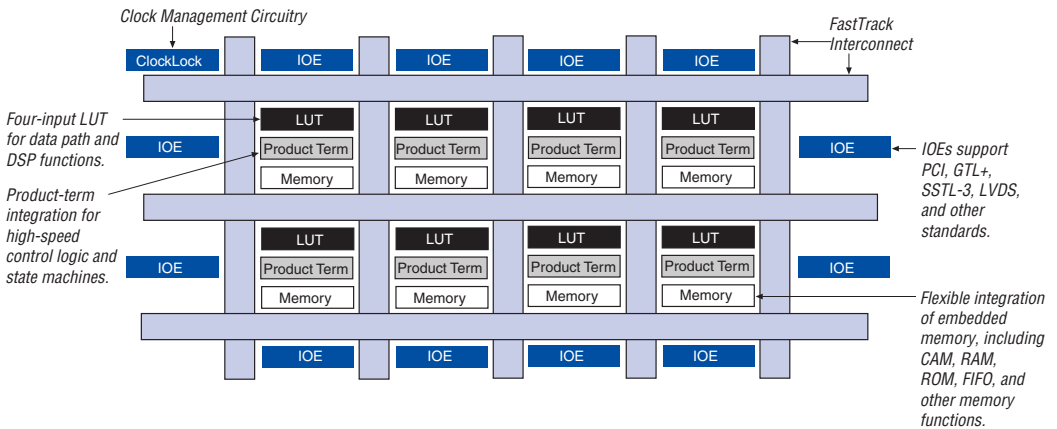
## Functional Description

APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB’s high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

**Figure 1. APEX 20KC Device Block Diagram**

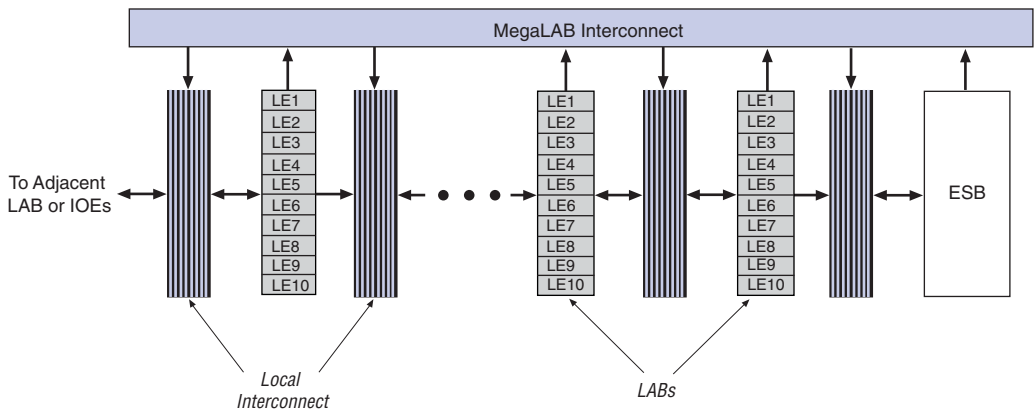


APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

## MegaLAB Structure

APEX 20KC devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000C devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20KC LAB.

APEX 20KC devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas, minimizing the use of the MegaLAB and FastTrack interconnect and providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 6. APEX 20KC Carry Chain

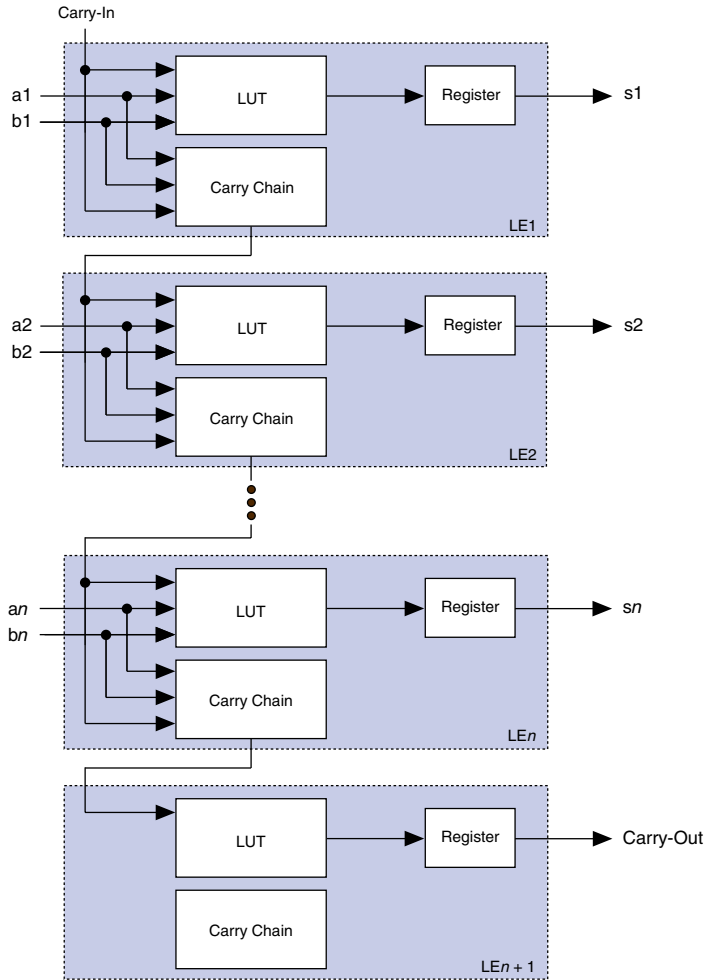
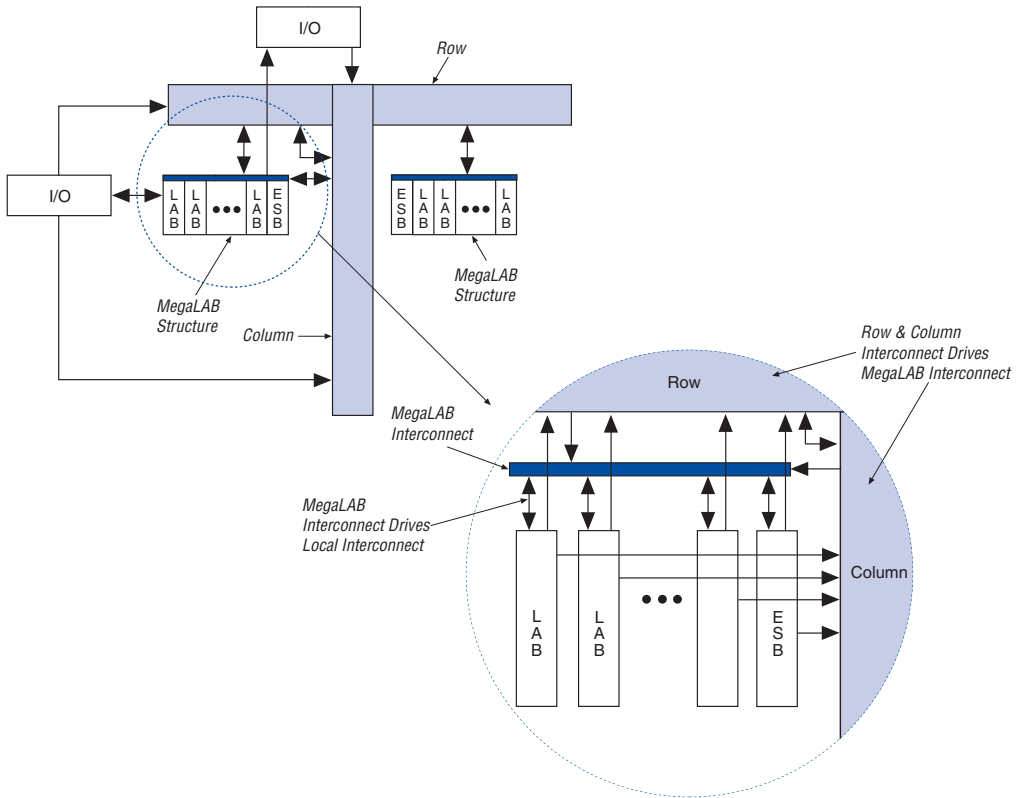
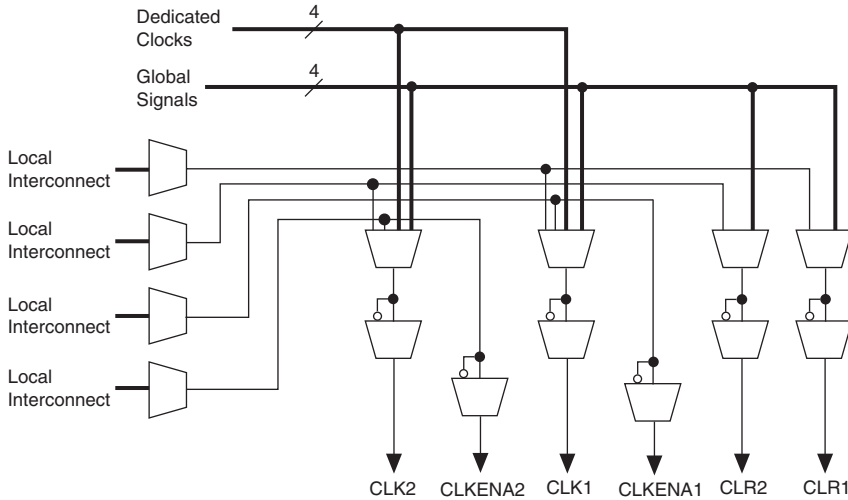


Figure 10. FastTrack Connection to Local Interconnect



The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



### Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.



APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

<b>Table 9. APEX 20KC Programmable Delay Chains</b>	
<b>Programmable Delay</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin
Clock enable delay	Increase clock enable delay

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

Figure 25. APEX 20KC Bidirectional I/O Registers Notes (1), (2)

Row, Column, FastRow, 4 Dedicated  
or Local Interconnect Clock Inputs

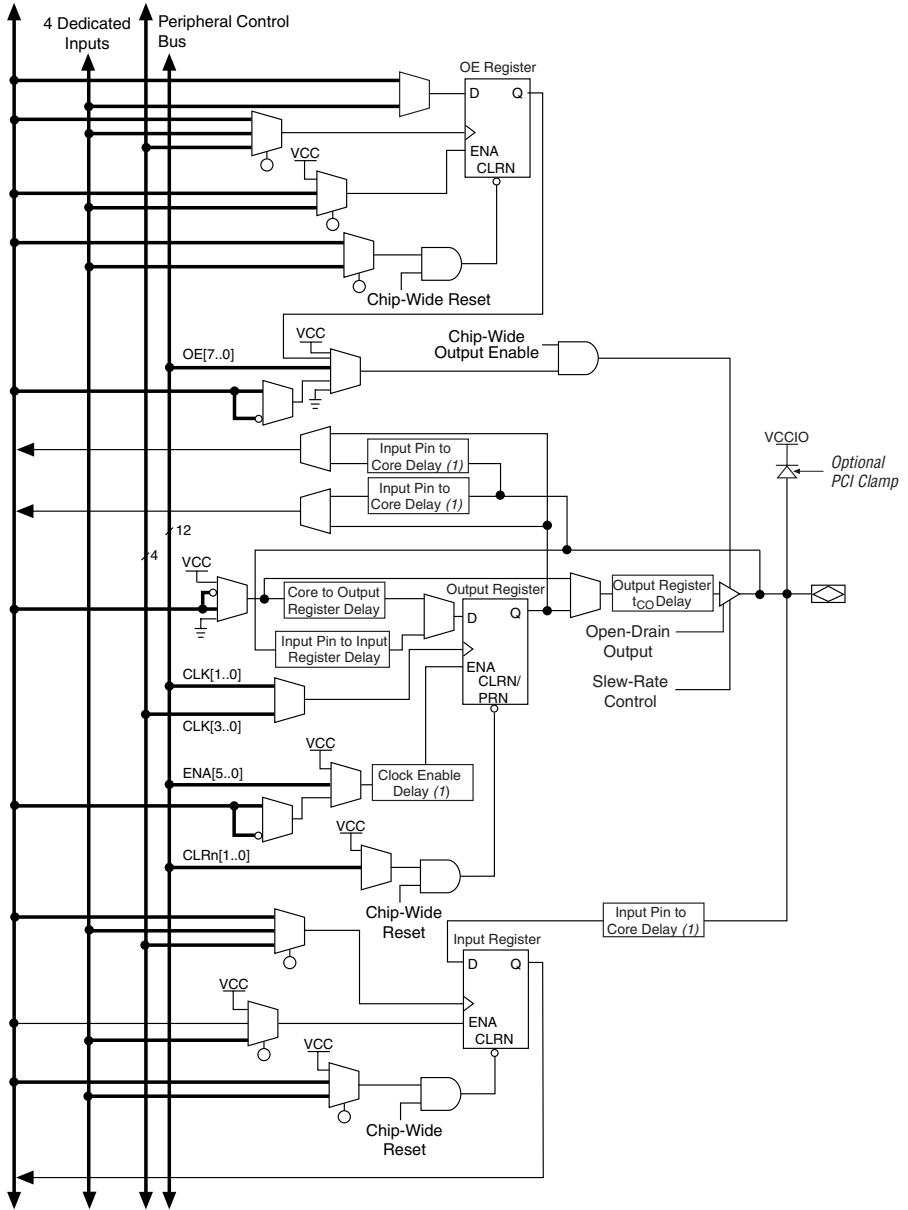
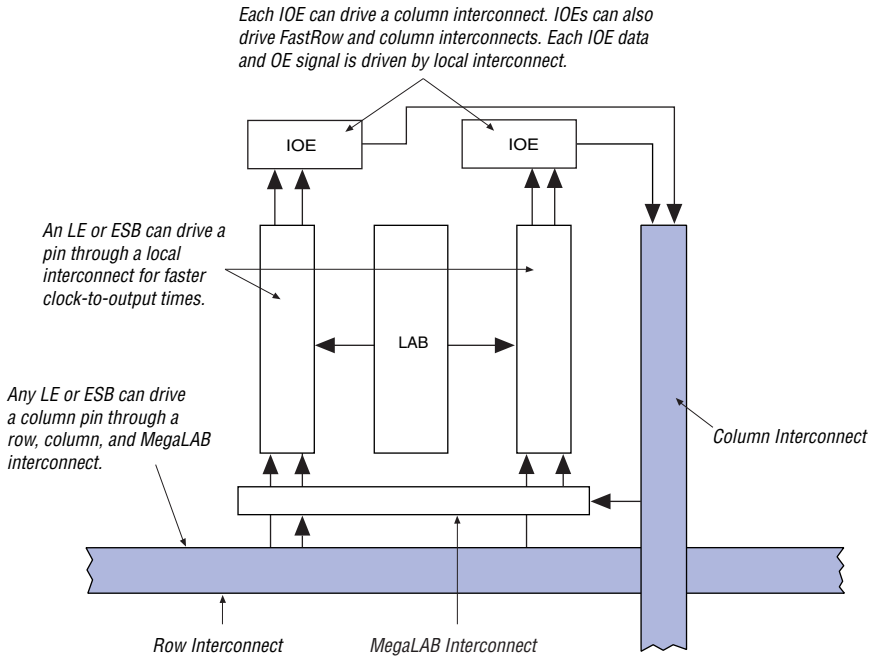


Figure 27 shows how a column IOE connects to the interconnect.

**Figure 27. Column IOE Connection to the Interconnect**



### Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

**Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz
$f_{IN}$	Input clock frequency	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

**Notes to Tables 11 and 12:**

- (1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
- (2) The maximum lock time is 40  $\mu$ s or 2,000 input clock cycles, whichever occurs first.
- (3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the CLKLK\_ENA pin goes high in user mode.
- (4) The PLL VCO operating range is  $200 \text{ MHz} \leq f_{VCO} \leq 840 \text{ MHz}$  for LVDS mode.
- (5) Contact Altera Applications for information on these parameters.

## SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

**Figure 30. APEX 20KC JTAG Waveforms**

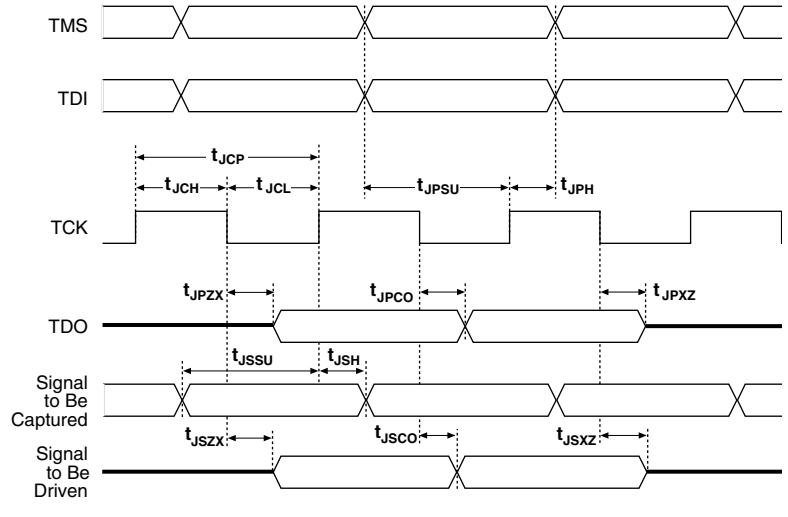


Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

**Table 16. APEX 20KC JTAG Timing Parameters & Values**

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- [Application Note 39 \(IEEE Std. 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#)

**Table 28. GTL+ I/O Specifications**

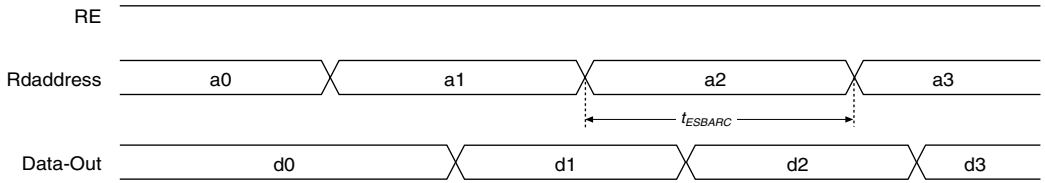
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{TT}$	Termination voltage		1.35	1.5	1.65	V
$V_{REF}$	Reference voltage		0.88	1.0	1.12	V
$V_{IH}$	High-level input voltage		$V_{REF} + 0.1$			V
$V_{IL}$	Low-level input voltage				$V_{REF} - 0.1$	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 36 \text{ mA}$ (2)			0.65	V

**Table 29. SSTL-2 Class I Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{CCIO}$	I/O supply voltage		2.375	2.5	2.625	V
$V_{TT}$	Termination voltage		$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
$V_{REF}$	Reference voltage		1.15	1.25	1.35	V
$V_{IH}$	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
$V_{IL}$	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -7.6 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 7.6 \text{ mA}$ (2)			$V_{TT} - 0.57$	V

Figure 33. ESB Asynchronous Timing Waveforms

**ESB Asynchronous Read**



**ESB Asynchronous Write**

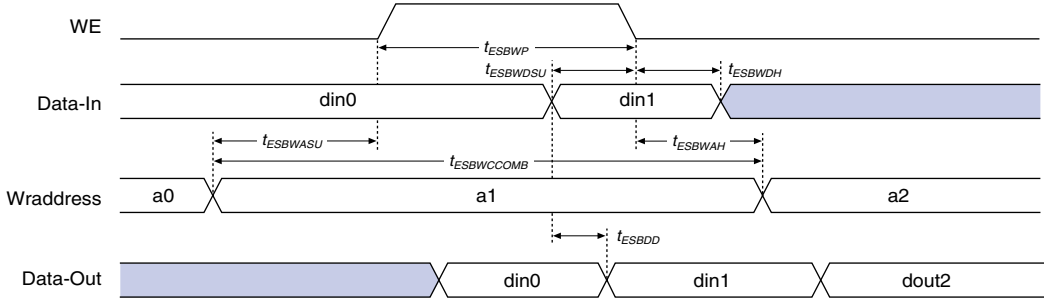


Figure 34. ESB Synchronous Timing Waveforms

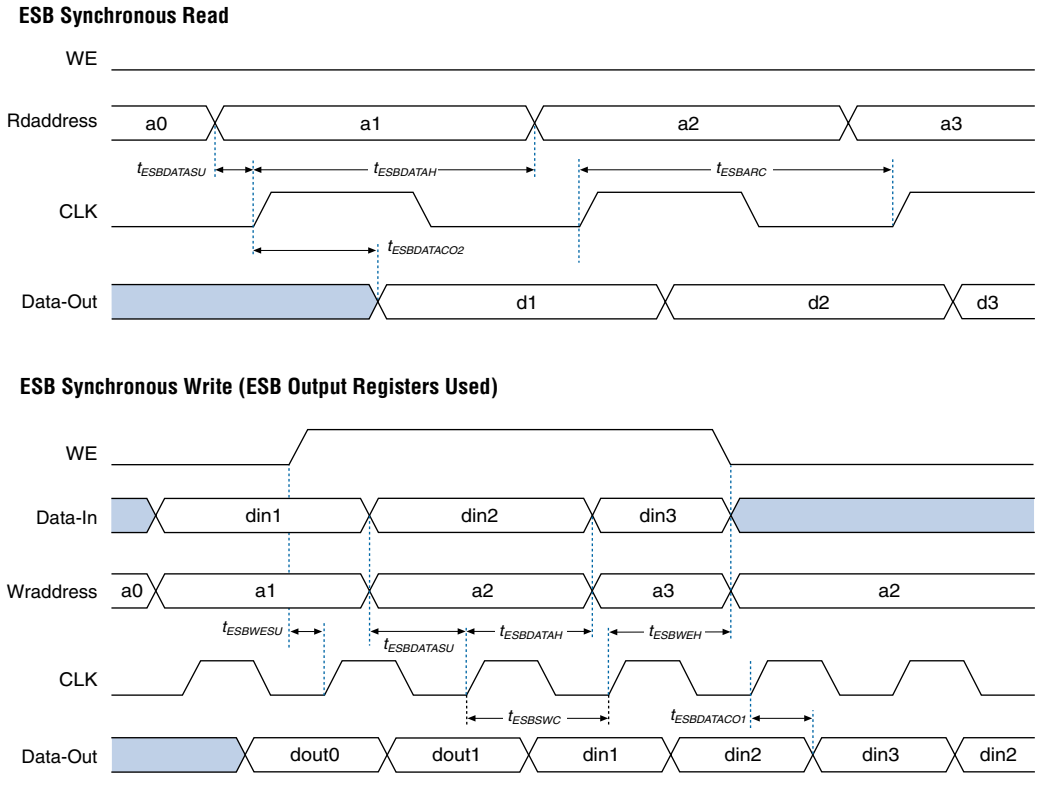


Figure 35 shows the timing model for bidirectional I/O pin timing.



**Table 51. EP20K400C  $t_{MAX}$  ESB Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.30		1.51		1.69	ns
$t_{ESBSRC}$		2.35		2.49		2.72	ns
$t_{ESBAWC}$		2.92		3.46		3.86	ns
$t_{ESBSWC}$		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
$t_{ESBWAH}$	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
$t_{ESBWDH}$	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
$t_{ESBRAH}$	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	-0.20		-0.24		-0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		-0.02		ns
$t_{ESBDATAO1}$		1.09		1.28		1.43	ns
$t_{ESBDATAO2}$		2.10		2.52		2.82	ns
$t_{ESBDD}$		2.50		2.97		3.32	ns
$t_{PD}$		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

**Table 52. EP20K400C  $t_{MAX}$  Routing Delays**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.15		0.17		0.19	ns
$t_{F5-20}$		0.94		1.06		1.25	ns
$t_{F20+}$		1.73		1.96		2.30	ns

**Table 53. EP20K400C Minimum Pulse Width Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.33		1.66		2.00		ns
$t_{CL}$	1.33		1.66		2.00		ns
$t_{CLRP}$	0.20		0.20		0.20		ns
$t_{PREP}$	0.20		0.20		0.20		ns
$t_{ESBCH}$	1.33		1.66		2.00		ns
$t_{ESBCL}$	1.33		1.66		2.00		ns
$t_{ESBWP}$	1.05		1.28		1.44		ns
$t_{ESBRP}$	0.87		1.06		1.19		ns

**Table 54. EP20K400C External Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	1.37		1.52		1.64		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.25	2.00	4.61	2.00	5.03	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.27	0.50	2.55	-	-	ns

**Table 59. EP20K600C Minimum Pulse Width Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.33		1.66		2.00		ns
$t_{CL}$	1.33		1.66		2.00		ns
$t_{CLRP}$	0.20		0.20		0.20		ns
$t_{PREP}$	0.20		0.20		0.20		ns
$t_{ESBCH}$	1.33		1.66		2.00		ns
$t_{ESBCL}$	1.33		1.66		2.00		ns
$t_{ESBWP}$	1.05		1.28		1.44		ns
$t_{ESBRP}$	0.87		1.06		1.19		ns

**Table 60. EP20K600C External Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	1.28		1.40		1.45		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.37	0.50	2.63	-	-	ns

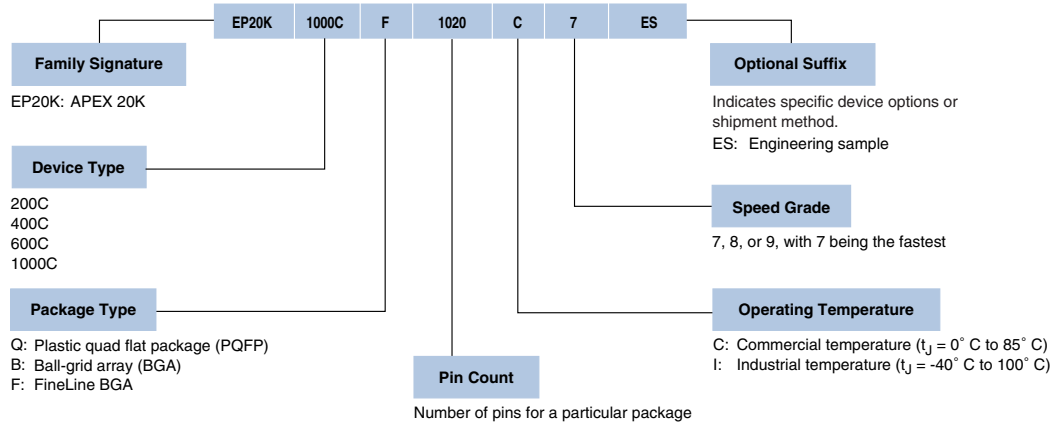
**Table 61. EP20K600C External Bidirectional Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.03		2.57		2.97		ns
$t_{\text{INHIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{\text{XZBIDIR}}$		8.31		9.14		9.76	ns
$t_{\text{ZXBIDIR}}$		8.31		9.14		9.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.99		4.77		-		ns
$t_{\text{INHIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.37	0.50	2.63	-	-	ns
$t_{\text{XZBIDIRPLL}}$		6.35		6.94		-	ns
$t_{\text{ZXBIDIRPLL}}$		6.35		6.94		-	ns

**Table 62. EP20K1000C  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.01		0.01		0.01		ns
$t_{\text{H}}$	0.10		0.10		0.10		ns
$t_{\text{CO}}$		0.27		0.30		0.32	ns
$t_{\text{LUT}}$		0.66		0.79		0.92	ns

Figure 39. APEX 20KC Device Packaging Ordering Information



## Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2 supersedes information published in previous versions.

### Version 2.2

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2:

- Updated [Tables 1](#).
- Updated notes in [Tables 20](#).

### Version 2.1

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.1:

- Removed figure on AC Test Conditions.
- Updated conditions in [Tables 40](#) and [41](#).
- Added [Tables 42](#) and [43](#).
- Updated  $V_{OD}$  in [Table 27](#).
- Added [Figures 36](#) through [38](#).
- Updated [Tables 44](#) through [49](#).
- Updated [Tables 62](#) through [67](#).
- Removed notes in [Tables 44](#) through [67](#).
- Various textual changes throughout the document.