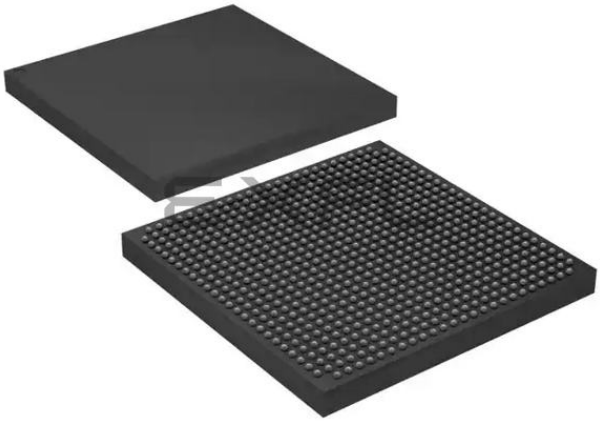

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	-
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200cf672c7

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP & BGA Package Options & I/O Count *Notes (1), (2)*

Device	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K200C	136	168	271	
EP20K400C				488
EP20K600C				488
EP20K1000C				488

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

Table 7. APEX 20KC Device Features (Part 1 of 2)

Feature	APEX 20KC Devices
MultiCore system integration	Full support
Hot-socketing support	Full support
SignalTap logic analysis	Full support
32-/64-bit, 33-MHz PCI	Full compliance
32-/64-bit, 66-MHz PCI	Full compliance in -7 and -8 speed grades in selected devices
MultiVolt I/O	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected bank by bank 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift circuitry LVDS support Up to four PLLs ClockShift clock phase adjustment
Dedicated clock and input pins	Eight

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

Functional Description

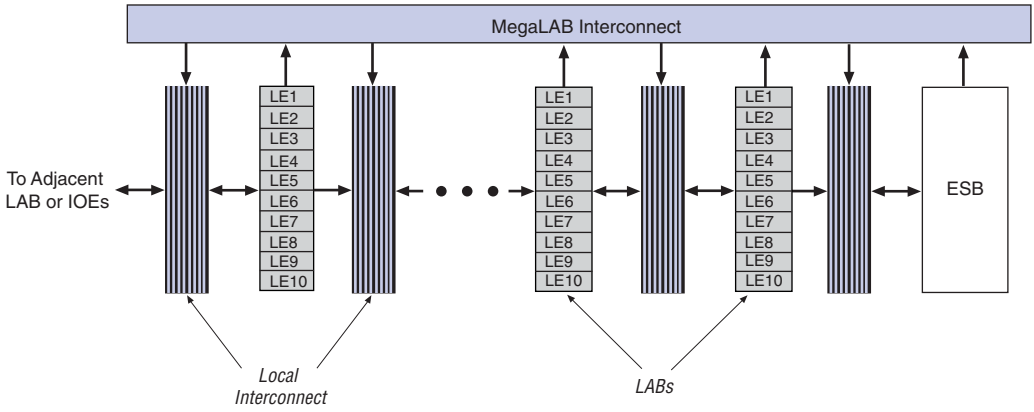
APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

MegaLAB Structure

APEX 20KC devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000C devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20KC LAB.

APEX 20KC devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas, minimizing the use of the MegaLAB and FastTrack interconnect and providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset or to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20KC devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20KC architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 12. APEX 20KC FastRow Interconnect

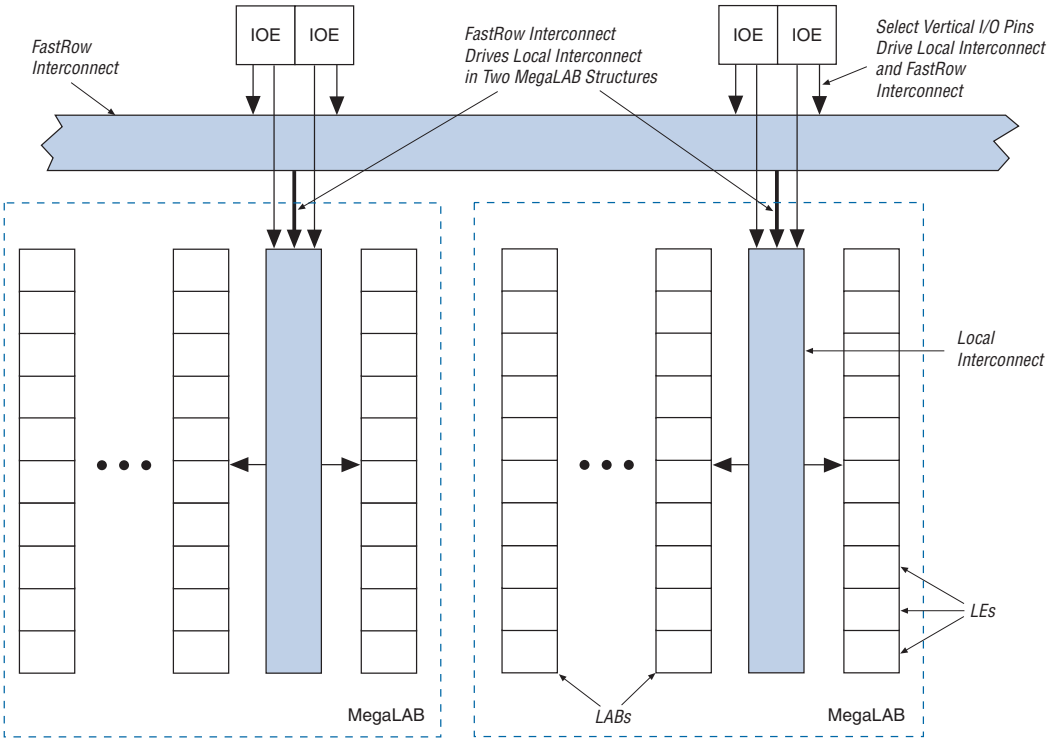


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20KC ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20KC device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20KC IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor and the PCI clamp diode enabled.

For more information on 5.0-V tolerance, refer to the "5.0-V Tolerance in APEX 20KE Devices White Paper," as the information found therein also applies to APEX 20KC devices.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ *(1)*	✓ *(1)*		✓			
2.5		✓	✓ *(1)*			✓		
3.3		✓	✓	✓ *(2)*		✓ *(3)*	✓	✓

Notes to Table 10:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor and the PCI clamp diode enabled.

(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

Table 13. APEX 20KC JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Table 22. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0 V I_{OH} = –0.1 mA *(1)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0 V I_{OL} = 0.1 mA *(2)*		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA *(1)*	2.1		V
		I_{OH} = –1 mA *(1)*	2.0		V
		I_{OH} = –2 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA *(2)*		0.2	V
		I_{OL} = 1 mA *(2)*		0.4	V
		I_{OL} = 2 mA *(2)*		0.7	V

Table 30. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(2)*			V_{TT} – 0.76	V

Table 31. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{TT} – 0.6	V

Table 32. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(2)*			V_{TT} – 0.8	V

Table 33. HSTL Class I I/O Specifications

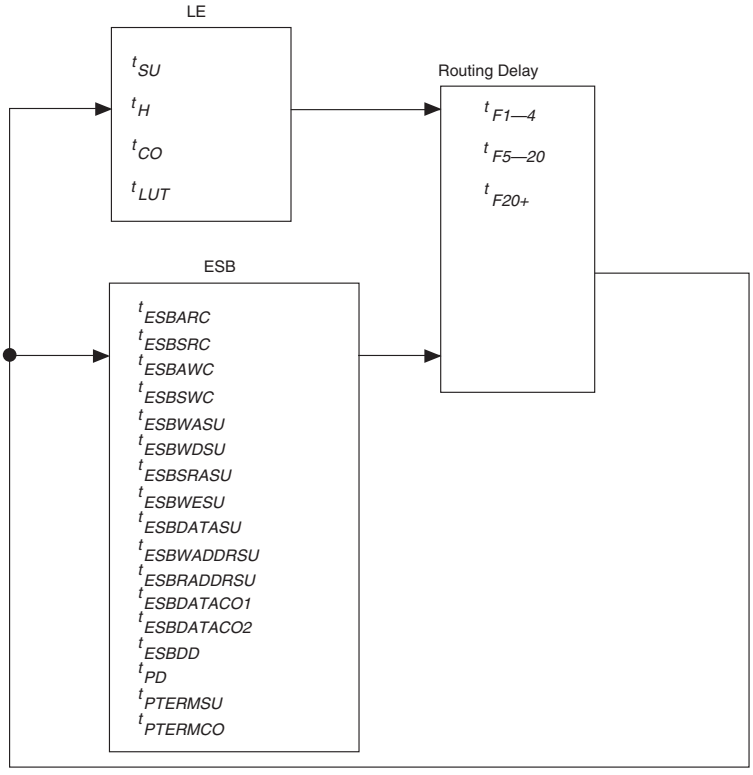
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			0.4	V

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 32 shows the f_{MAX} timing model for APEX 20KC devices.

Figure 32. f_{MAX} Timing Model



Figures 33 and 34 show the asynchronous and synchronous timingwaveforms, respectively, for the ESB macroparameters in Table 37.

Figure 36. AC Test Conditions for LVTTL, 2.5 V, 1.8 V, PCI & GTL+ I/O Standards

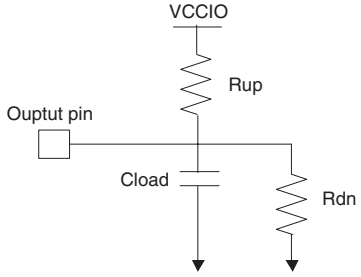


Figure 37. AC Test Conditions for SSTL-3 Class I & II I/O Standards

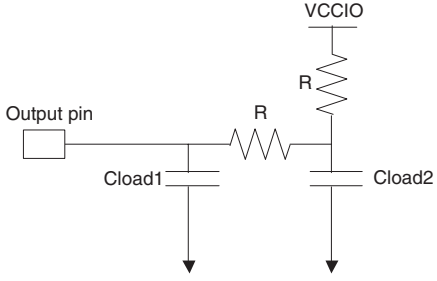


Figure 38. AC Test Conditions for the LVDS I/O Standard

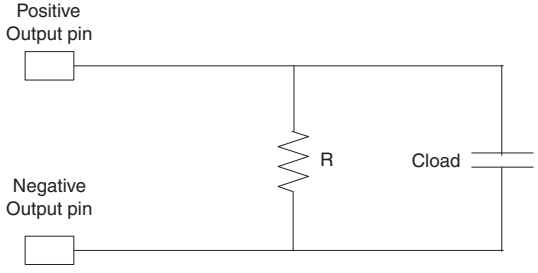


Table 49. EP20K200C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.38		1.78		1.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	3.79	2.00	4.31	2.00	4.70	ns
$t_{XZBIDIR}$		6.12		6.51		7.89	ns
$t_{ZXBIDIR}$		6.12		6.51		7.89	ns
$t_{INSUBIDIRPLL}$	2.82		3.47		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.36	0.50	2.62	-	-	ns
$t_{XZBIDIRPLL}$		4.69		4.82		-	ns
$t_{ZXBIDIRPLL}$		4.69		4.82		-	ns

Table 50. EP20K400C f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.01		0.01		ns
t_{H}	0.10		0.10		0.10		ns
t_{CO}		0.27		0.30		0.32	ns
t_{LUT}		0.65		0.78		0.92	ns

Table 53. EP20K400C Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.33		1.66		2.00		ns
t_{CL}	1.33		1.66		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.33		1.66		2.00		ns
t_{ESBCL}	1.33		1.66		2.00		ns
t_{ESBWP}	1.05		1.28		1.44		ns
t_{ESBRP}	0.87		1.06		1.19		ns

Table 54. EP20K400C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.37		1.52		1.64		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.25	2.00	4.61	2.00	5.03	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.27	0.50	2.55	-	-	ns

Table 63. EP20K1000C f_{MAX} ESB Timing Microparameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.48		1.57		1.65	ns
t_{ESBSRC}		2.36		2.50		2.73	ns
t_{ESBAWC}		2.93		3.46		3.86	ns
t_{ESBSWC}		3.08		3.43		3.83	ns
$t_{ESBWASU}$	0.51		0.50		0.52		ns
t_{ESBWAH}	0.38		0.51		0.57		ns
$t_{ESBWDSU}$	0.62		0.62		0.66		ns
t_{ESBWDH}	0.38		0.51		0.57		ns
$t_{ESBRASU}$	1.40		1.47		1.53		ns
t_{ESBRAH}	0.00		0.07		0.18		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	1.92		2.19		2.35		ns
$t_{ESBWADDRSU}$	–0.20		–0.28		–0.32		ns
$t_{ESBRADDRSU}$	0.00		–0.03		–0.05		ns
$t_{ESBDATACO1}$		1.12		1.30		1.46	ns
$t_{ESBDATACO2}$		2.11		2.53		2.84	ns
t_{ESBDD}		2.56		2.96		3.30	ns
t_{PD}		1.49		1.79		2.02	ns
$t_{PTERMSU}$	0.61		0.69		0.77		ns
$t_{PTERMCO}$		1.13		1.32		1.48	ns

Table 64. EP20K1000C f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.15		0.17		0.19	ns
t_{F5-20}		1.13		1.31		1.50	ns
t_{F20+}		2.30		2.71		3.19	ns

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