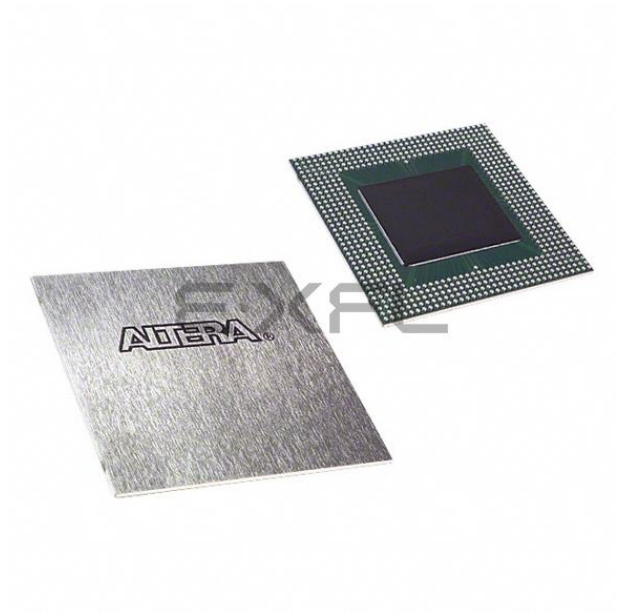

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

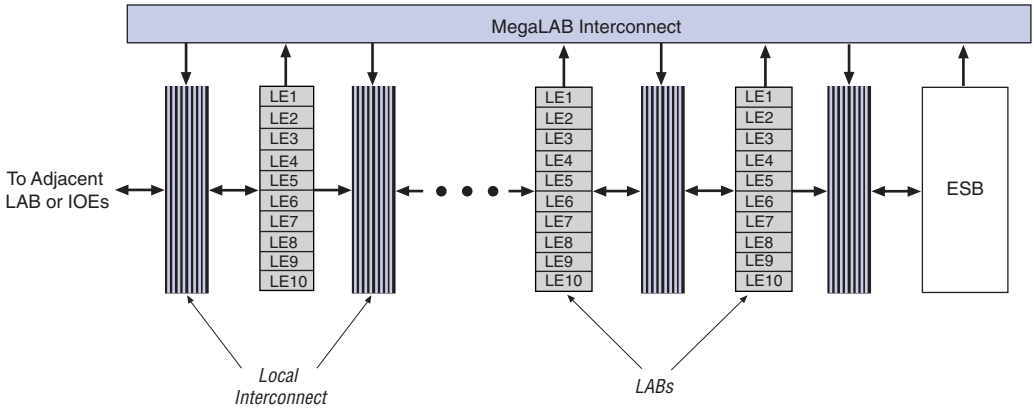
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	212992
Number of I/O	488
Number of Gates	1052000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k400cb652c8

MegaLAB Structure

APEX 20KC devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000C devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure

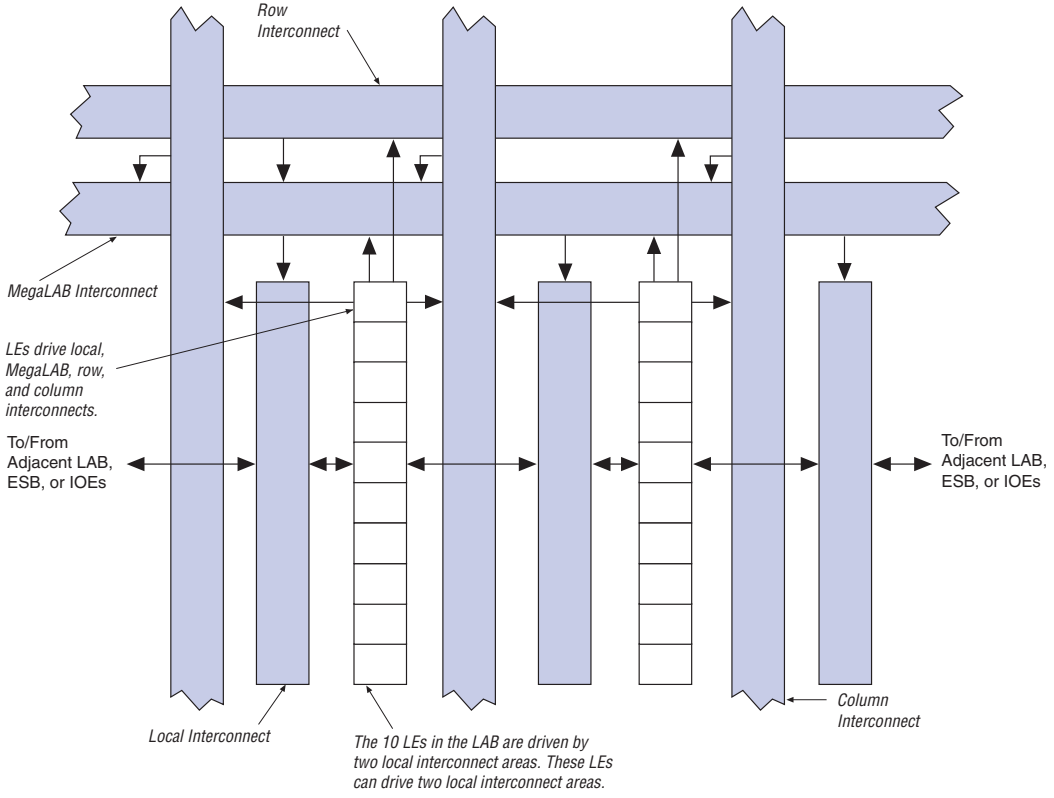


Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20KC LAB.

APEX 20KC devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas, minimizing the use of the MegaLAB and FastTrack interconnect and providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure

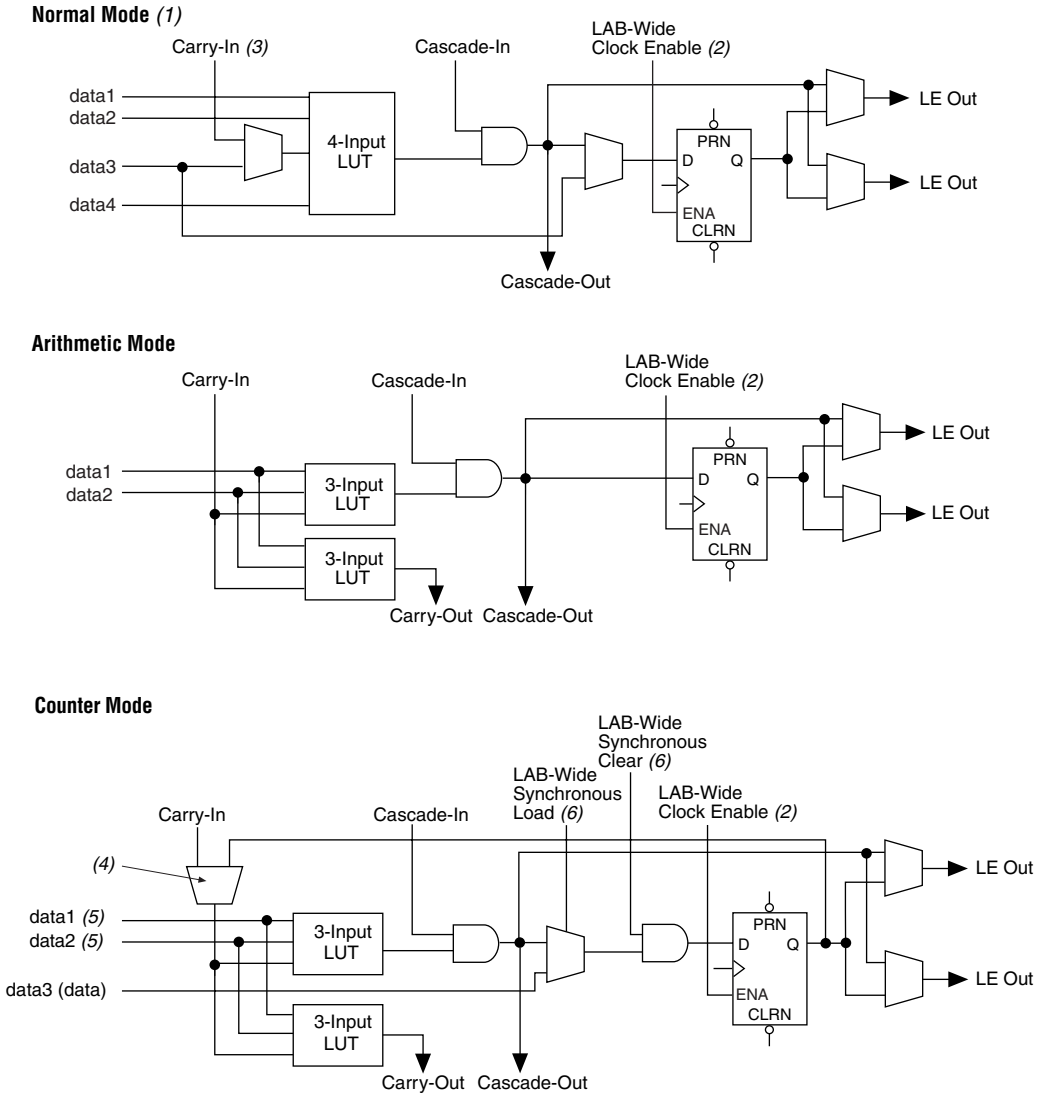


Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

Figure 8. APEX 20KC LE Operating Modes

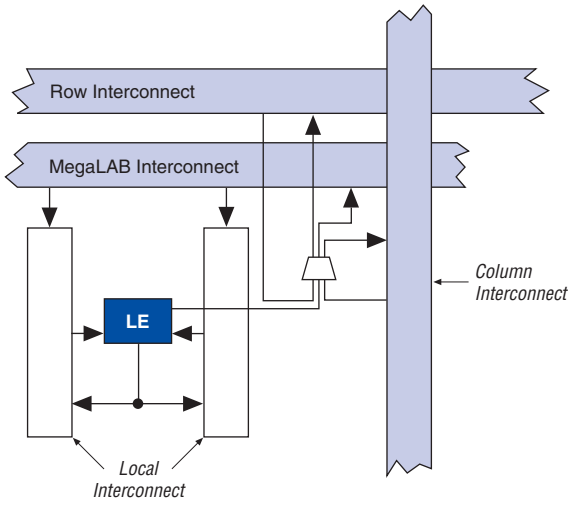


Notes to Figure 8:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

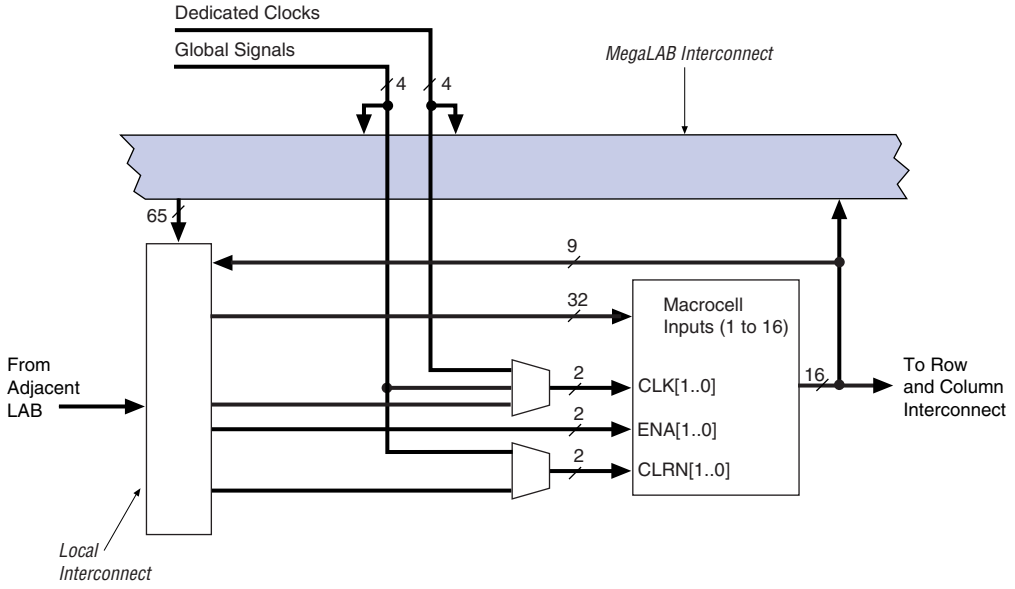
Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX 20KC devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. The FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K400C and larger devices, the FastRow interconnect drives the two MegaLAB structures in the top left corner, the two MegaLAB structures in the two right corner, the two MegaLAB structures in the bottom left corner, and the two MegaLAB structures in the bottom right corner. On EP20K200C and smaller devices, FastRow interconnect drives the two MegaLAB structures on the top and the two MegaLAB structures on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLAB structures except the end local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Figure 13. Product-Term Logic in ESB

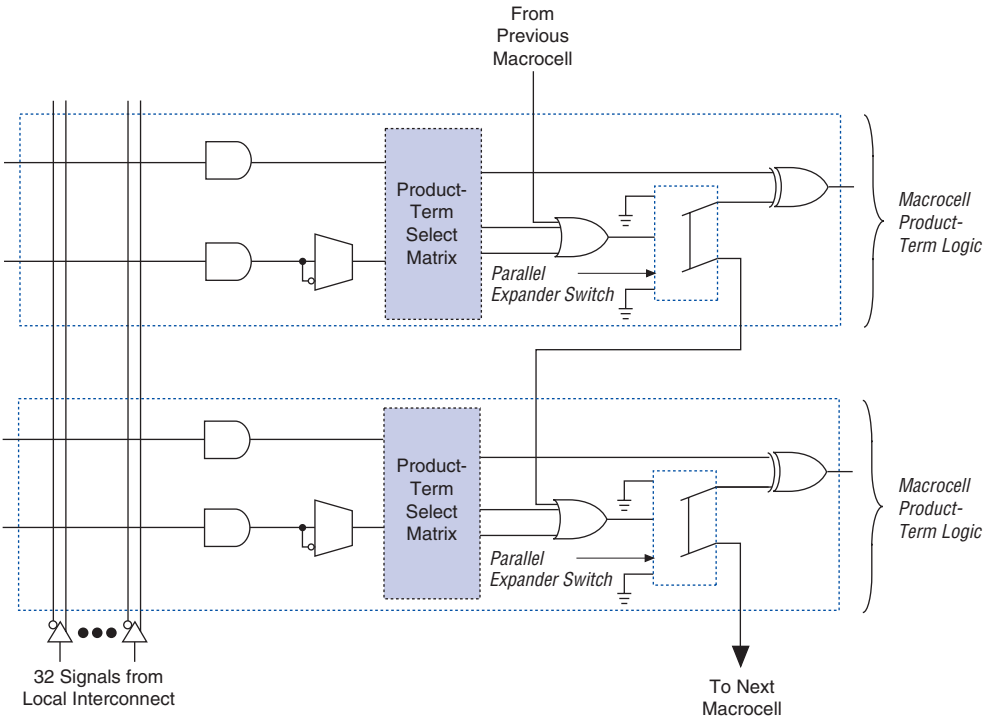


Macrocells

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20KC macrocell.

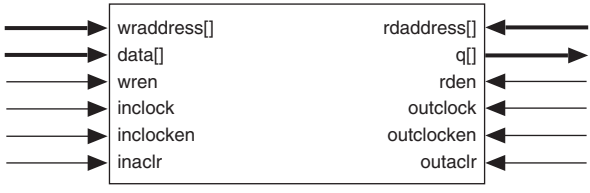
Figure 16. APEX 20KC Parallel Expanders



Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

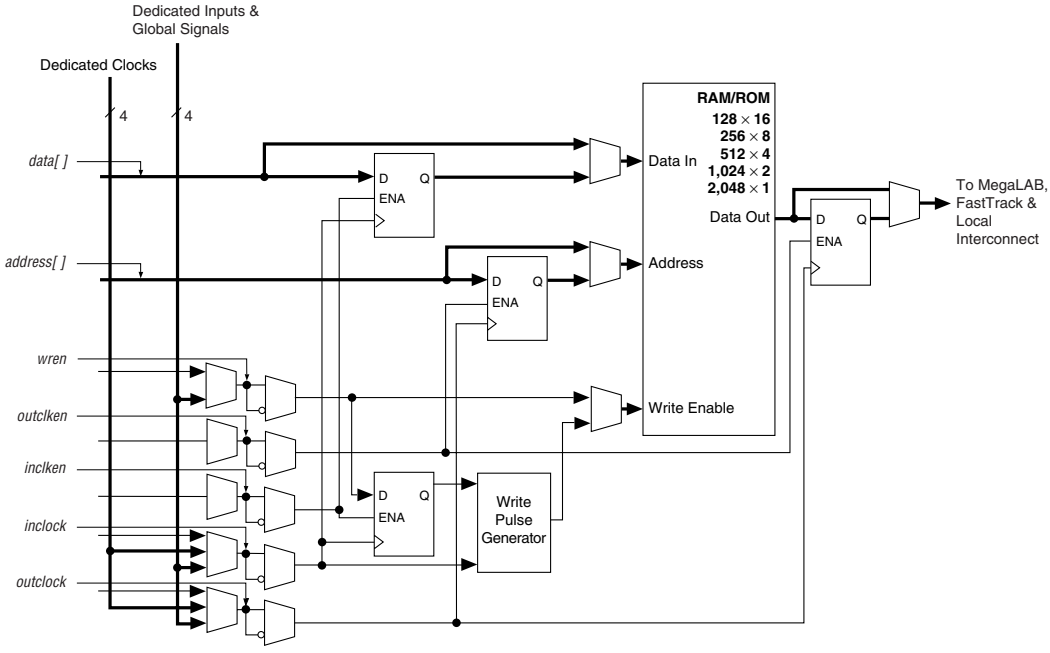
Figure 17. ESB Block Diagram



Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



Note to Figure 22:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

Table 11. APEX 20KC ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	%
$t_{OUTJITTER}$	RMS jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	%
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} *(2), (3)*	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} *(4)*	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz
f_{IN}	Input clock frequency	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Notes to Tables 11 and 12:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ f_{VCO} ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

Table 14. APEX 20KC Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K200C	1,164
EP20K400C	1,506
EP20K600C	1,806
EP20K1000C	2,190

Table 15. 32-Bit APEX 20KC Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K200C	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K400C	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600C	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000C	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 15:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 17 through 20:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and time periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KC device recommended operating conditions, shown in Table 18 on page 55.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(10) Capacitance is sample-tested only.

Tables 21 through 35 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –12 mA, V_{CCIO} = 3.0 V *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{CCIO} = 3.0 V *(2)*		0.4	V

Table 22. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0 V I_{OH} = –0.1 mA *(1)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0 V I_{OL} = 0.1 mA *(2)*		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA *(1)*	2.1		V
		I_{OH} = –1 mA *(1)*	2.0		V
		I_{OH} = –2 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA *(2)*		0.2	V
		I_{OL} = 1 mA *(2)*		0.4	V
		I_{OL} = 2 mA *(2)*		0.7	V

Table 30. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(2)*			V_{TT} – 0.76	V

Table 31. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{TT} – 0.6	V

Figure 33. ESB Asynchronous Timing Waveforms

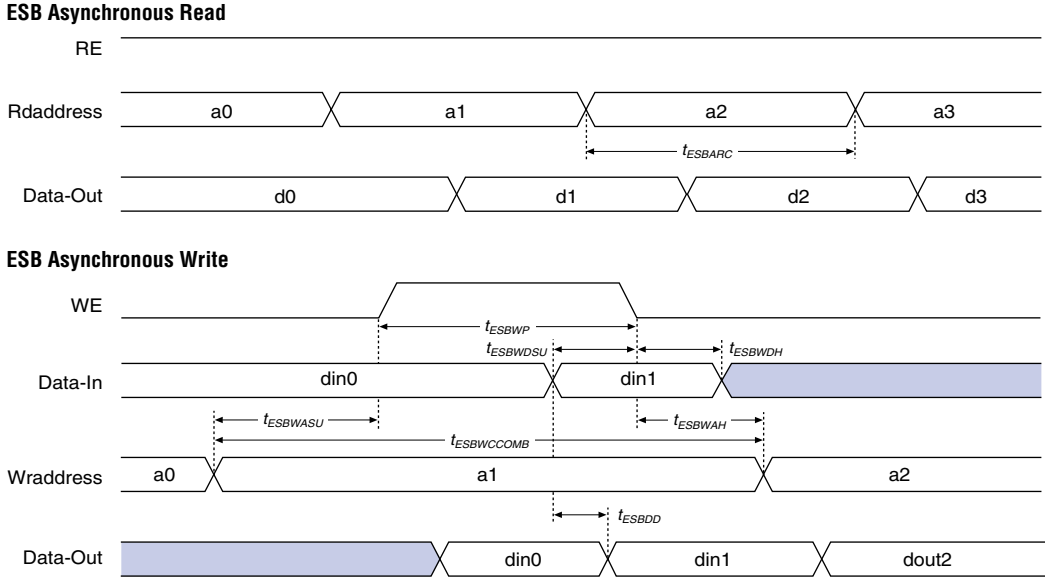


Table 37. APEX 20KC f_{MAX} ESB Timing Parameters	
Symbol	**Parameter**
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Table 38. APEX 20KC f_{MAX} Routing Delays	
Symbol	**Parameter**
t_{F1-4}	Fan-out delay estimate using local interconnect
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect
t_{F20+}	Fan-out delay estimate using FastTrack interconnect

Table 42. APEX 20KC Selectable I/O Standard Input Adder Delays (Part 2 of 2) *Note (1)*		
Symbol	**Parameter**	**Condition**
LVDS	Input adder delay for the LVDS I/O standard	
CTT	Input adder delay for the CTT I/O standard	
AGP	Input adder delay for the AGP I/O standard	

Table 43. APEX 20KC Selectable I/O Standard Output Adder Delays *Note (1)*		
Symbol	**Parameter**	**Condition**
LVCMOS	Output adder delay for the LVCMOS I/O standard	
LVTTL	Output adder delay for the LVTTL I/O standard	Cload = 35 pF Rup = 564.5 Ω Rdn = 430 Ω *(2)*
2.5 V	Output adder delay for the 2.5-V I/O standard	Cload = 35 pF Rup = 450 Ω Rdn = 450 Ω *(2)*
1.8 V	Output adder delay for the 1.8-V I/O standard	Cload = 35 pF Rup = 520 Ω Rdn = 480 Ω *(2)*
PCI	Output adder delay for the PCI I/O standard	Cload = 10 pF Rup = 1M Ω Rdn = 25 Ω *(2)*
GTl+	Output adder delay for the GTL+ I/O standard	Cload = 30 pF Rup = 25 Ω *(2)*
SSTL-3 Class I	Output adder delay for the SSTL-3 Class I I/O standard	Cload1 = 0 pF Cload2 = 30 pF R = 25 Ω *(2)*
SSTL-3 Class II	Output adder delay for the SSTL-3 Class II I/O standard	Cload1 = 0 pF Cload2 = 30 pF R = 25 Ω *(2)*
SSTL-2 Class I	Output adder delay for the SSTL-2 Class I I/O standard	
SSTL-2 Class II	Output adder delay for the SSTL-2 Class II I/O standard	
LVDS	Output adder delay for the LVDS I/O standard	Cload = 4 pF R=100 Ω *(2)*
CTT	Output adder delay for the CTT I/O standard	
AGP	Output adder delay for the AGP I/O standard	

Note to Tables 42 and 43:

(1) These delays report the differences in delays for different I/O standards. Add the delay for the I/O standard that is used to the external timing parameters.

(2) See Figure 36 for more information.

Figure 36. AC Test Conditions for LVTTL, 2.5 V, 1.8 V, PCI & GTL+ I/O Standards

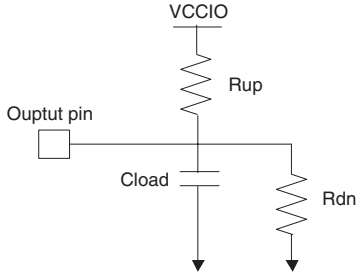


Figure 37. AC Test Conditions for SSTL-3 Class I & II I/O Standards

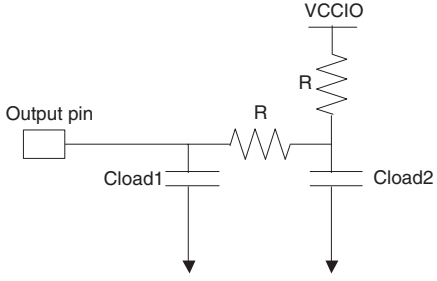


Figure 38. AC Test Conditions for the LVDS I/O Standard

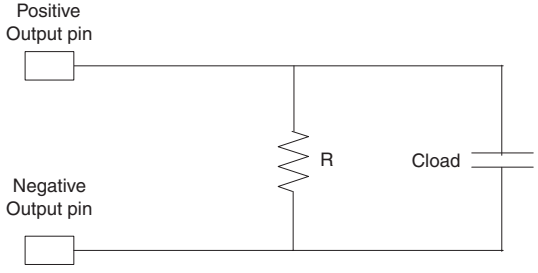
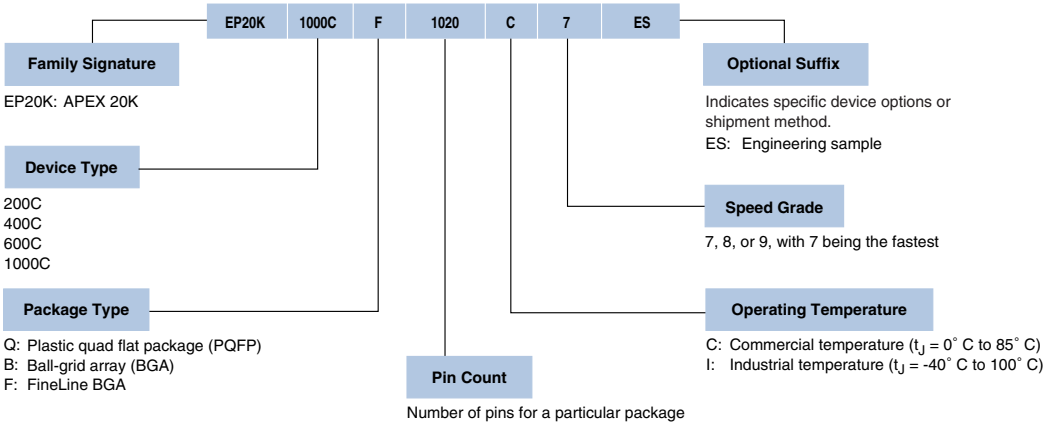


Figure 39. APEX 20KC Device Packaging Ordering Information



Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2 supersedes information published in previous versions.

Version 2.2

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2:

- Updated Tables 1.
- Updated notes in Tables 20.

Version 2.1

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.1:

- Removed figure on AC Test Conditions.
- Updated conditions in Tables 40 and 41.
- Added Tables 42 and 43.
- Updated V_{OD} in Table 27.
- Added Figures 36 through 38.
- Updated Tables 44 through 49.
- Updated Tables 62 through 67.
- Removed notes in Tables 44 through 67.
- Various textual changes throughout the document.