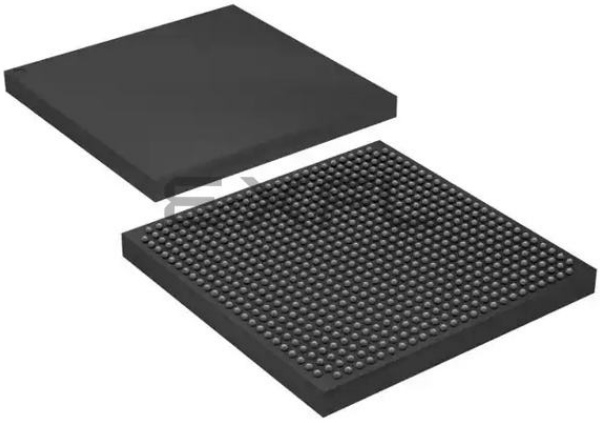
# Intel - EP20K400CF672C8AA Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1664 |
| Number of Logic Elements/Cells | 16640 |
| Total RAM Bits | 212992 |
| Number of I/O | 488 |
| Number of Gates | 1052000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k400cf672c8aa |

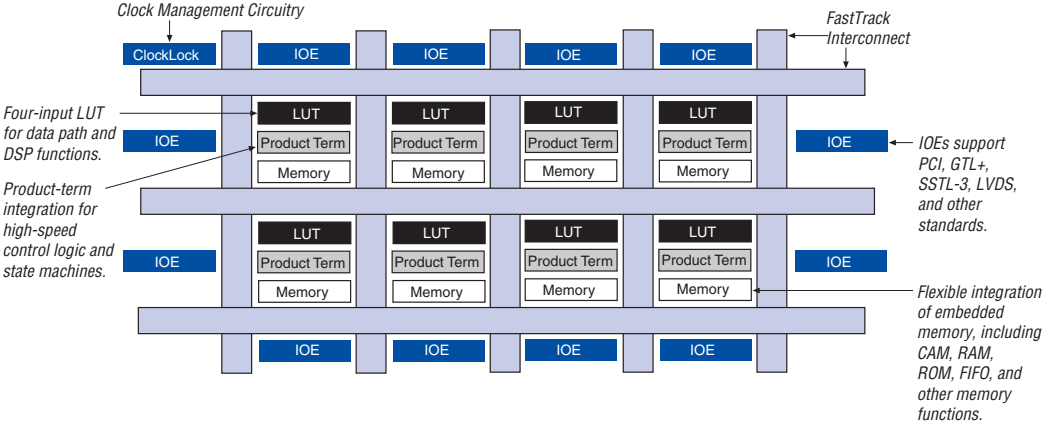
APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

*Table 7. APEX 20KC Device Features (Part 1 of 2)*

| Feature | APEX 20KC Devices |
|---|---|
| MultiCore system integration | Full support |
| Hot-socketing support | Full support |
| SignalTap logic analysis | Full support |
| 32-/64-bit, 33-MHz PCI | Full compliance |
| 32-/64-bit, 66-MHz PCI | Full compliance in -7 and -8 speed grades in selected devices |
| MultiVolt I/O | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected bank by bank<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>$m/(n \times v)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift circuitry<br>LVDS support<br>Up to four PLLs<br>ClockShift clock phase adjustment |
| Dedicated clock and input pins | Eight |

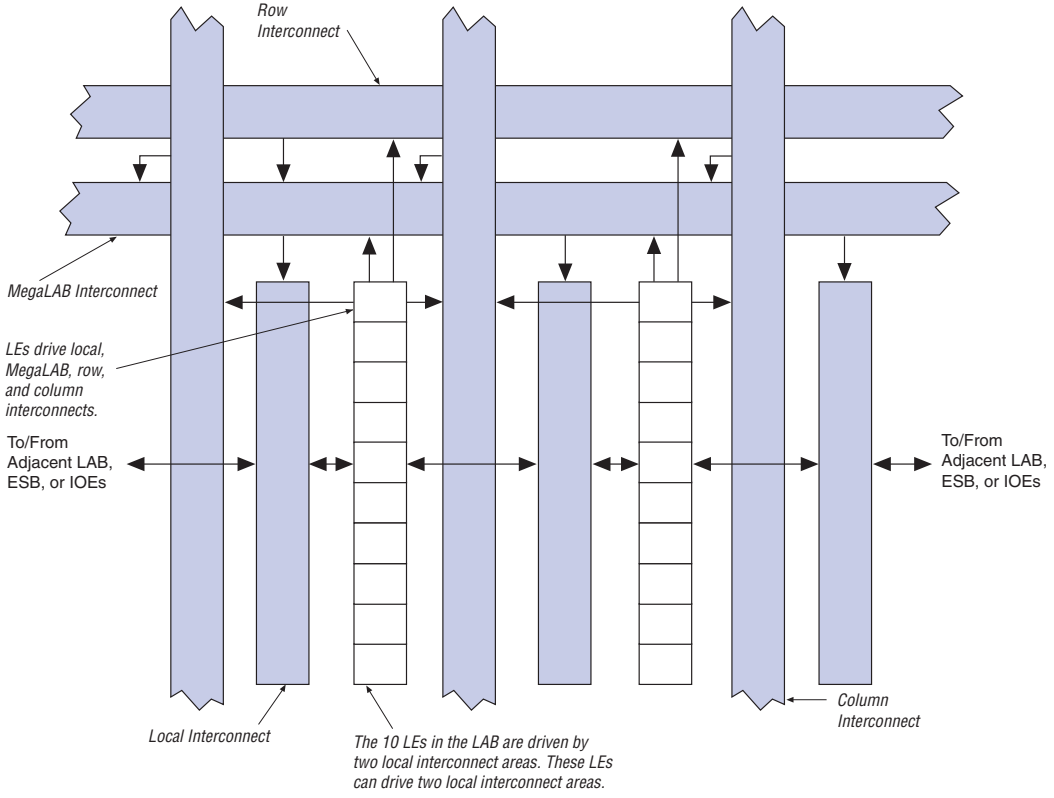
The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

*Figure 1. APEX 20KC Device Block Diagram*




APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

*Figure 3. LAB Structure*




Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset or to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

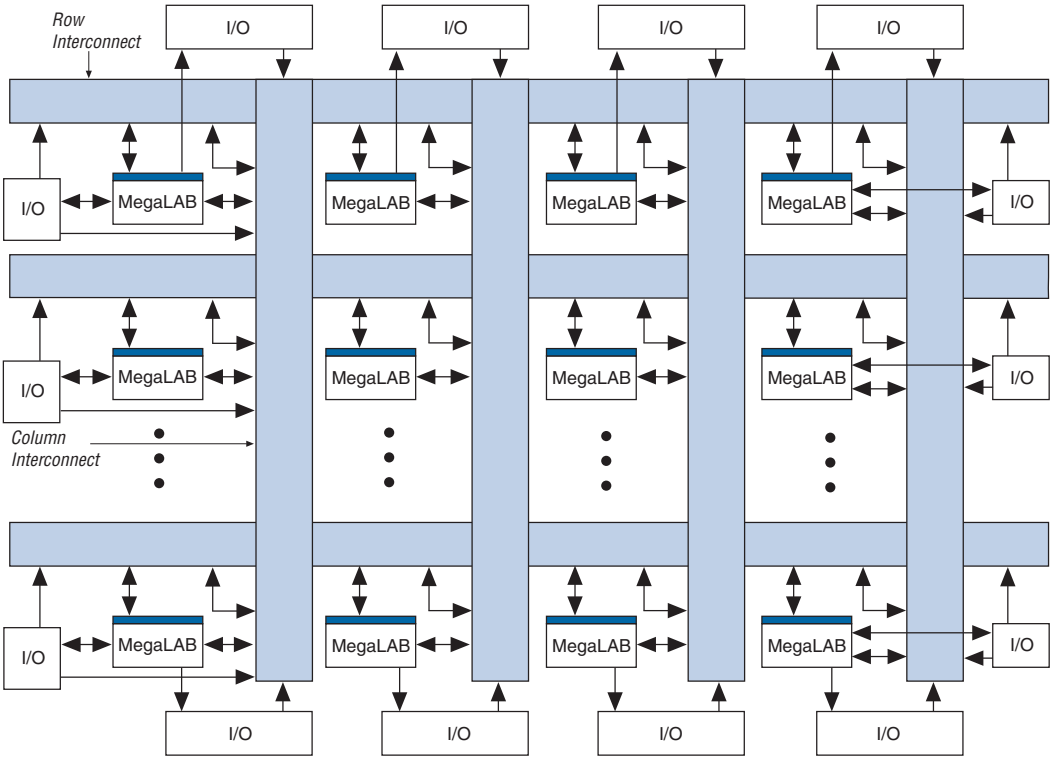
In addition to the two clear and preset modes, APEX 20KC devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## FastTrack Interconnect

In the APEX 20KC architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

*Figure 9. APEX 20KC Interconnect Structure*




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

*Table 8. APEX 20KC Routing Scheme*

| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Row I/O Pin | Column I/O Pin | LE | ESB | Local Interconnect | MegaLAB Interconnect | Row FastTrack Interconnect | Column FastTrack Interconnect | FastRow Interconnect |
| Row I/O pin | | | | | ✓ | ✓ | ✓ | ✓ | |
| Column I/O pin | | | | | | | | ✓ | ✓ |
| LE | | | | | ✓ | ✓ | ✓ | ✓ | |
| ESB | | | | | ✓ | ✓ | ✓ | ✓ | |
| Local interconnect | ✓ | ✓ | ✓ | ✓ | | | | | |
| MegaLAB interconnect | | | | | ✓ | | | | |
| Row FastTrack interconnect | | | | | | ✓ | | ✓ | |
| Column FastTrack interconnect | | | | | | ✓ | ✓ | | |
| FastRow interconnect | | | | | ✓ | | | | |

## Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

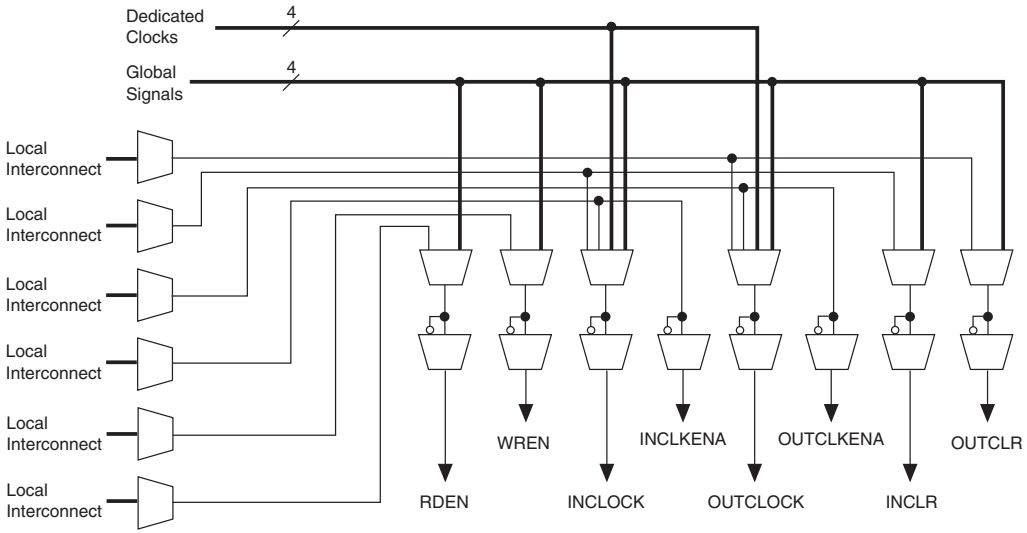
In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

For more information on APEX 20KC devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

*Figure 24. ESB Control Signal Generation*




An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

*Table 9. APEX 20KC Programmable Delay Chains*

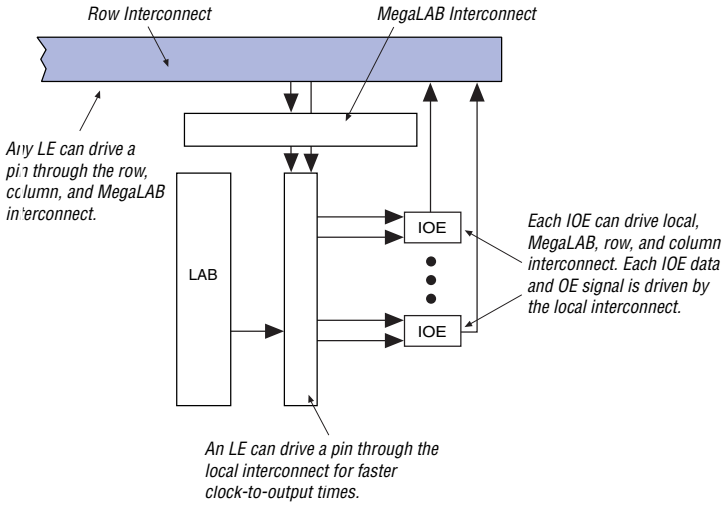
| Programmable Delay | Quartus II Logic Option |
|---|---|
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input registers |
| Core to output register delay | Decrease input delay to output register |
| Output register $t_{CO}$ delay | Increase delay to output pin |
| Clock enable delay | Increase clock enable delay |

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

*Notes to Figure 25:*
(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

***Figure 26. Row IOE Connection to the Interconnect***



## Advanced I/O Standard Support

APEX 20KC IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KC devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KC device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL at up to 156 Mbps per channel with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K400C and larger APEX 20KC devices support the LVDS interface for data pins (EP20K200C devices support LVDS clock pins, but not data pins). EP20K400C and EP20K600C devices support LVDS for data pins at up to 840 Mbps per channel. EP20K1000C devices support LVDS on 16 channels at up to 750 Mbps.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for the LVDS I/O standard, they support all of the other I/O standards. Figure 28 shows the arrangement of the APEX 20KC I/O banks.

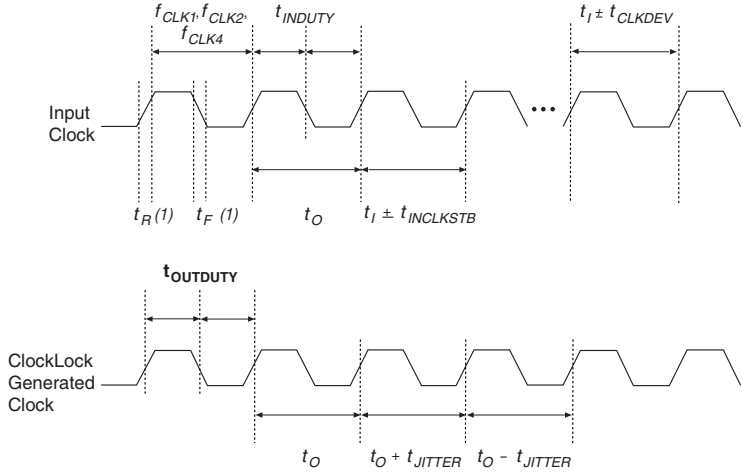
## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20KC ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KC devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 29 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

***Figure 29. Specifications for the Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*




***Note to Figure 29:***

(1) Rise and fall times are measured from 10% to 90%.

*Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -7 Speed Grade | | -8 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{CLOCK1\_EXT}$ | Output clock frequency for external clock1 output | 3.3-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 2.5-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 1.8-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | GTL+ | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | LVDS | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 2.5-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | 1.8-V LVTTL | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | GTL+ | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-2 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class I | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | SSTL-3 Class II | *(5)* | *(5)* | *(5)* | *(5)* | MHz |
| | | LVDS | *(5)* | *(5)* | *(5)* | *(5)* | MHz |

***Notes to Tables 11 and 12:***

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ $f_{VCO}$ ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

## SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

*Table 20. APEX 20KC Device Capacitance* *Note (10)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 17 through 20:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and time periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KC device recommended operating conditions, shown in Table 18 on page 55.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(10) Capacitance is sample-tested only.

Tables 21 through 35 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

*Table 21. LVTTL I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –12 mA, $V_{CCIO}$ = 3.0 V *(1)* | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 12 mA, $V_{CCIO}$ = 3.0 V *(2)* | | 0.4 | V |

*Table 24. 1.8-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.7 | 1.9 | V |
| $V_{IH}$ | High-level input voltage | | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | 0.35 × $V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 mA *(1)* | $V_{CCIO}$ – 0.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA *(2)* | | 0.45 | V |

*Table 25. 3.3-V PCI Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.3 × $V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10 | | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |

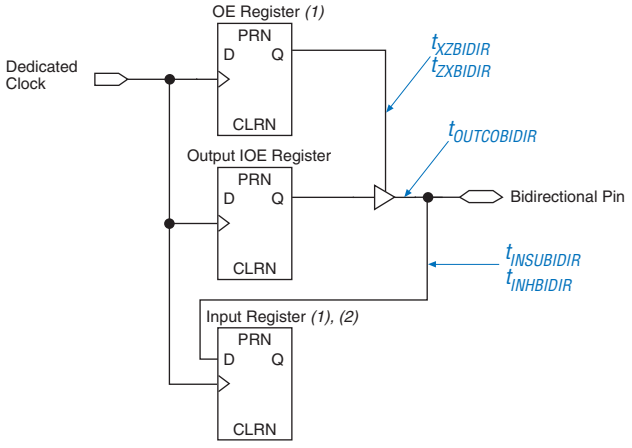
*Table 26. 3.3-V PCI-X Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.35 × $V_{CCIO}$ | V |
| $V_{IPU}$ | Input pull-up voltage | | 0.7 × $V_{CCIO}$ | | | V |
| $I_{IL}$ | Input pin leakage current | 0 < $V_{IN}$ < $V_{CCIO}$ | –10.0 | | 10.0 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |
| $L_{pin}$ | Pin Inductance | | | | 15.0 | nH |

*Table 27. 3.3-V LVDS I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{OD}$ | Differential output voltage | $R_L$ = 100 Ω | 250 | | 650 | mV |
| Δ $V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{OS}$ | Output offset voltage | $R_L$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| Δ $V_{OS}$ | Change in $V_{OS}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{TH}$ | Differential input threshold | $V_{CM}$ = 1.2 V | –100 | | 100 | mV |
| $V_{IN}$ | Receiver input voltage range | | 0.0 | | 2.4 | V |
| $R_L$ | Receiver differential input resistor (external to APEX devices) | | 90 | 100 | 110 | Ω |

*Figure 35. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 35:*

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the "Output Enable Routing = Single-Pin" option in the Quartus II software to set the output enable register.

(2) Use the "Decrease Input Delay to Internal Cells = OFF" option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set "Decrease Input Delay to Internal Cells = ON" and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 36 to 38 describes the $f_{MAX}$ timing parameters shown in Figure 32. Table 39 describes the functional timing parameters.

*Table 36. APEX 20KC $f_{MAX}$ LE Timing Parameters*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time before clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in to data-out |

*Table 51. EP20K400C $f_{MAX}$ ESB Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.30 | | 1.51 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.35 | | 2.49 | | 2.72 | ns |
| $t_{ESBAWC}$ | | 2.92 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.05 | | 3.44 | | 3.85 | ns |
| $t_{ESBWASU}$ | 0.45 | | 0.50 | | 0.54 | | ns |
| $t_{ESBWAH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.57 | | 0.63 | | 0.68 | | ns |
| $t_{ESBWDH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.25 | | 1.43 | | 1.56 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.03 | | 0.11 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 2.01 | | 2.27 | | 2.45 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.24 | | –0.28 | | ns |
| $t_{ESBRADDRSU}$ | 0.02 | | 0.00 | | –0.02 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.28 | | 1.43 | ns |
| $t_{ESBDATACO2}$ | | 2.10 | | 2.52 | | 2.82 | ns |
| $t_{ESBDD}$ | | 2.50 | | 2.97 | | 3.32 | ns |
| $t_{PD}$ | | 1.48 | | 1.78 | | 2.00 | ns |
| $t_{PTERMSU}$ | 0.58 | | 0.72 | | 0.81 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.29 | | 1.45 | ns |

*Table 52. EP20K400C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.19 | ns |
| $t_{F5-20}$ | | 0.94 | | 1.06 | | 1.25 | ns |
| $t_{F20+}$ | | 1.73 | | 1.96 | | 2.30 | ns |

*Table 53. EP20K400C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 54. EP20K400C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.37 | | 1.52 | | 1.64 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.25 | 2.00 | 4.61 | 2.00 | 5.03 | ns |
| $t_{INSUPLL}$ | 0.80 | | 0.91 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.27 | 0.50 | 2.55 | - | - | ns |

*Table 59. EP20K600C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 60. EP20K600C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.28 | | 1.40 | | 1.45 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.29 | 2.00 | 4.77 | 2.00 | 5.11 | ns |
| $t_{INSUPLL}$ | 0.80 | | 0.91 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.37 | 0.50 | 2.63 | - | - | ns |

*Table 61. EP20K600C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.03 | | 2.57 | | 2.97 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.29 | 2.00 | 4.77 | 2.00 | 5.11 | ns |
| $t_{XZBIDIR}$ | | 8.31 | | 9.14 | | 9.76 | ns |
| $t_{ZXBIDIR}$ | | 8.31 | | 9.14 | | 9.76 | ns |
| $t_{INSUBIDIRPLL}$ | 3.99 | | 4.77 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.37 | 0.50 | 2.63 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 6.35 | | 6.94 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 6.35 | | 6.94 | | - | ns |

*Table 62. EP20K1000C $f_{MAX}$ LE Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.01 | | 0.01 | | ns |
| $t_{H}$ | 0.10 | | 0.10 | | 0.10 | | ns |
| $t_{CO}$ | | 0.27 | | 0.30 | | 0.32 | ns |
| $t_{LUT}$ | | 0.66 | | 0.79 | | 0.92 | ns |