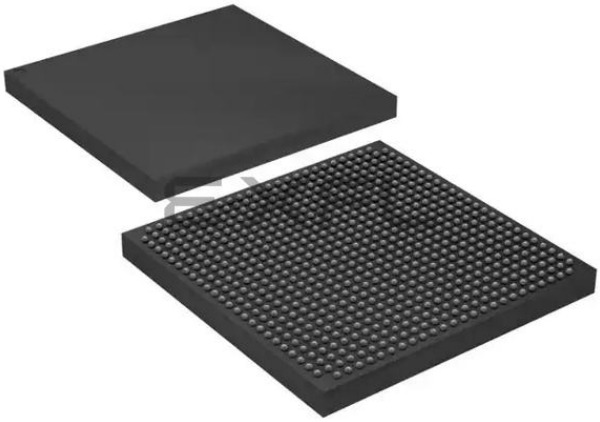

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	212992
Number of I/O	488
Number of Gates	1052000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k400cf672i8

…and More Features

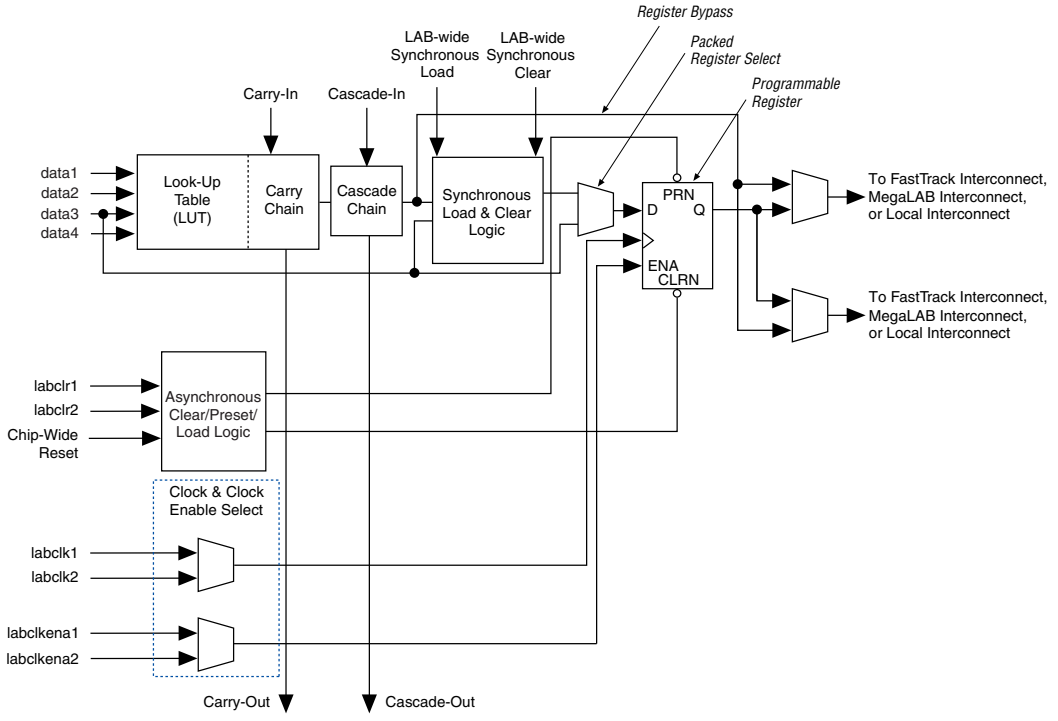
- Low-power operation design
  - 1.8-V supply voltage (see Table 2)
  - Copper interconnect reduces power consumption
  - MultiVolt™ I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offering programmable power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ feature providing programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR synchronous dynamic RAM (SDRAM) and ZBT static RAM (SRAM)
  - 16 input and 16 output LVDS channels at 840 megabits per second (Mbps)
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, SSTL-3 and SSTL-2, GTL+, and HSTL Class I
  - Supports hot-socketing operation
  - Pull-up on I/O pins before and during configuration

Table 2. APEX 20KC Supply Voltages

Feature	Voltage
Internal supply voltage (V_{CCINT})	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

Note to Table 2:
(1) APEX 20KC devices can be 5.0-V tolerant by using an external resistor.

Figure 5. APEX 20KC Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20KC architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

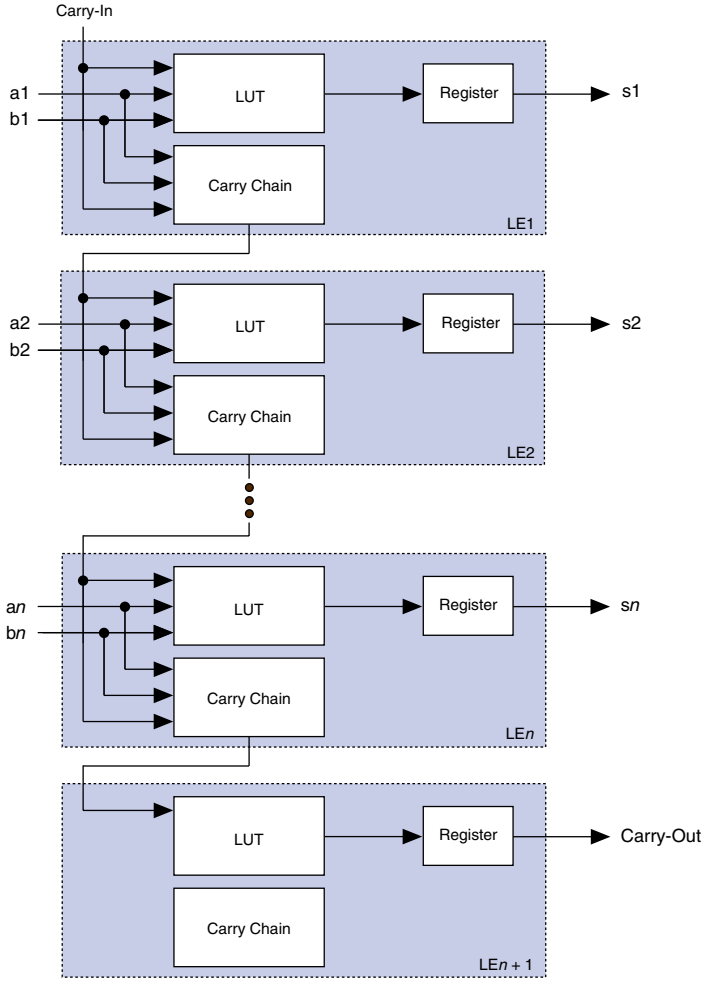
Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20KC architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by automatically linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 6. APEX 20KC Carry Chain



LE Operating Modes

The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset or to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20KC devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20KC architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

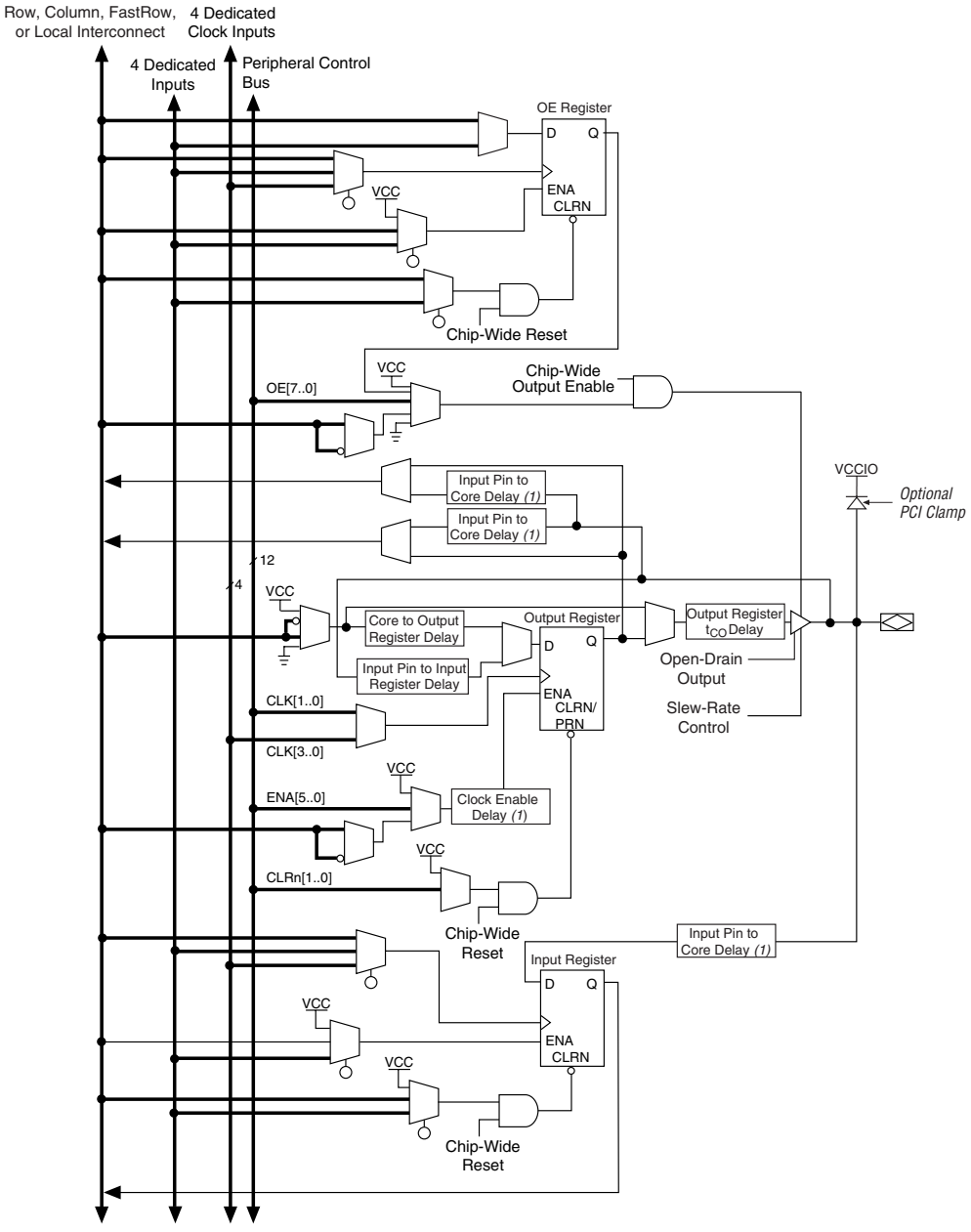
Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

Table 9. APEX 20KC Programmable Delay Chains

Programmable Delay	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input registers
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin
Clock enable delay	Increase clock enable delay

The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)*



Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades have PLLs and support the ClockLock and ClockBoost features.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

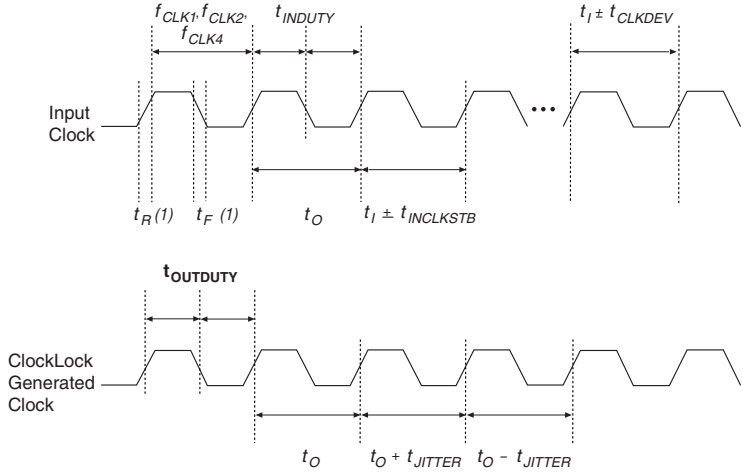
ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20KC ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KC devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 29 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Figure 29. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.



Note to Figure 29:

(1) Rise and fall times are measured from 10% to 90%.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

Table 11. APEX 20KC ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	%
$t_{OUTJITTER}$	RMS jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	%
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} *(2), (3)*	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} *(4)*	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz
f_{IN}	Input clock frequency	3.3-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		2.5-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		1.8-V LVTTL	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		GTL+	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-2 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class I	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		SSTL-3 Class II	*(5)*	*(5)*	*(5)*	*(5)*	MHz
		LVDS	*(5)*	*(5)*	*(5)*	*(5)*	MHz

Notes to Tables 11 and 12:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ f_{VCO} ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current *(8)*	V_I = 3.6 to 0.0 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current *(8)*	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

DC operating specifications on APEX 20KC I/O standards are listed in Tables 21 to 35.

Table 24. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage			0.35 × V_{CCIO}	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Table 25. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 32. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(2)*			V_{TT} – 0.8	V

Table 33. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			0.4	V

Table 34. 3.3-V AGP I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		0.39 × V_{CCIO}		0.41 × V_{CCIO}	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA

Table 35. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(3)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high Z)	GND ≤ V_{OUT} ≤ V_{CCIO}	–10		10	µA

Notes to Tables 21 through 35:

(1) The I_{OH} parameter refers to high-level output current.
(2) The I_{OL} parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) V_{REF} specifies center point of switching range.

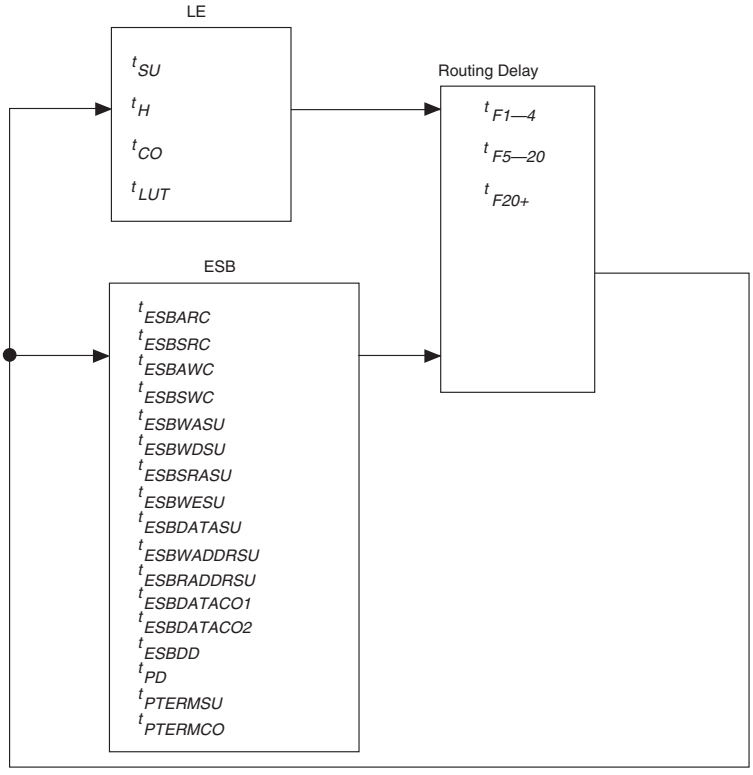
Figure 31 shows the output drive characteristics of APEX 20KC devices.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 32 shows the f_{MAX} timing model for APEX 20KC devices.

Figure 32. f_{MAX} Timing Model



Figures 33 and 34 show the asynchronous and synchronous timingwaveforms, respectively, for the ESB macroparameters in Table 37.

Table 69. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grad		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
1.8 V		1.18		1.41		1.57	ns
PCI		–0.52		–0.53		–0.56	ns
GTL+		–0.18		–0.29		–0.39	ns
SSTL-3 Class I		–0.67		–0.71		–0.75	ns
SSTL-3 Class II		–0.67		–0.71		–0.75	ns
SSTL-2 Class I		–0.67		–0.71		–0.75	ns
SSTL-2 Class II		–0.67		–0.71		–0.75	ns
LVDS		–0.69		–0.70		–0.73	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com